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A PROCESS FOR MANUFACTURING A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

The present invention relates to a process for manufacturing a semiconductor integrated circuit device, and particularly, but not exclusively, to a process for manufacturing a semiconductor integrated circuit device comprising a static random access memory (hereinafter abbreviated to 'SRAM').

The memory cell of an SRAM is formed by a flip-flop circuit in which a pair of inverter circuits are cross-coupled. Each of the inverter circuits has a load element and a drive MISFET (gate-insulated field effect transistor) connected in series. The power source potential is applied to the common terminal of the two load elements, and the common source of the two drive MISFETs receives the ground potential of the circuit.

A memory cell of the type in which a resistance element made of polycrystalline silicon is employed as a load element, is known. The memory cell of this type permits a high density of integration because the resistance element can be formed over a drive MISFET. An SRAM having memory cells of this type is disclosed in Japanese Patent Application Laid-open No. 54-128295, Japanese Patent Application No. 57-160999, and Japanese Patent Application No. 59-125247. A similar SRAM was also disclosed in the article entitled 'A 30ns 64k CMOS RAM' by Kim Hardee,

Michael Griffus and Ron Galves in IEEE International Solid-State Circuits Conference in 1984.

The inventors have investigated how it is possible to enhance the densities of integration of SRAMs, and have found the following problems:

First, wiring for cross-coupling two inverter circuits needs to be formed by different conductor layers. For example, in the SRAM described in Japanese Patent Application No. 59-125247, the first crossing wiring is of semiconductor material, while the second crossing wiring is formed of a conductor layer which lies above the gate electrodes of the SRAM and which is fabricated in the same step as two resistance elements. The second wiring is laid between the two resistance elements with the intention of preventing the area of a memory cell from enlarging. However, the pitch between the resistance elements must necessarily be increased. Since this pitch between the resistance elements determines the pitch between the gate electrodes of the MISFETs of a flip-flop circuit to be arranged below the resistance elements, the area of the memory cell is inevitably increased.

Secondly, the ground potential of the circuit is supplied to the common source of the two drive MISFETs by a wiring line which is made of semiconductor material. Since the resistance value of this wiring line may be as high as several tens of $\Omega/\square$, the potential thereof is liable to rise. Consequently, the difference between a power

source potential and the source potential becomes small. Thus, operating margins in writing and reading of information are reduced, and malfunctions are prone to occur. To suppress such malfunctions, the cross-sectional area of the wiring line needs to be increased so as to lower the resistance thereof. It is accordingly difficult to reduce the area of the memory cell.

Thirdly, in order to microminiaturize the memory cell while preventing soft errors attributed to alpha particles etc., Japanese Patent Application No. 57-160999 discloses a technique in which a P-type semiconductor region of comparatively high impurity concentration is provided under the source or drain region of the drive MISFET. It is necessary to prevent the P-type semiconductor region from being formed in a channel region in order to suppress fluctuation in the threshold voltage of the drive MISFET and increase in the substrate effect. Therefore, a mask for introducing a P-type impurity needs to be provided. As a result, a tolerance for mask registration is required, and this hampers the enhancement of the density of integration. Moreover, threshold voltage fluctuations occur due to mask misregistration.

Fourthly, the resistance value of the resistance element is set very large in order to lower the power dissipation. The current supply ability is therefore low, so that the speed of writing information into the memory cell is low.

The present invention therefore seeks to overcome, or

at least ameliorate, these problems.

Therefore, according to the present invention there is provided a process for manufacturing a semiconductor integrated circuit device having memory cells each of which includes first and second MISFETs in a first semiconductor region of a first conductivity type, a gate electrode of each of the first and second MISFETs being coupled to either the source or drain region of the other MISFET, the source and drain region of each MISFET not connected to the gate electrode being connected to wiring for a fixed potential; said process comprising:

forming an insulator film to serve as a mask for the introduction of impurity, on side walls of each gate electrode;

forming second semiconductor regions of a second conductivity type by the introduction of an impurity employing the gate electrodes and the insulator film as the principal mask, the second semiconductor regions being at least part of the source or drain regions of said MISFETs; and

forming third semiconductor regions under the source or drain regions of the MISFETs by the introduction of an impurity employing the gate electrodes and the insulator film as the principal mask, the third semiconductor regions being of the first conductivity type and having an impurity concentration higher than that of the first semiconductor region.

An embodiment of the invention will now be described in detail, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is an equivalent circuit diagram showing a memory cell of an SRAM for explaining one embodiment of the present invention;

Fig. 2A is a plan view of the memory cell of the SRAM of Fig. 1 for explaining one embodiment of the present invention;

Fig. 2B is a simplified schematic view with Fig. 2A showing features of the present invention;

Fig. 3 is a sectional view taken along line III - III in Fig. 2A; and

Figs. 4 to 10 are views showing the memory cell of an SRAM at various steps in the manufacturing process for explaining a process according to present invention, in which Figs. 4 to 6 are plan views, and Figs. 7 to 10 are sectional views.

The present invention will now be described with reference to an embodiment in which the invention is applied to the manufacture of an SRAM wherein the flip-flop circuit of a memory cell is constructed of two resistance elements and two MISFETs. Components having the same functions are assigned the same reference numerals in all the figures and shall not be repeatedly described.

Referring to Fig. 1, a word line WL extends in a row

direction, and a plurality of word lines are laid in a column direction (the direction in which the word lines extend shall hereinafter be called the row direction.)

A set of complementary data lines DL and $\overline{DL}$ extend in the column direction, and a plurality of sets are laid in the row direction (the direction in which the data lines extend shall hereinafter be called the column direction).

The memory cell of the SRAM comprises a flip-flop circuit which has a pair of input/output terminals, and switching MISFETs Q_{s1} and Q_{s2} which are respectively

connected to the input/output terminals. A plurality of such memory cells are arranged and disposed at the predetermined intersection between the word lines WL and the data lines DL, $\overline{DL}$, and constitute a memory cell array.

One of the source and drain regions of each switching MISFET is connected to the data line DL or $\overline{DL}$, while the other is connected to the input/output terminal of the flip-flop. The word line WL is connected to the gate electrodes of both the switching MISFETs Q_{s1} and Q_{s2}. The MISFETs Q_{s1} and Q_{s2} are switches which are controlled by the word line WL, and they serve to selectively connect the flip-flop circuit with the data lines DL and $\overline{DL}$.

The flip-flop circuit comprises MISFETs Q_1 and Q_2 and resistance elements R_1 and R_2. This flip-flop circuit stores information "1" or "0" which is transmitted from the data line DL or $\overline{DL}$. The flip flop circuit comprises two inverter circuits which are cross-coupled. The respective inverter circuits comprise the resistance element R_1 as a load and the drive MISFET Q_1, and those R_2 and Q_2. The output of one of the inverter circuits is applied to the gate electrode of the drive MISFET as the input of the other inverter circuit in mutual fashion. The cross-coupling therefore is achieved without

lowering the density of integration as will be described later, in accordance with the present invention.

The inverter circuits are supplied with a power source potential V_{cc} through the corresponding resistance elements R_1 and R_2. The resistance elements R_1 and R_2 control the magnitudes of currents flowing from the power source V_{cc}, and stably hold the written information. According to the present invention, the resistance elements R_1 and R_2 are self-biased as will be described later. That is, the resistance values of the resistance elements R_1 and R_2 are changed in correspondence with signals to be delivered as outputs by the inverter circuits.

The two inverter circuits are connected to a fixed potential, for example, the ground potential V_{ss} of circuitry by common wiring. To this end, the sources of the two drive MISFETs are connected to the common wiring for the ground potential. According to the present embodiment this wiring is not formed of a semiconductor region but is formed of a layer having a still lower resistance.

In the memory cell, the written information can be regarded as being stored in a parasitic capacitance C. The parasitic capacitance C includes principally the capacitance of the gate electrode of the MISFET Q_1 or Q_2 and the junction capacitance between one semiconductor

region (source region or drain region) and a substrate. According to the present embodiment the parasitic capacitances C are increased and soft errors are reduced without exerting influences on the MISFETs Q_1 and Q_2.

Fig. 2A is a plan view showing the memory cells of the SRAM of the present invention, Fig. 2B is a conceptual view of the memory cells in Fig. 2A, and Fig. 3 is a sectional view taken along line III - III in Fig. 2A. In the plan view of Fig. 2A and in plan views shown in Figs. 4 to 6 to be referred to later, insulator films other than field insulator films which are provided between respective conductor layers are not shown in order to facilitate understanding of the arrangement of the present embodiment.

Referring to Figs. 2A and 3, numeral 1 designates a semiconductor substrate which is made of single-crystal silicon of the n^--type. Numeral 2 designates a well region of the p^--type, which is provided in the predetermined part of the main surface of the semiconductor substrate 1. Shown at numeral 3 is a field insulator film, which is provided over the main surfaces of the semiconductor substrate 1 and the well region 2. This field insulator film 3 isolates semiconductor elements from one another. In the part of the well region 2 under the field insulator film 3, a p-type channel stopper region 4 is provided.

This channel stopper region 4 prevents parasitic MISFETs from operating, and electrically isolates the semiconductor elements.

In such a SRAM, the memory cells are constructed of n-channel MISFETs. The n-channel MISFETs are formed in the p^--type well region 2. Though not shown, the peripheral circuits of the memory cells (sense amplifiers, decoders, a timing signal generator, input and output circuits, etc.) include complementary MIS circuits. n-channel and p-channel MISFETs constituting the complementary MIS circuits are respectively formed in the p^--type well region 2 and the n^--type semiconductor substrate 1. Each MISFET is substantially surrounded with the field insulator film 3, and has its configuration stipulated by the same. That is, each MISFET is formed in a region (active region) where the field insulator film 3 is not provided.

The switching MISFETs Q_{s1} and Q_{s2} comprise insulator films 5 as gate insulator films, conductor layers 7A as gate electrodes, n^--type and n^+-type semiconductor regions 8 and 10 as source and drain regions, and p^+-type semiconductor regions 11 for preventing soft errors. The MISFET Q_1 comprises an insulator film 5 as a gate insulator film, a conductor layer 7D as a gate electrode, n^--type and n^+-type semiconductor regions

8 and 10 as source and drain regions, and a p^+-type semiconductor region 11 for preventing soft errors. The MISFET Q_2 comprises an insulator film 5 as a gate insulator film, a conductor layer 7C as a gate electrode, n^--type and n^+-type semiconductor regions 8 and 10 as source and drain regions, and a p^+-type semiconductor region 11 for preventing soft errors.

The MISFETs Q_1, Q_2, Q_{s1} and Q_{s2} are formed in the well region 2.

The gate insulator films 5 are made of silicon dioxide films which are formed on the parts of the main surface of the semiconductor substrate 1 as well as the well region 2 being the active regions.

The gate electrodes 7A, 7C and 7D are made of double-layer films (poly-cide structure) each of which comprises a film of polycrystalline silicon and a film of a silicide being the compound between silicon and a refractory metal (such as molybdenum, tantalum, titanium or tungsten), formed on the polycrystalline silicon film. The conductor layers 7A, 7C and 7D may be made of silicide films, refractory metal films, etc. The gate electrode 7A is extended in the row direction over the field insulator film 3. That is, the conductor layer 7A is used as the word line WL.

The source and drain regions are brought into the

so-called LDD (Lightly Doped Drain) structure by the semiconductor regions 8 and 10. In order to form the LDD structure, insulator films 9 are provided on both the sides of each of the conductor layers 7A to 7D in self-alignment thereto. The impurity introducing mask 9 may well be removed after the n^+-type semiconductor regions 10 and the p^+-type semiconductor regions 11 have been formed. The semiconductor region 8 has an impurity concentration lower than that of the semiconductor region 10. Thus, an electric field intensity at the p-n junction between the semiconductor region 8 and the well region 2 can be moderated. Since the junction depth (x_j) of the semiconductor region 8 is small, the coverage thereof under the gate electrode (into a region where a channel is formed) can be lessened. The semiconductor regions 8 are formed by ion implantation, using principally the gate electrodes 7A, 7C and 7D as a mask. The semiconductor region 10 constructs the substantial source region or drain region or the cross-coupling wiring of the flip-flop circuit. The semiconductor regions 10 are formed by introducing an impurity with ion implantation, using the impurity introducing mask 9. The insulator films 9 and the semiconductor regions 8 are omitted from all the plan views.

The layout of the MISFETs Q_1, Q_2, Q_{s1} and Q_{s2},

which is schematically shown in Fig. 2B, is done as follows in order to cross-couple the two inverters.

First, as regards the configuration of the field insulator film 3 within the memory cell, namely, the configuration of the MISFETs and the n^+-type semiconductor regions 10 as the wiring, Fig. 4 may be referred to.

The MISFETs Q_2 and Q_{s2} are formed in one active region defined by the field insulator film 3. In this active region, parts for forming the MISFETs Q_{s2} and Q_2 are respectively arranged in right upper and left lower areas in Figs. 2A and 2B. These two parts are made unitary by the n^+-type semiconductor region 10 which is formed obliquely from a right upper position to a left lower position in Figs. 2A and 2B. This semiconductor region 10 is the wiring for connecting the MISFETs Q_{s2} and Q_2, and is the source or drain region common to them. On the other hand, active regions for forming the MISFETs Q_1 and Q_{s1} are independently formed in right lower and left upper areas in Figs. 2A and 2B respectively. The connection between the MISFETs Q_1 and Q_{s1} is done by the gate electrode to be described below.

Secondly, as regards the configurations of the gate electrodes 7D and 7C of the respective MISFETs

Q_1 and Q_2, Fig. 5 may be referred to.

The conductor layer 7C which is the gate electrode of the MISFET Q_2 has one end part connected with the semiconductor region (source or drain region) 10 of the MISFET Q_{s1} through a contact hole 6 formed in the insulator film 5, and has the other end part connected with the semiconductor region (source or drain region) 10 of the other MISFET Q_1 through a contact hole 6. The conductor layer 7C forming the gate electrode of the MISFET Q_2, also serves as wiring for connecting the gate electrode of the MISFET Q_2 and the source or drain regions of the MISFETs Q_{s1} and Q_1 and as wiring for connecting the MISFETs Q_1 and Q_{s1}. The conductor layer 7D which is the gate electrode of the MISFET Q_1 has one end part connected with the semiconductor region (source or drain region) 10 of the MISFET Q_{s2} through a contact hole 6. The conductor layer 7D forming the gate electrode of the MISFET Q_1, also serves as wiring for connecting the gate electrode of the MISFET Q_1 and the source or drain region of the MISFET Q_{s2}. These two points will be understood by referring to Fig. 2B.

Owing to the configurations of the field insulator film 3 and the gate electrode 7C (and the gate electrode 7D), the cross coupling of the two inverter circuits is realized without hampering enhancement in the density of integration. More specifically, the semiconductor

regions 10 (and 8) defined by the field insulator film 3, and the gate electrodes 7C and 7D are used as the wiring for the cross coupling. Any wiring exclusive for the cross coupling and any area for connecting it are not necessary. No conductor layer for forming resistance elements is needed , either. Accordingly, the spacing between the gate electrodes 7C and 7D and the spacing between the resistance elements diminish.

The source and drain regions of the MISFETs Q_{s2} and Q_2 may be connected by shaping the gate electrode 7D similarly to the gate electrode 7C. Since the conductor layer 7C (7D) has as low a resistance as several $\Omega/\square$, it can be used as the wiring for connecting the MISFETs.

The sources of the two drive MISFETs Q_1 and Q_2 are supplied with the ground potential V_{ss} (= 0 V) of the circuitry by the conductor layer 7B. Since the conductor layer 7B is formed of the same material and by the same step as those of the conductor layers 7A, 7C and 7D, the resistance value thereof is as small as several $\Omega/\square$.

The conductor layer 7B is connected to the source regions of the MISFETs Q_1 and Q_2 through contact holes 6. This conductor layer 7B is provided while extending in the row direction over the field insulator film 3 substantially in parallel with the conductor layer 7A.

It forms a ground potential line common to a plurality of memory cells arranged in the row direction. The source regions of the MISFETs Q_1 and Q_2 are made larger than the drain regions thereof by parts for the connection with the conductor layer 7B. In particular, the source regions are made longer than the drain regions in the lengthwise direction of the gate electrodes 7C and 7D as shown in Fig. 2B. Thus, the conductor layer 7B can be prevented from overlapping the conductor layers 7C and 7D and can be made substantially rectilinear without lowering the density of integration.

Since the conductor layer 7B has a low resistance value, it can suppress the occurrence of the fluctuation of the potential thereof ascribable to currents flowing through the memory cells. Since,in this way, margins in the operations of writing and reading information can be widened, malfunctions can be prevented. Moreover, in a case where the wiring for supplying the ground potential is made of a semiconductor region, the cross-sectional area thereof needs to be enlarged for lowered resistance. This leads to the disadvantage that the width of the wiring enlarges. Since the resistance value of the conductor layer 7B is roughly one order smaller than that of the semiconductor region (the former is several hundredths of the latter), the area

of the ground potential line becomes smaller. It is accordingly possible to reduce the areas of the memory cells and the memory cell array in the column direction. Further, as exemplified in Fig. 2B, aluminum wiring L_{vss} needs to be run for a predetermined number of memory cells and to be connected with the conductor layer 7B so as to suppress the fluctuation of the potential thereof. In this regard, since the conductor layer 7B has the low resistance value, the number of the aluminum wiring lines L_{vss} can be reduced. Thus, especially the density of integration in the row direction in the memory cell array can be enhanced.

In order to prevent soft errors and to increase the parasitic capacitances of the storage nodes of the memory cell, the p^+-type semiconductor region 11 is formed.

The semiconductor region 11 is provided in contact with the semiconductor regions 10. This semiconductor region 11 is provided especially under the two semiconductor regions 10 of each of the MISFETs Q_1 and Q_2 and under one semiconductor region 10 of each of the MISFETs Q_{s1} and Q_{s2} (in a part enclosed with a dot-and-dash line 11 in Fig. 2A and 5). More specifically, it is added to the semiconductor regions 10 shown in Fig. 2B. In other words, the semiconductor region 11 is provided in those

parts of the memory cell which contribute to increase the parasitic capacitances C of the storage nodes for information. Since the p-n junction between the semiconductor region 11 and the semiconductor region 10 is one of the regions of high impurity concentrations, the junction capacitance thereof can be increased. Thus, the soft errors attributed to alpha particles can be prevented. The semiconductor region 11 is formed at an impurity concentration higher than that of the well region 2. Accordingly, it can serve as a barrier for suppressing the intrusion of minority carriers created in the well region 2 by alpha particles and can prevent the soft errors.

The semiconductor region 11 is formed by introducing an impurity by ion implantation, using the gate electrodes 7C and 7D and the impurity introducing mask 9. Accordingly, the semiconductor region 11 is constructed so as not to reach the region where the channel is formed. It does not affect the threshold voltages of the MISFETs Q_1 and Q_2. Since the allowance of mask registration for constructing the semiconductor region 11 is not required, the density of integration can be raised.

The impurity for constructing the semiconductor region 11 (for example, boron ions) has a higher diffusion coefficient when compared with the impurity for constructing

the semiconductor regions 10 (for example, arsenic ions). Since both the impurities are ion-implanted using the identical mask, the semiconductor region 11 is provided along the semiconductor regions 10 or so as to envelop the semiconductor regions 10. Thus, the areas of the p-n junctions between the semiconductor region 11 and the semiconductor regions 10 can be increased. The semiconductor region 11 is also formed under the semiconductor regions 8 by the difference of the diffusion coefficient. This can prevent the combination of depletion regions (the punch-through) between the semiconductor regions 10 functioning as the source region and the drain region. Thus, the short channel effect can be reduced.

The semiconductor region 11 may be used merely for enhancing the function of the barrier to the minority carriers. In that case, it can be formed in a deeper part apart from the semiconductor regions 10.

The semiconductor regions 10 may be constructed using the conductor layers 7A - 7C as a mask, the semiconductor region 11 may be constructed using the conductor layers 7A - 7C and the impurity introducing mask 9, and the semiconductor regions 8 need not be provided.

An insulator film 12 is formed so as to cover the MISFETs Q_1, Q_2, Q_{s1} and Q_{s2}. The insulator film 12 is made of, for example, a silicon oxide film.

The resistance elements R_1 and R_2 and the wiring for applying the power source potential V_{cc} thereto are formed on the insulator film 12. They are formed using a polycrystalline silicon layer 14 which is formed on the insulator film 12. The polycrystalline silicon layer 14 comprises parts (conductor layers) 14A whose resistance is lowered by introducing an impurity, and parts of high resistance 14B in which no impurity is introduced. The impurity, for example arsenic, is introduced into a part other than a part (14B) which is enclosed with a dot-and-dash line 14B indicated in Fig. 2A and 6.

The conductor layer 14A is placed over the conductor layer 7B (the wiring for the ground potential), and is extended in the row direction on the insulator film 12. It constructs the wiring for the power source potential, which is connected to the respective memory cells arranged in the row direction.

Owing to the fact that the conductor layer 14A (the wiring for the power source potential) and the conductor layer 7B (the wiring for the ground potential) are placed with the insulator film 12 intervening therebetween, a capacitor is inserted between the power source potential and the ground potential as illustrated in Fig. 2B. This capacitor has a higher capacitance because of the thinner insulator film, when compared with a capacitor

in which the conductor layer 14A is placed over a wiring for a ground potential made of a semiconductor region. This capacitor can reduce the malfunctions of the memory cells attributed to the fluctuation of the power source potential or the ground potential. Parts of the conductor layers 7B and 14A may be formed wider than the other parts so as to increase the capacitance.

The part 14B in which no impurity is introduced (the part which is enclosed with the dot-and-dash line 14B) is used as the resistance elements R_1 and R_2. One end of each of the resistance elements R_1 and R_2 is connected to the power source potential wiring 14A. The other end of the resistance element R_1 is connected to the source or drain region 10 of the MISFET Q_{s1} through a contact hole 6 and a contact hole 13 which is formed in the insulator film 12. In addition, the other end of the resistance element R_1 is connected to the gate electrode 7C of the MISFET Q_2 through the contact hole 13. In consequence, it is connected to the source or drain region 10 of the MISFET Q_1 through the gate electrode 7C. The other end of the resistance element R_2 is connected to the gate electrode 7D of the MISFET Q_1 through a contact hole 13. In addition, the other end of the resistor R_2 is connected to the common source or drain region 10 of the MISFETs Q_{s2} and Q_2 through contact

holes 6 and 13.

Since the gate electrodes 7C and 7D are shaped as stated before, the resistance elements R_1 and R_2 can complete all the necessary connections substantially by the mere connections thereof to the gate electrodes 7C and 7D. This point will become more apparent from Fig. 2B. Besides, owing to the foregoing shapes of the gate electrodes 7C and 7D, the wiring lines for the cross coupling of the flip-flop circuit, etc. need not be constructed by the use of the polycrystalline silicon 14. Accordingly, the resistance elements 14B can be constructed sufficiently long between the conductor layer 14A and the contact holes 13.

Since the resistance elements 14B are constructed sufficiently long, the resistance values thereof can be increased. Accordingly, standby currents flowing from the resistance elements 14B can be diminished in order to hold information. Moreover, the sufficiently long construction of the resistance elements 14B can prevent the combination (punch-through) of the depletion regions which are formed within the resistance elements 14B from the junctions between the resistance elements 14B and the conductor layer 14A and the junctions between the resistance elements 14B and the semiconductor regions 10 and the conductor layers 7C, 7D.

The resistance element 14B is placed over the conductor layer 7C or the conductor layer 7D through the insulator film 12, and is disposed extending in the column direction substantially similarly. That is, a MIS type structure (refer to Fig. 2B) is constructed in which the conductor layer 7C or 7D is a gate electrode, the insulator film 12 is a gate insulator and the resistance element 14B is a semiconductor. The n^+-type semiconductor region 10 and the conductor layer 14A can be regarded as source and drain regions. The conductor layer 14A is of the n^+-type because it is formed by introducing arsenic. Accordingly, the resistance element 14B can be regarded as the channel region of a parasitic n-channel MISFET. Now, let's consider a case where the potential of a high level is applied to the conductor layer 7D (gate electrode) of the MISFET Q_1 and where the potential of a low level is applied to the conductor layer 7C (gate electrode) of the MISFET Q_2. The current from the power source potential V_{cc} easily flow through the resistance element 14B (R_2), whereas it is difficult for it to flow through the resistance element 14B (R_1). That is, the resistance elements 14B (R_1, R_2) change their resistance values (are self-biased) in accordance with information (a voltage) written in the memory cell. As a result, the currents can be supplied in the direction

in which the voltage difference between "1" and "0" is clarified. This is effective to stably hold the information and to enhance the speed of writing the information into the memory cell.

An insulator film 15 is provided on the conductor layer 14A and the resistance elements 14B. The insulator film 15 electrically isolates the conductor layer 14A and the resistance elements 14B from a conductor layer 17 to be provided on them.

The conductor layer 17 is provided so as to be electrically connected to the predetermined semiconductor regions 10 through contact holes 16, to extend in the column direction across the conductor layers 7A, 7B and 14B over the insulator film 15 and to be placed over the conductor layers 7C, 7D and the resistance elements 14B. This conductor layer 17 serves to construct data lines DL and $\overline{DL}$. By stacking the conductor layers 7C and 17 and the resistance element 14B or the conductor layers 7D and 17 and the resistance element 14B, the area of the SRAM can be reduced, and hence, the density of integration thereof can be enhanced.

On the left (or right)-hand side of the memory cell in Fig. 2A, a memory cell which is in line symmetry with respect to a line Xa - Xa (or Xb - Xb) is arranged. The two memory cells form one unit, and a large number

of such units are arrayed in the row direction. Besides, on the upper (or lower) side of the illustrated memory cell in Fig. 2A, a memory cell which is in point symmetry with respect to a point Ya (or Yb) is arranged. The two memory cells form one unit, and a large number of such units are arrayed in the column direction.

Next, a method of manufacturing the present embodiment will be described.

Figs. 4 to 10 are views for explaining the method of manufacturing the SRAM shown in Figs. 2A, 2B and 3. Figs. 4 to 6 are plan views of the memory cell of the SRAM at several manufacturing steps, while Figs. 7 to 10 are sectional views thereof. Fig. 7 shows a section taken along line VII - VII in Fig. 4, Fig. 9 shows a section taken along line IX - IX in Fig. 5, and Fig. 10 shows a section taken along line X - X in Fig. 6.

First, a semiconductor substrate 1 of the n^--type made of single-crystal silicon is prepared. A well region 2 of the p^--type is formed in a predetermined main surface portion of the semiconductor substrate 1. By way of example, the well region 2 is formed in such a way that BF_2 ions at approximately 2×10^{12} atoms/cm^2 are introduced by ion implantation using an energy of approximately 60 keV and are subjected to drive-in diffusion.

A field insulator film 3 is formed on the predetermined parts of the semiconductor substrate 1 and the well region 2. Besides, channel stopper regions 4 of the p-type are formed in the predetermined parts of the well region 2. Used as the field insulator film 3 is a silicon oxide film which is formed by local thermal oxidation. By way of example, the channel stopper regions 4 are formed in such a way that BF_2 ions at approximately 3×10^{13} atoms/cm^2 are introduced by ion implantation using an energy of approximately 60 keV and are annealed by the step of forming the field insulator film 3.

Subsequently, as shown in Figs. 4 and 7, an insulator film 5 is formed on the parts of the main surfaces of the semiconductor substrate 1 and the well region 2 to become regions for forming semiconductor elements. The insulator film 5 is, for example, a silicon oxide film which is formed by thermal oxidation and which has a thickness of 200 - 300 Å. After the insulator film 5 has been formed, the predetermined parts thereof are removed so as to form contact holes 6.

As shown in Fig. 8, conductor layers 7A - 7D are formed on the field insulator film 3 and the insulator film 5. Each of the conductor layers 7A - 7D is made up of a double-layer film which is connected with the predetermined part of the main surface of the well

region 2 through the contact hole 6. That is, it is formed of a polycrystalline silicon film 71 which is formed by, e. g., CVD (Chemical Vapor Deposition) and in which phosphorus is introduced in order to lower the resistance value thereof, and a molybdenum silicide film 72 which is formed on the film 71 by sputtering. The thickness of the polycrystalline silicon film 71 is, e. g., approximately 2000 Å, and that of the molybdenum silicide film 72 is, e. g., approximately 3000 Å. Since the conductor layers 7A to 7D contain molybdenum silicide, their resistance value can be rendered several Ω/□.

Though not shown, an n-type semiconductor region is formed by the diffusion of the phosphorus introduced in the polycrystalline silicon film 71, in that main surface part of the well region 2 which is connected with the conductor layer 7B, 7C or 7D through the contact hole 6.

Subsequently, as shown in Fig. 8, semiconductor regions 8 of the n^--type are formed in order to construct LDD structures in the main surface of the well region 2 at the parts of both the sides of each of the conductor layers 7A, 7C and 7D with the insulator film 5 intervening therebetween. Using the conductor layers 7A, 7C and 7D and the field insulator film 3 as a mask for introducing an impurity, phosphorus is ion-implanted

at a dose of approximately 1 x 10^{13} atoms/cm^2 and an energy of approximately 50 keV by way of example. It is thereafter annealed. Thus, the semiconductor regions 8 are formed.

After the semiconductor regions 8 have been formed, an impurity introducing mask 9 is formed on both sides of each of the conductor layers 7A to 7D. By way of example, the impurity introducing mask 9 is formed in such a way that a silicon oxide film is provided on the whole surface of the resultant substrate by CVD, whereupon it is subjected to reactive ion etching. The mask 9 is an insulator film which is formed in self-alignment to the conductor layers 7A – 7D.

Using the impurity introducing mask 9 and the conductor layers 7A to 7D as a mask for ion implantation, semiconductor regions 10 of the n^+-type are formed in the predetermined parts of the main surface of the well region 2. The semiconductor regions 10 form the source regions or drain regions of MISFETs. By way of example, arsenic is ion-implanted at a dose of approximately 1 x 10^{16} atoms/cm^2 and an energy of approximately 80 keV and is thereafter annealed.

Thereafter, an impurity introducing mask is formed in order to form p^+-type semiconductor regions which serve principally to prevent soft errors. This mask

covers a part except an area which is enclosed with a dot-and-dash line 11 in Fig. 5.

In the state in which this impurity introducing mask has been formed, ion implantation is carried out using the mask 9 and the conductor layers 7C, 7D as a mask. Then, as shown in Figs. 5 and 9, the p^+-type semiconductor regions 11 are formed under the predetermined ones of the semiconductor regions 10. By way of example, boron is ion-implanted at a dose of approximately 1×10^{13} atoms/cm^2 and an energy of approximately 50 keV and is thereafter annealed. Referring to Fig. 5, the impurity to form the semiconductor regions 11 is introduced through the insulator film 5 into the region enclosed with the dot-and-dash line 11.

The conductor layers 7A to 7D and the semiconductor regions 8 and 10 are formed by the same manufacturing steps as the steps of forming MISFETs which constitute peripheral circuits. In addition, the semiconductor regions 11 may be formed under predetermined n^+-type semiconductor regions, for example, under the source regions and drain regions of MISFETs which constitute an input protection circuit.

After the step of forming the semiconductor regions 11, an insulator film 12 is formed. The insulator film 12 is, for example, a silicon oxide film which is formed

by CVD and which has a thickness of approximately 1000 - 2000 Å. The predetermined parts of the insulator film 12 overlying the conductor layers 7C, 7D and the semiconductor regions 10 are removed to form contact holes 13.

Thereafter, a polycrystalline silicon film 14 which is connected to the predetermined ones of the semiconductor regions 10 through the contact holes 13 is formed in order to form wiring 14A for a power source potential and resistance elements 14B. By way of example, the polycrystalline silicon film may be formed by CVD to a thickness of approximately 1000 - 2000 Å. An impurity for lowering a resistance value is introduced into that part of the polycrystalline silicon film which is other than regions for forming the resistance elements 14B and which becomes the power source potential wiring 14A. Arsenic used as the impurity is introduced by ion implantation, and is thereafter annealed. Since the impurity is introduced by ion implantation, the controllability of the resistance value is good. Moreover, owing to the ion implantation, the extention of the impurity under the impurity introducing mask is slight. Accordingly, the allowances of processing dimensions can be rendered small, and the resistance elements 14B can be constructed sufficiently long.

Thereafter, as shown in Figs. 6 and 10, the polycrystalline silicon film is patterned to form the conductor layer 14A which is used as the power source potential wiring and the resistance elements 14B which are used as resistance elements R_1 and R_2. The impurity for forming the conductor layer 14A is introduced into the part of the polycrystalline silicon film other than an area enclosed with a dot-and-dash line 14B in Fig. 6.

After the step of forming the conductor layer 14A and the resistance elements 14B, an insulator film 15 is formed. This insulator film 15 is, for example, a silicon oxide film which is formed by CVD and whose thickness is approximately 3000 - 4000 Å. The predetermined parts of the insulator films 5, 12 and 15 overlying the semiconductor regions 10 are removed to form contact holes 16.

Thereafter, as shown in Figs. 2A and 3, a conductor layer 17 which is electrically connected with the predetermined ones of the semiconductor regions 10 through the contact holes 16 is formed. The conductor layer 17 extends on the insulator film 15 in the column direction so as to cross the conductor layer 7A. It is, for example, an aluminum film formed by sputtering.

Thereafter, the processing steps of a passivation film etc. are carried out. The SRAM

is finished up by these series of manufacturing steps.

According to the process disclosed in the present invention, effects listed below may be attained:

(1) The gate electrode of one MISFET of a flip-flop circuit composed of two MISFETs is extended to form wiring for cross coupling. Owing to this construction, it is unnecessary to provide any special wiring for cross coupling between gate electrodes, so that the pitch between the gate electrodes can be reduced. Besides, owing to the above construction, it is unnecessary to provide any special wiring for cross coupling between resistance elements which lie above the gate electrodes, so that the pitch between the resistance elements can be reduced. Since the occupation area of the memory cell can be reduced by the aforementioned two features, the density of integration of an SRAM may be enhanced.

(2) The gate electrode of one MISFET of a flip-flop circuit composed of two MISFETs is extended to form wiring for cross coupling. Thus, the conductor layer formed by the same step as that of resistance elements makes it unnecessary to provide any special wiring for cross coupling, so that only a margin for the mask registration between the resistance elements

and wiring for a power source potential may be considered and that the resistance elements can be reduced in size or can be constructed sufficiently long. Since the resistance elements can be reduced in size, the occupation area of the memory cell can be reduced, and the density of integration of an SRAM can be enhanced.

(3) The gate electrodes of MISFETs and resistance elements, which constitute a memory cell, and data lines which are connected to the memory cell, are placed one over another, whereby a planar area can be reduced, so that the density of integration of an SRAM can be enhanced.

(4) The gate electrodes of MISFETs which constitute the flip-flop circuit of a memory cell, and resistance elements are placed one over the other. In this way, the resistance elements can be self-biased, so that charges to serve as information can be stably held. Also in this way, the margin of read-out in a reading operation can be widened.

(5) An impurity for decreasing the resistance value of a conductor layer made of polycrystalline silicon is introduced by ion implantation. Since the ion implantation is lower in the impurity concentration-dependence than thermal diffusion, the controllability of the resistance value can be improved. In addition, the resistance values of resistance elements can be controlled to high

precision. Owing to the use of the ion implantation, the coverage of the impurity under an impurity introducing mask for forming the resistance elements can be lessened, so that allowances for the processing dimensions of the resistance elements can be decreased. Accordingly, the occupation areas of the resistance elements can be reduced, and the density of integration of an SRAM can be enhanced. Besides, since the allowances for the processing dimensions of the resistance elements can be decreased, these resistance elements can be constructed sufficiently long. Since the resistance elements can be constructed sufficiently long, standby currents to flow through these resistance elements can be diminished. In addition, since the resistance elements can be formed long, the combination (punch-through) between depletion regions to spread in the resistance elements can be prevented.

(6) On the sides of the gate electrode of a predetermined MISFET which constitutes a memory cell, an impurity introducing mask is provided in self-alignment. The impurity introducing mask is used for providing a first semiconductor region which serves as a source region or a drain region, and a second semiconductor region which is opposite in the conductivity type to the first semiconductor region and which underlies the first semiconductor region. Thus, an allowance for the mask registration between

the gate electrode and the second semiconductor region is dispensed with, so that the density of integration of an SRAM can be enhanced. Besides, the coverage of the second semiconductor region into a channel region can be prevented, so that the fluctuation of the threshold voltage of the MISFET and the increase of the substrate effect can be prevented.

(7) As stated in Item (6), the second semiconductor region is provided along and under the first semiconductor region. For this reason, the capacitance of the p-n junction between the first semiconductor region and the second semiconductor region can be increased, so that the parasitic capacitance of a node for storing information can be increased. For the same reason, the second semiconductor region can be used as a barrier which prevents minority carriers, created in a well region (or a substrate), from entering the storage node of the information. Owing to the above two features, soft errors ascribable to alpha particles may be prevented.

(8) By providing each second semiconductor region in a part where a depletion region spreading to a region in which a channel is formed is suppressed, the combination (punch-through) of the depletion regions between a source region and a drain region can be prevented. Accordingly, the short channel effect can be reduced.

(9) Wiring for the ground potential, which is connected to memory cells, is formed of a conductor layer of low resistance made of poly-cide, silicide, a refractory metal or the like, so that the occupation area of the ground potential wiring in a memory cell array can be reduced. Since the number of aluminum wiring lines to be connected with the ground potential wiring can be decreased, the occupation area of the aluminum wiring in the memory cell array can be reduced. In addition, the resistance value of the ground potential wiring can be decreased, and the stability of the potential thereof can be improved, so that the margins of the operations of writing and reading information can be widened. Accordingly, malfunctions in the information writing and reading operations can be suppressed, and the electrical reliability of an SRAM can be enhanced.

(10) Since wiring for the ground potential and wiring for a power source potential are placed one over the other, the information of a memory cell is less influenced by fluctuations in the power source potential and/or the ground potential. In addition, the occupation area of the memory cell can be reduced, so that the density of integration of an SRAM can be enhanced.

While the invention made by the inventors has thus far been concretely described in conjunction with

one embodiment, it is a matter of course that the present invention is not restricted to the foregoing embodiment but that it can be variously modified within a scope not departing from the purport thereof.

For example, the flip-flop circuit of a memory cell may well be constructed of two P-channel MISFETs as load elements and two N-channel MISFETs. Besides, the load elements may be omitted.

A MISFET to constitute a memory cell need not have an LDD structure.

The conductivity types of various semiconductor regions may be reversed.

UK Patent Applications 87.20041 and 87.20042 (published under numbers 2195496 and 2195497 respectively) have been divided from this application and disclose matter also disclosed in the present application. Attention is therefore drawn to applications 87.20041 and 87.20042.

CLAIMS:

1. A process for manufacturing a semiconductor integrated circuit device having memory cells each of which includes first and second MISFETs in a first semiconductor region of a first conductivity type, a gate electrode of each of the first and second MISFETs being coupled to either the source or drain region of the other MISFET, the source and drain region of each MISFET not connected to the gate electrode being connected to wiring for a fixed potential; said process comprising:

forming an insulator film to serve as a mask for the introduction of impurity, on side walls of each gate electrode;

forming second semiconductor regions of a second conductivity type by the introduction of an impurity employing the gate electrodes and the insulator film as the principal mask, the second semiconductor regions being at least part of the source or drain regions of said MISFETs; and

forming third semiconductor regions under the source or drain regions of the MISFETs by the introduction of an impurity employing the gate electrodes and the insulator film as the principal mask, the third semiconductor regions being of the first conductivity type and having an impurity concentration higher than that of the first semiconductor region.

2. A process according to claim 1, wherein the third semiconductor regions are formed under the source or drain regions connected to the gate electrodes.

3. A process according to claim 1 or claim 2, wherein the second semiconductor regions lie in contact with the source or drain regions.

4. A process according to any one of claims 1 to 3, further comprising:

forming fourth semiconductor regions of the second conductivity type by introduction of an impurity employing the gate electrodes as a principal mask, the impurity concentration of the fourth semiconductor regions being lower than that of the second semiconductor regions.

5. A process according to claim 4, wherein each fourth semiconductor region is between the first semiconductor region and the second semiconductor region so as to form, together with the second semiconductor region, the source or drain region of the MISFETs.

6. A process for manufacturing a semiconductor integrated circuit device having a MISFET which is formed in

a first semiconductor region of a first conductivity type, said process comprising:

forming a fourth semiconductor region of a second conductivity type by introduction of an impurity employing a gate electrode of the MISFET as a principal mask;

forming an insulator film to serve as a mask for impurity introduction, on side walls of the gate electrode;

forming a second semiconductor region of the second conductivity type by the introduction of an impurity employing the gate electrode and the insulator film as the principal mask, the second semiconductor region having an impurity concentration higher than that of the first semiconductor region, the second and fourth semiconductor regions forming a source or drain region of the MISFET; and

forming a third semiconductor region under the source or drain region of the MISFET by the introduction of an impurity employing the gate electrode and the insulator film as the principal mask, the third semiconductor region being of the first conductivity type and having an impurity concentration higher than that of the first semiconductor region.

7. A method of manufacturing a semiconductor device substantially as any one herein described with reference to the accompanying drawings.

8. A device produced by a process according to any one of claims 1 to 7.