

DECIMATION OF BASEBAND DTV SIGNALS PRIOR TO CHANNEL EQUALIZATION IN DIGITAL TELEVISION SIGNAL RECEIVERS

This is a continuation-in-part of U.S. patent application serial No. 08/773,949 filed December 26, 1996.

The invention relates to radio receivers having the capability of receiving digital television (DTV) signals such as digital high-definition television (HDTV) signals, transmitted using quadrature amplitude modulation (QAM) of the principal carrier wave or transmitted using vestigial sideband (VSB) amplitude modulation of the principal carrier wave.

BACKGROUND OF THE INVENTION

A Digital Television Standard published 16 September 1995 by the Advanced Television Systems Committee (ATSC) specifies vestigial sideband (VSB) signals for transmitting digital television (DTV) signals in 6-MHz-bandwidth television channels such as those currently used in over-the-air broadcasting of National Television System Committee (NTSC) analog television signals within the United States. The VSB DTV signal is designed so its spectrum is likely to interleave with the spectrum of a co-channel interfering NTSC analog TV signal. This is done by positioning the pilot carrier and the principal amplitude-modulation sideband frequencies of the DTV signal at odd multiples of one-quarter the horizontal scan line rate of the NTSC analog TV signal that fall between the even multiples of one-quarter the horizontal scan line rate of the NTSC analog TV signal, at which even multiples most of the energy of the luminance and chrominance components of a co-channel interfering NTSC analog TV signal will fall. The video carrier of an NTSC analog TV signal is offset 1.25 MHz from the lower limit frequency of the television channel. The carrier of the DTV signal is offset from such video carrier by 59.75 times the horizontal scan line rate of the NTSC analog TV signal, to place the carrier of the DTV signal about 309,877.6 Hz from the lower limit frequency of the television channel. Accordingly, the carrier of the DTV signal is about 2,690,122.4 Hz from the middle frequency of the television

channel. The exact symbol rate in the Digital Television Standard is $(684/286)$ times the 4.5 MHz sound carrier offset from video carrier in an NTSC analog TV signal.

The number of symbols per horizontal scan line in an NTSC analog TV signal is 684, and 286 is the factor by which horizontal scan line rate in an NTSC analog TV signal

5 is multiplied to obtain the 4.5 MHz sound carrier offset from video carrier in an NTSC analog TV signal. The symbol rate is 10.762238×10^6 symbols per second, which can be contained in a VSB signal extending 5.381119 MHz from DTV signal carrier.

That is, the VSB signal can be limited to a band extending 5.690997 MHz from the lower limit frequency of the television channel.

10 The ATSC standard for digital HDTV signal terrestrial broadcasting in the United States of America is capable of transmitting either of two high-definition television (HDTV) formats with 16:9 aspect ratio. One HDTV format uses 1920 samples per scan line and 1080 active horizontal scan lines per 30 Hz frame with 2:1 field interlace. The other HDTV format uses 1280 luminance samples per scan line
15 and 720 progressively scanned scan lines of television image per 60 Hz frame. The ATSC standard also accommodates the transmission of DTV formats other than HDTV formats, such as the parallel transmission of four television signals having normal definition in comparison to an NTSC analog television signal.

DTV transmitted by vestigial-sideband (VSB) amplitude modulation (AM) for
20 terrestrial broadcasting in the United States of America comprises a succession of consecutive-in-time data fields each containing 313 consecutive-in-time data segments. There are 832 symbols per data segment. So, with the symbol rate being 10.76 MHz, each data segment is of 77.3 microseconds duration. Each segment of data begins with a line synchronization code group of four symbols having successive
25 values of +S, -S, -S and +S. The value +S is one level below the maximum positive data excursion, and the value -S is one level above the maximum negative data excursion. The initial line of each data field includes a field synchronization code group that codes a training signal for channel-equalization and multipath suppression procedures. The training signal is a 511-sample pseudo-noise sequence (or

"PN-sequence") followed by three 63-sample PN sequences. The middle one of these 63-sample PN sequences is transmitted in accordance with a first logic convention in the first line of each odd-numbered data field and in accordance with a second logic convention in the first line of each even-numbered data field, the first and second
5 logic conventions being one's complementary respective to each other. The other two 63-sample PN sequences and the 511-sample PN sequence are transmitted in accordance with the same logic convention in all data fields.

The data within data lines are trellis coded using twelve interleaved trellis codes, each a 2/3 rate trellis code with one uncoded bit. The interleaved trellis codes
10 are subjected to Reed-Solomon forward error-correction coding, which provides for correction of burst errors arising from noise sources such as a nearby unshielded automobile ignition system. The Reed-Solomon coding results are transmitted as 8-level (3 bits/symbol) one-dimensional-constellation symbol coding for over-the-air transmission, which transmissions are made without symbol precoding separate from
15 the trellis coding procedure. The Reed-Solomon coding results are transmitted as 16-level (4 bits/symbol) one-dimensional-constellation symbol coding for cablecast, which transmissions are made without precoding. The VSB signals have their natural carrier wave, which would vary in amplitude depending on the percentage of modulation, suppressed.

20 The natural carrier wave is replaced by a pilot carrier wave of fixed amplitude, which amplitude corresponds to a prescribed percentage of modulation. This pilot carrier wave of fixed amplitude is generated by introducing a direct component shift into the modulating voltage applied to the balanced modulator generating the amplitude-modulation sidebands that are supplied to the filter supplying the VSB
25 signal as its response. If the eight levels of 3-bit symbol coding have normalized values of -7, -5, -3, -1, +1, +3, +5 and +7 in the carrier modulating signal, the pilot carrier has a normalized value of 1.25. The normalized value of +S is +5, and the normalized value of -S is -5.

VSB signals using 8-level symbol coding will be used in over-the-air broadcasting within the United States, and VSB signals using 16-level symbol coding can be used in over-the-air narrowcasting systems or in cable-casting systems.

However, certain cable-casting is likely to be done using suppressed-carrier

5 quadrature amplitude modulation (QAM) signals instead, rather than using VSB signals. This presents television receiver designers with the challenge of designing receivers that are capable of receiving either type of transmission and of automatically selecting suitable receiving apparatus for the type of transmission currently being received.

10 It is assumed that the data format supplied for symbol encoding is the same in transmitters for the VSB DTV signals and in transmitters for the QAM DTV signals. The VSB DTV signals modulate the amplitude of only one phase of the carrier at symbol rate of 10.76×10^6 symbols per second to provide a real signal unaccompanied by an imaginary signal, which real signal fits within a 6MHz band because of its VSB
15 nature with carrier near edge of band. Accordingly, the QAM DTV signals, which modulate two orthogonal phases of the carrier to provide a complex signal comprising a real signal and an imaginary signal as components thereof, are designed to have a symbol rate of 5.38×10^6 symbols per second, which complex signal fits within a 6MHz band because of its QAM nature with carrier at middle of band.

20 Processing after symbol decoding is similar in receivers for the VSB DTV signals and in receivers for the QAM DTV signals, assuming the data format supplied for symbol encoding is the same in transmitters for the VSB DTV signals and in transmitters for the QAM DTV signals. The data recovered by symbol decoding are supplied as input signal to a data de-interleaver, and the de-interleaved data are
25 supplied to a Reed-Solomon decoder. Error-corrected data are supplied to a data de-randomizer which regenerates packets of data for a packet decoder. Selected packets are used to reproduce the audio portions of the DTV program, and other selected packets are used to reproduce the video portions of the DTV program.

The zero-intermediate-frequency (ZIF) receivers, which perform amplification and channel selection at baseband, that are used for receiving QAM DTV signals are not well suited for receiving VSB DTV signals. This is because of problems with securing adequate adjacent-channel rejection in a ZIF receiver when the carrier is not at the center frequency of the channel. The tuners can be quite similar in receivers for the VSB DTV signals and in receivers for the QAM DTV signals if the receivers are of superheterodyne types, however. The differences in the receivers reside in the synchrodyning procedures used to translate the final IF signal to baseband and in the symbol decoding procedures. A receiver that is capable of receiving either VSB or QAM DTV signals is more economical in design if it does not duplicate the similar tuner circuitry prior to synchrodyning to baseband and the similar receiver elements used after the symbol decoding circuitry. The challenge is in optimally constructing the circuitry for synchrodyning to baseband and for symbol decoding to accommodate both DTV transmission standards and in arranging for the automatic selection of the appropriate mode of reception for the DTV transmission currently being received.

DTV signal radio receivers are known of a type that uses double-conversion in the tuner followed by synchronous detection, having been used during field testing of the HDTV system used during development the ATSC standard. A frequency synthesizer generates first local oscillations that are heterodyned with the received VSB DTV signals to generate first intermediate frequencies (e. g., with 920 MHz center frequency and 922.69 MHz carrier). A passive LC bandpass filter selects these first intermediate frequencies from their image frequencies for amplification by a first intermediate-frequency amplifier, and the amplified first intermediate frequencies are filtered by a ceramic resonator filter that rejects adjacent channel signals. The first intermediate frequencies are heterodyned with second local oscillations to generate second intermediate frequencies (e. g., with 46.69 MHz carrier); and a filter, which can be of surface-acoustic-wave (SAW) type, selects these second intermediate frequencies from their images and from remnant adjacent channel responses for amplification by a second intermediate-frequency amplifier. The response of the second intermediate-frequency amplifier is supplied to a third mixer to be

synchrodyne to baseband with third local oscillations of fixed frequency. The third local oscillations of fixed frequency can be supplied in 0° phasing and in 90° phasing, thereby implementing separate in-phase and quadrature-phase synchronous detection procedures during synchrodyne. Synchrodyne is the procedure of multiplicatively
5 mixing a modulated signal with a wave having a fundamental frequency the same as the carrier of the modulated signal, being locked in frequency and phase thereto, and lowpass filtering the result of the multiplicative mixing to recover the modulating signal at baseband, baseband extending from zero frequency to the highest frequency in the modulating signal.

10 Separately digitizing in-phase and quadrature-phase synchronous detection results generated in the analog regime presents problems with regard to the synchronous detection results satisfactorily tracking each other after digitizing; quantization noise introduces pronounced phase errors in the complex signal considered as a phasor. These problems can be avoided in DTV signal radio receivers
15 of types performing the in-phase and quadrature-phase synchronous detection procedures in the digital regime. By way of example, the response of the second intermediate-frequency amplifier is digitized at twice the Nyquist rate of the symbol coding. The successive samples are considered to be consecutively numbered in order of their occurrence; and odd samples and even samples are separated from each other
20 to generate respective ones of the in-phase (or real) and quadrature-phase (or imaginary) synchronous detection results. Quadrature-phase (or imaginary) synchronous detection takes place after Hilbert transformation of one set of samples using appropriate finite-impulse-response (FIR) digital filtering, and in-phase (or real) synchronous detection of the other set of samples is done after delaying them for a
25 time equal to the latency time of the Hilbert-transformation filter. The methods of locking the frequency and phase of synchronous detection and the methods of locking the frequency and phase of symbol decoding differ in the VSB and QAM DTV receivers.

These types of known DTV signal radio receiver present some problem in the design of the tuner portion of the receiver because the respective carrier frequencies of VSB DTV signals and of QAM DTV signals are not the same as each other. The carrier frequency of a QAM DTV signal is at the middle of a 6-MHz-wide TV channel, but the carrier frequency of a VSB DTV signal nominally is about 310 kHz above the lower limit frequency of the TV channel. Accordingly, the third local oscillations of fixed frequency, which are used for synchrodyning to baseband, must be of different frequency when synchrodyning VSB DTV signals to baseband than when synchrodyning QAM DTV signals to baseband. The 2.69 MHz difference between the two carrier frequencies is larger than that which is readily accommodated by applying automatic frequency and phase control to the third local oscillator. A third oscillator that can switchably select between two frequency-stabilizing crystals is a practical necessity. In such an arrangement, of course, alterations in the tuner circuitry are involved with arranging for the automatic selection of the appropriate mode of reception for the DTV transmission currently being received. The radio-frequency switching that must be done reduces the reliability of the tuner. The RF switching and the additional frequency-stabilizing crystal for the third oscillator increase the cost of the tuner appreciably.

Radio receivers for receiving digital television signals, in which receiver the final intermediate-frequency signal is somewhere in the 1 - 8 MHz frequency range rather than at baseband, are described by C. B. Patel *et alii* in U. S. patent No. 5,479,449 issued 26 December 1995, entitled **DIGITAL VSB DETECTOR WITH BANDPASS PHASE TRACKER, AS FOR INCLUSION IN AN HDTV RECEIVER**, and included herein by reference. The use of infinite-impulse response filters for developing complex digital carriers in such receivers is described by C. B. Patel *et alii* in U. S. patent No. 5,548,617 issued 20 August 1996, entitled **DIGITAL VSB DETECTOR WITH BANDPASS PHASE TRACKER USING RADER FILTERS, AS FOR USE IN AN HDTV RECEIVER**, and incorporated herein by reference. The use of finite-impulse response filters for developing complex digital carriers in such receivers is described by C. B. Patel *et alii* in allowed U. S. patent

application serial No. 08/577,469 filed 22 December 1995, entitled **DIGITAL VSB DETECTOR WITH BANDPASS PHASE TRACKER USING NG FILTERS, AS FOR USE IN AN HDTV RECEIVER**, and incorporated herein by reference. The design of receivers for both QAM and VSB signals in which QAM/VSB receivers both types of signal are processed through the same intermediate-frequency amplifiers receivers is described by C. B. Patel *et alii* in U. S. patent No. 5,506,636 issued 9 April 1996, entitled **HDTV SIGNAL RECEIVER WITH IMAGINARY-SAMPLE-PRESENCE DETECTOR FOR QAM/VSB MODE SELECTION**, and incorporated herein by reference. U.S. patent No. 5,606,579 issued 25 February 1997 to C. B. Patel *et alii* and entitled **DIGITAL VSB DETECTOR WITH FINAL I-F CARRIER AT SUBMULTIPLE OF SYMBOL RATE, AS FOR HDTV RECEIVER** is incorporated herein by reference. U. S. patent application serial No. 5,659,372 issued 19 August 1997 by C. B. Patel *et alii* and entitled **DIGITAL TV DETECTOR RESPONDING TO FINAL-IF SIGNAL WITH VESTIGIAL SIDEBAND BELOW FULL SIDEBAND IN FREQUENCY** is incorporated herein by reference. Allowed U. S. patent application serial No. 08/266,753 filed 28 June 1994 by C. B. Patel *et alii* and entitled **RADIO RECEIVER FOR RECEIVING BOTH VSB AND QAM DIGITAL HDTV SIGNALS** is incorporated herein by reference. U. S. patent No. 5,715,012 issued 3 February 1998 to C. B. Patel *et alii* and entitled **RADIO RECEIVERS FOR RECEIVING BOTH VSB AND QAM DIGITAL HDTV SIGNALS** is incorporated herein by reference. These patents and patent applications are all assigned to Samsung Electronics Co., Ltd., pursuant to employee invention agreements already in force at the time the inventions disclosed in these patents and patent applications were made.

In the QAM/VSB radio receivers described in U. S. patents Nos. 5,506,636 and 5,715,012 the final intermediate-frequency signal is digitized, and synchrodyne procedures to obtain baseband samples are carried out in the digital regime. A tuner within the receiver includes elements for selecting one of channels at different locations in a frequency band used for transmitting DTV signals, a succession of

mixers for performing a plural conversion of signal received in the selected channel to a final intermediate-frequency (IF) signal, a respective frequency-selective amplifier between each earlier one of the mixers in that succession and each next one of said mixers in that succession, and a respective local oscillator for supplying oscillations to

5 each of the mixers. Each of these local oscillators supplies respective oscillations of substantially the same frequency irrespective of whether the selected DTV signal is a QAM signal or is a VSB signal. The final IF signal is digitized, and thereafter there are differences in signal processing depending on whether the selected DTV signal is a QAM signal or is a VSB signal. These differences are accommodated in digital

10 circuitry including QAM synchrodyning circuitry and VSB synchrodyning circuitry. The QAM synchrodyning circuitry generates real and imaginary sample streams of interleaved QAM symbol code, by synchrodyning the digitized final IF signal to baseband providing it is a QAM signal and otherwise processing the digitized final IF signal as if it were a QAM signal to be synchrodynd to baseband. The VSB

15 synchrodyning circuitry generates a real sample stream of interleaved VSB symbol code, by synchrodyning the digitized final IF signal to baseband providing it is a VSB signal and otherwise processing the digitized final IF signal as if it were a VSB signal to be synchrodynd to baseband. A detector determines by sensing the presence of a pilot carrier accompanying a DTV signal of VSB type whether or not the final IF

20 signal is a VSB signal to generate a control signal, which is in a first condition when the final IF signal apparently is not a VSB signal and is in a second condition when the final IF signal apparently is a VSB signal. Responsive to the control signal being in its first condition, the radio receiver is automatically switched to operate in a QAM signal reception mode; and responsive to the control signal being in its second

25 condition, the radio receiver is automatically switched to operate in a VSB signal reception mode.

U. S. patent No. 5,506,636, U. S. patent application serial No. 08/266,753 and U. S. patent application serial No. 08/614,471 were written presuming that the carrier frequency of a VSB DTV signal would be 625 kHz above lowest channel frequency,

30 as earlier proposed by a subcommittee of the Advanced Television Systems

Committee. This specification presumes that the carrier frequency of a VSB DTV signal is about 310 kHz above lowest channel frequency, as specified in Annex A of the Digital Television Standard published 16 September 1995.

5 The carrier of the final IF signal is preferably one prescribed subharmonic of a multiple of the symbol frequencies of both the QAM and VSB signals if the selected DTV signal is a QAM signal and is another prescribed subharmonic of that multiple if the selected DTV signal is a VSB signal. When the carrier frequency of a VSB DTV signal is nominally 310 kHz above lowest channel frequency, these prescribed subharmonics should differ in frequency by substantially 2.69 MHz. Digitizing the
10 final IF signal at this multiple of the symbol frequencies of both the QAM and VSB signals facilitates the generation of the digital carriers used to synchrodyne the QAM and VSB final IF signals to baseband. This multiple of the symbol frequencies of both the QAM and VSB signals should be low enough that digitization is practical, but is preferably above Nyquist rate.

15 In one type of these QAM/VSB radio receivers the prescribed subharmonic of a multiple of the symbol frequency of the QAM signal is substantially 2.69 MHz higher in frequency than the prescribed subharmonic of a multiple of the symbol frequency of said VSB signal. In a preferred such receiver the frequency of the QAM carrier in the final IF signal is 5.38 MHz, the first subharmonic of 10.76 MHz, and the
20 frequency of the VSB signal carrier in the final IF signal is 2.69 MHz, the third subharmonic of 10.76 MHz.

In another type of these QAM/VSB radio receivers the prescribed subharmonic of a multiple of the symbol frequency of the QAM signal is substantially 2.69 MHz lower in frequency than the prescribed subharmonic of a multiple of the
25 symbol frequency of the VSB signal. The VSB signal having its full sideband below carrier frequency in the final IF signal is sampled with better resolution in such embodiments of the invention. In a preferred such embodiment the frequency of the QAM carrier in the final IF signal is 5.38 MHz, the first subharmonic of 10.76 MHz,

and the frequency of the VSB signal carrier in the final IF signal is 8.07 MHz, the third subharmonic of the third harmonic of 10.76 MHz.

When synchrodyning is done in the digital regime, the generation of the digital carriers from read-only memory (ROM) is facilitated by digitizing the final IF signal of both the QAM and VSB signals at a sampling rate that is a multiple of each of their symbol rates. Phase-locking the frequency of the carrier used for synchrodyning to the carrier of the QAM or VSB signals to baseband is thereby facilitated.

Digitizing the QAM and VSB DTV signals at multiples of their symbol rates facilitates symbol synchronization, whether synchrodyning is done in the digital regime as described by Patel *et alii* or is done in the analog regime. In order to perform symbol synchronization satisfactorily, digital samples must be provided at a sample rate at least twice symbol rate. Supplying digital samples at a rate higher than symbol rate will increase the number of taps in the digital filters used for channel equalization of the baseband DTV signal, since the number of sample times in a ghost of any particular duration will increase in direct ratio to how many times the symbol rate the sampling rate is. Digitizing a QAM or VSB DTV signal at a multiple M times N of its symbol rate, M being a positive number at least one and N being a positive integer at least 2 allows the N:1 decimation of the digital DTV baseband signal before performing channel equalization thereof, so long as the Nyquist criterion for transmitting symbols is satisfied in the decimated digital signal.

SUMMARY OF THE INVENTION

In accordance with an aspect of the invention, the digitized DTV signal is decimated before performing channel equalization thereof, which reduces the number of samples in the kernels of the digital filters for performing channel equalization and reduces the cost of the DTV receiver substantially.

Decimation of a digitized VSB signal to a sampling rate less than twice its symbol rate (i. e., particularly to a sampling rate equal to its symbol rate) requires that symbol synchronization take place before the decimation procedure, in order that

symbol information not be lost in the decimation procedure. An aspect of the invention is performing symbol synchronization before that decimation procedure. A further aspect of the invention is a method of performing the symbol synchronization by steps of: extracting a signal associated with the required symbol rate and timing
5 from the baseband DTV data, detecting frequency and phase error between the extracted signal and the sampling rate of the analog-to-digital converter in the radio receiver portion of the DTV receiver, applying the detected frequency and phase error to a controlled oscillator as an automatic frequency and phase control signal, and generating from the oscillations of that controlled oscillator the sample clock signal
10 determining the sampling rate of the analog-to-digital converter.

The invention is embodied in a digital television (DTV) receiver including a radio receiver portion for selecting a channel for reception, for converting DTV signal in the selected channel to intermediate frequencies for filtering and amplification, and for synchrodyning an analog final intermediate-frequency output signal resulting from
15 that filtering and amplification to baseband, thereby to generate a baseband signal. The DTV receiver may be one designed for receiving QAM DTV signal, VSB DTV signal or both types of DTV signal. An analog-to-digital converter (ADC) is included in this radio receiver portion for sampling one of the signals therein and digitizing it so that the baseband signal is supplied from the radio receiver portion as a first stream
20 of digital samples descriptive of the baseband signal. A sample clock generator is connected for supplying a sample clock signal to time the sampling by the ADC so that the first stream of digital samples has a sample rate substantially equal to a prescribed multiple MN times the symbol rate of the DTV signal. MN is the product of a positive number M greater than one and of a positive integer N at least two. A
25 decimator is connected for receiving the first stream of digital samples and generating in response thereto a second stream of digital samples in which only every N^{th} one of the first stream of digital samples is reproduced at a sample rate that is one- N^{th} that of the first stream of digital samples. The number of taps required in a channel equalizer for performing channel equalization to generate a channel equalizer response is
30 reduced by the N:1 decimation of the second stream of digital samples. The resultant

saving in digital multipliers provides a substantial benefit in cost and reliability. A symbol synchronizer is included in the DTV receiver for correcting the symbol phase error in the channel equalizer response; and a symbol decoder is included in the DTV receiver for decoding symbols in the channel equalizer response, as corrected for
5 symbol phase error, to recover groups of bits corresponding to decoded symbols.

In a preferred embodiment of this type of DTV receiver the sample clock generator comprises an oscillator for supplying oscillations at a frequency controlled by an automatic frequency and phase control signal, and circuitry for generating the sample clock signal at a rate responsive to the oscillation frequency; and the symbol
10 synchronizer comprises an FIR filter for selecting only signal of a prescribed subharmonic of symbol rate from the first stream of digital samples, and an automatic frequency and phase control detector for detecting frequency and phase error between the sampling rate of the ADC and the prescribed subharmonic of the symbol rate as selected in the response of the FIR filter.

15 In another aspect of invention, a controlled oscillator used to time samples supplied from a sample clock generator is synchronized with the symbols in a baseband DTV signal, by developing an automatic-frequency-and-phase-control (AFPC) signal for the controlled oscillator from the symbol code despite the baud frequency being absent therefrom. This is done by subjecting the
20 baseband-DTV-signal symbol code to a narrow bandpass finite-impulse-response (FIR) digital filter timed by the samples supplied from the sample clock generator. A non-linear procedure that will generate second harmonics, such as squaring, is applied to the narrow bandpass FIR digital filter response to regenerate the baud frequency accompanied by a noise spectrum. An automatic-frequency-and-phase-control
25 detector detects the error of the oscillation frequency of the controlled oscillator respective to the regenerated baud frequency and provides a lowpass filtered response to the error signal applied to the controlled oscillator as its AFPC signal.

BRIEF DESCRIPTION OF THE DRAWING

FIGURE 1 is a block schematic diagram of initial portions of a digital television (DTV) receiver of a type that can embody the invention, including circuitry for detecting symbols in a DTV signal of QAM type, circuitry for detecting symbols in a DTV signal of VSB type, and an amplitude-and-group-delay equalizer for symbols selected from the circuitry for detecting symbols in a DTV signal of QAM type and the circuitry for detecting symbols in a DTV signal of VSB type.

FIGURE 2 is a block schematic diagram of the remaining portions of the DTV receiver of a type that can embody the invention, which are not shown in FIGURE 1.

FIGURE 3 is a detailed block schematic diagram of digital circuitry for synchrodyning QAM DTV signals to baseband, of digital circuitry for synchrodyning VSB DTV signals to baseband, and of circuitry associated with applying input signals to that QAM and VSB synchrodyning circuitry, as used in a DTV signal radio receiver of the type shown in FIGURES 1 and 2.

FIGURE 4 is a detailed block schematic diagram of circuitry for providing the sample clock generator, the look-up table read-only memories (ROMs) for supplying digital descriptions of the complex carriers used for synchrodyning digital QAM signals and digital VSB signals at final IF signal frequencies each to baseband, and the address generators for those ROMs, which circuitry is included in certain DTV signal radio receivers of the type that can embody the invention.

FIGURE 5 is a detailed block schematic diagram of circuitry similar to that of FIGURE 4, modified so that the address generator for the ROMs supplying digital descriptions of the complex carrier used for synchrodyning digital QAM signals to baseband and the ROMs supplying digital descriptions of the complex carrier used for synchrodyning digital VSB signals to baseband share an address counter in common.

FIGURE 6 is a detailed block schematic diagram of circuitry for converting digital samples to complex form in DTV signal radio receivers embodying the invention, which circuitry includes a Hilbert transformation filter for generating

imaginary samples from real samples, and which includes delay compensation for the real samples equivalent to the latency of that filter.

FIGURE 7 is a detailed block schematic diagram of a pair of all-pass digital filters of infinite-impulse-response (IIR) type designed based on Jacobian elliptic functions and exhibiting a constant $\pi/2$ difference in phase response for the digitized bandpass signals, as are known in the prior art and can be employed for converting digital samples to complex form in DTV signal radio receivers embodying the invention.

FIGURES 8 and 9 are block schematic diagrams of changes that can be made the filter circuitry of FIGURE 7 to remove redundant delay.

FIGURE 10 is a detailed block schematic diagram of a pair of all-pass digital filters of finite-impulse-response (FIR) type exhibiting a constant $\pi/2$ difference in phase response for the digitized bandpass signals, as can be employed for converting digital samples to complex form in DTV signal radio receivers embodying the invention.

FIGURE 11 is a graph of the constraints on the final intermediate frequencies to which the carriers of a QAM DTV signal and a VSB DTV signal can be frequency translated, when the carrier of a VSB DTV signal is lower in frequency than the carrier of a QAM DTV signal in the final IF signal, so the full sideband of the VSB DTV signal is higher in frequency than its vestigial sideband in the final IF signal, and when the sample rate during digitization is constrained to 21.52×10^6 samples per second.

FIGURE 12 is a graph of the constraints on the final intermediate frequencies to which the carriers of a QAM DTV signal and a VSB DTV signal can be frequency translated, when the carrier of a VSB DTV signal is higher in frequency than the carrier of a QAM DTV signal in the final IF signal, so the full sideband of the VSB DTV signal is lower in frequency than its vestigial sideband in the final IF signal, and

when the sample rate during digitization is constrained to $21.52 * 10^6$ samples per second.

FIGURE 13 is a block schematic diagram of portions of another type of DTV receiver that can embody the invention, which portions are not shown in FIGURE 1 and differ from those of FIGURE 2 in the way data sync recovery is provided for.

In the block schematic diagrams, clock or control signal connections are shown in dashed line, where it is desired to distinguish them from connections for the signals being controlled. To avoid overcomplexity in the block schematic diagrams, some shimming delays necessary in the digital circuitry are omitted, where a need for such shimming delay is normally taken into account by a circuit or system designer.

DETAILED DESCRIPTION

FIGURE 1 shows a tuner 5 comprising elements 11-21 that selects one of channels at different locations in the frequency band for DTV signals and performs plural frequency conversion of the selected channel to a final intermediate-frequency signal in a final intermediate-frequency band. FIGURE 1 shows a broadcast receiving antenna 6 arranged to capture the DTV signals for the tuner 5. Alternatively, the tuner 5 can be connected for receiving DTV signals from a narrowcast receiving antenna or from a cablecast transmission system.

More particularly, in the tuner 5 shown in FIGURE 1, a channel selector 10 designed for operation by a human being determines the frequency of first local oscillations that a frequency synthesizer 11, which functions as a first local oscillator, furnishes to a first mixer 12 for heterodyning with DTV signals received from the antenna 6 or an alternative source of such signals. The first mixer 12 upconverts the received signals in the selected channel to prescribed first intermediate frequencies (e. g., with 922.69 MHz carrier), and an LC filter 13 is used to reject the unwanted image frequencies that accompany the upconversion result supplied from the first mixer 12. The first intermediate-frequency signal resulting from the upconversion, supplied as the filter 13 response, is applied as the input signal to a first

intermediate-frequency amplifier 14, which supplies amplified first IF signal for driving a first surface-acoustic-wave (SAW) filter 15 or a filter constructed from ceramic resonators. The upconversion to the rather high-frequency first intermediate frequencies facilitates the SAW filter 15 having a large number of poles and zeroes.

5 The SAW filter 15 passband is designed to pass those frequencies obtained by converting frequencies extending from the lower limit frequency of the television channel up to about 300 kHz of the upper limit frequency of the television channel. Preferably the SAW filter 15 is designed to reject the frequency-modulated sound carrier of any co-channel interfering NTSC analog TV signal. Second local

10 oscillations from a second local oscillator 16 are supplied to a second mixer 17 for heterodyning with the response of the first SAW filter 15, to generate second intermediate frequencies (e. g., with 46.69 MHz carrier). A second SAW filter 18 is used for rejecting the unwanted image frequencies that accompany the downconversion result supplied from the second mixer 17. During the period of

15 transition from NTSC television transmissions to digital television transmissions, the second SAW filter 18 will usually include traps for sound and video carriers of adjacent-channel NTSC television transmissions. The second IF signal supplied as the response of the second SAW filter 18 is applied as input signal to a second intermediate-frequency amplifier 19, which generates an amplified second IF signal

20 response to its input signal. Oscillations from a third local oscillator 20 are heterodyned with the amplified second IF signal response in a third mixer 21. The plural-conversion tuner 5 as thusfar described resembles those previously proposed by others, except that the frequency of the oscillations from the third local oscillator 20 is chosen such that the third mixer 21 supplies a third intermediate-frequency signal

25 response.

This third IF signal response is the final intermediate-frequency output signal of the tuner 5, which is supplied to a subsequent analog-to-digital converter (ADC) 22 for digitization. This final IF signal occupies a frequency band 6 MHz wide, the lowest frequency of which is above zero frequency. The lowpass analog filtering of

30 the third mixer 21 response done in the ADC 22 as a preliminary step in

analog-to-digital conversion suppresses the image frequencies of the third intermediate frequencies, and the second SAW filter 18 has already restricted the bandwidth of the third intermediate-frequency signals presented to the ADC 22 to be digitized; so the ADC 22 functions as a bandpass analog-to-digital converter. The
5 sampling of the lowpass analog filter response in the ADC 22 as the next step in analog-to-digital conversion is done responsive to pulses in a first clock signal supplied from a sample clock generator 23.

The sample clock generator 23 preferably includes a crystal oscillator capable of frequency control over a relatively narrow range for generating cissoidal
10 oscillations at a multiple of symbol rate. A symmetrical clipper or limiter generates a square-wave response to these cissoidal oscillations to generate the first clock signal, which the ADC 22 uses to time the sampling of the final IF signal after filtering to limit bandwidth. The frequency of the cissoidal oscillations generated by the crystal oscillator in the sample clock generator 23 can be determined by an automatic
15 frequency and phase control (AFPC) signal developed in response to components of the received DTV signal that are subharmonics of symbol or baud rate, for example, as will be described in detail further on in this specification. The pulses in the first clock signal recur at a $21.52 * 10^6$ samples-per-second rate, twice the $10.76 * 10^6$ symbols-per-second symbol rate for VSB signals and four times the $5.38 * 10^6$
20 symbols-per-second symbol rate for QAM signals. At this $21.52 * 10^6$ samples-per-second clock rate, placing the final IF signal so its mid-frequency is above 5.38 MHz reduces the number of $21.52 * 10^6$ samples-per-second rate samples in the QAM carrier to less than four, which undesirably reduces the uniformity of synchrodyne response supplied for symbol decoding.

25 The ADC 22 supplies real digital responses of 10-bit or so resolution to the samples of the band-limited final IF signal, which digital responses are converted to complex digital samples by the circuitry 24. Various ways to construct the circuitry 24 are known. The imaginary digital samples at the QAM carrier frequency may be generated using a Hilbert transformation filter, for example, as described in U. S.

patent No. 5,479,449. If the frequency band 6 MHz wide occupied by the final IF signal has a lowest frequency of at least a megaHertz or so, it is possible to keep the number of taps in the Hilbert transformation filter reasonably small and thus keep the latency time of the filter reasonably short. Other ways to construct the circuitry 24 described in U. S. patent No. 5,548,617 rely on the differential delay between the responses of two infinite-impulse-response (IIR) filters being substantially equal to 90° phase shift at all frequencies. Still other ways to construct the circuitry 24 rely on the differential delay between the responses of two finite-impulse-response (FIR) filters being substantially equal to 90° phase shift at all frequencies.

10 In the FIGURE 1 receiver circuitry the complex digital samples of final IF signal supplied from the circuitry 24 are applied to circuitry 25 for synchrodyning the QAM signal to baseband. The circuitry 25 supplies a stream of real samples and a stream of imaginary samples in parallel to a symbol de-interleaver 26, to provide baseband description of the QAM modulating signal. The QAM synchrodyning circuitry 25 receives complex-number digital descriptions of two phasings of the QAM carrier, as translated to final intermediate frequency and in quadrature relationship with each other, from read-only memory 27. ROM 27, which comprises sine and cosine look-up tables for QAM carrier frequency, is addressed by a first address generator 28. The first address generator 28 includes an address counter (not explicitly shown in FIGURE 1) for counting the recurrent clock pulses in the first clock signal generated by the sample clock generator 23. The resulting address count is augmented by a symbol phase correction term generated by QAM de-rotator correction circuitry, thereby to generate the addressing for the ROM 27. The QAM synchrodyne circuitry 25, the first address generator 28, and the operation of each will be explained in greater detail further on in this specification.

In the FIGURE 1 receiver circuitry the complex digital samples of final IF signal supplied from the circuitry 24 are also applied to circuitry 30 for synchrodyning the VSB signal to baseband. The VSB synchrodyning circuitry 30 supplies streams of samples descriptive of real and imaginary components of the vestigial-sideband

modulating signal as synchrodyne to baseband. The VSB synchrodyne circuitry 30 receives complex-number digital descriptions of two phasings of the VSB carrier, as translated to final intermediate frequency and in quadrature relationship with each other, from read-only memory 31. ROM 31, which comprises sine and cosine look-up
5 tables for VSB carrier frequency, is addressed by a second address generator 32. The second address generator 32 includes an address counter (not explicitly shown in FIGURE 1) for counting the recurrent clock pulses in the first clock signal generated by the sample clock generator 23. In preferred embodiments of the invention this address counter is the same address counter used by the first address generator 28.
10 The resulting address count is augmented by a symbol phase correction term generated by symbol phase correction circuitry, thereby to generate the addressing for the ROM 31. The VSB synchrodyne circuitry 30, the second address generator 32, and the operation of each will be explained in greater detail further on in this specification.

15 A digital-signal multiplexer 33 functions as a synchrodyne result selector that selects as its response either a first or a second one of two complex digital input signals supplied thereto, the selection being controlled by a detector 34 for detecting the zero-frequency term of the real samples from the VSB synchrodyne circuitry 30. When the zero-frequency term has essentially zero energy, indicating the absence of
20 pilot carrier signal that accompanies a VSB signal, the multiplexer 33 selectively responds to its first complex digital input signal, which is the de-interleaved QAM synchrodyne-to-baseband result supplied from the de-interleaver 26. When the zero-frequency term has substantial energy, indicating the presence of pilot carrier signal that accompanies a VSB signal, the multiplexer 33 selectively responds to its
25 second complex digital input signal comprising the real and imaginary components of the baseband response of the VSB synchrodyne circuitry 30.

The response of the synchrodyne result selection multiplexer 33 is resampled in response to a second clock signal from the sample clock generator 23 in 2:1 decimation circuitry 35, to reduce the sample rate of complex baseband response

down to the 10.76 MHz VSB symbol rate, which is twice the 5.38 MHz QAM symbol rate. That is, the stream of real digital samples and the stream of imaginary digital samples are both decimated 2:1. The 2:1 decimation of the multiplexer 33 response prior to its application as input signal to an amplitude-and-group-delay equalizer 36
5 reduces the hardware requirements on the equalizer. Alternatively, rather than 2:1 decimation circuitry 35 being used after the synchrodyne result selection multiplexer 33, the baseband responses of the QAM synchrodyne circuitry 25 and of the VSB synchrodyne circuitry 30 can each be resampled in response to a second clock signal from the sample clock generator 23 to carry out 2:1 decimation before the
10 synchrodyne result selection multiplexer 33.

FIGURE 2 shows the amplitude-and-group-delay equalizer 36, which converts a baseband response with an amplitude-and-phase-versus-frequency characteristic that tends to cause inter-symbol error to an improved amplitude-versus-frequency characteristic that minimizes the likelihood of inter-symbol error. The
15 amplitude-and-group-delay equalizer 36 can be a suitable one of the monolithic ICs available off-the-shelf for use in equalizers. Such an IC includes a multiple-tap digital filter used for amplitude-and-group-delay equalization, the tap weights of which filter are programmable; circuitry for selectively accumulating a training signal and temporarily storing the accumulation results; and a microcomputer for calculating
20 updated tap weights of the multiple-tap digital filter used for amplitude-and-group-delay equalization.

When the DTV signal being received is of VSB type, training signal is contained in the initial data segment of each data field. The microcomputer is programmed for comparing the temporarily stored accumulation results with the ideal
25 training signal as known *a priori* and establishing a set of weighting coefficients for the multiple-tap digital filter used for amplitude-and-group-delay equalization. Thereafter, better to compensate for changing multipath conditions such as caused by overflying aircraft, weighting coefficients may be updated on a more frequent basis using decision-directed equalization techniques, such as those disclosed by the

inventors and Dr. Jian Yang in U. S. patent No. 5,648,987 issued 15 July 1997 and entitled **RAPID-UPDATE ADAPTIVE CHANNEL-EQUALIZATION FILTERING FOR DIGITAL RADIO RECEIVERS, SUCH AS HDTV RECEIVERS**. When the DTV signal being received is of QAM type, unless
5 provision is made for inclusion of a training signal, decision-directed equalization techniques have to be used if equalization is to be effected. The establishment of a satisfactory set of initial weighting coefficients takes more time than when a training signal is available. If the DTV receiver remains in place during periods of operation and non-operation, the time required to establish a satisfactory set of initial weighting
10 coefficients when a DTV channel is retuned can be reduced by if the last determined set of weighting coefficients for that DTV channel have been stored in memory.

Both the real and the imaginary responses of the amplitude-and-group-delay equalizer 36 are applied as input signal to two-dimensional symbol decoding circuitry 37, which performs the symbol decoding that recovers symbol-decoded digital data
15 streams from a QAM-origin signal. Presuming that the QAM-origin signal contains data synchronizing information corresponding to the data synchronizing information in the VSB-origin signal, one of these symbol-decoded digital data streams is a trellis-decoded digital data stream supplied for further data processing, and another of these symbol-decoded digital data streams is generated by data-slicing without
20 subsequent trellis decoding. Data synchronizing information is extracted from this latter symbol-decoded digital data stream and is employed for controlling the processing of the QAM-origin data by the receiver.

The real response of the amplitude-and-group-delay equalizer 36 is applied as input signal to one-dimensional symbol decoding circuitry 38, which performs the
25 symbol decoding that recovers symbol-decoded digital data streams from a VSB-origin signal. A VSB signal in accordance with the ATSC standard uses trellis coding of the data in all data segments except the initial data segment of each data field, which contains field synchronization code groups that are not subject to trellis coding. As in the prior art, one of the symbol-decoded digital data streams that the

symbol decoding circuitry 38 supplies, which is to be employed for further data processing is generated by trellis-decoding the results of data-slicing procedures, and optimal Viterbi decoding techniques are customarily employed. As in the prior art, another of the symbol-decoded digital data streams that the symbol decoding circuitry 5 38 supplies, which is to be employed for controlling data handling by the receiver responsive to synchronization information contained in the received VSB-origin signal, is generated using data-slicing procedures without subsequent trellis decoding. The symbol decoding circuitry 38 preferably departs from usual prior-art practice by utilizing data-slicing techniques similar to those described in allowed U. S. patent 10 application serial No. 08/746,520 filed 12 November 1996, entitled **DIGITAL TELEVISION RECEIVER WITH ADAPTIVE FILTER CIRCUITRY FOR SUPPRESSING NTSC CO-CHANNEL INTERFERENCE**, and incorporated herein by reference.

A digital-signal multiplexer 39 functions as a data source selector that selects 15 as its response either a first or a second one of two digital input signals thereto, the selection being controlled by the detector 34 for detecting the zero-frequency term of the real samples from the VSB synchrodyne circuitry 30. When the zero-frequency term has essentially zero energy, indicating the absence of pilot carrier signal that accompanies a VSB signal, the multiplexer 39 selectively responds to its first digital 20 input signal, selecting as the source of its digital data output the two-dimensional symbol decoding circuitry 37 that decodes the symbols received in the QAM signal. When the zero-frequency term has substantial energy, indicating the presence of pilot carrier signal that accompanies a VSB signal, the multiplexer 39 selectively responds to its second digital input signal, selecting as the source of its digital data output the 25 one-dimensional symbol decoding circuitry 38 that decodes the symbols received in the VSB signal.

The data selected by the data source selection multiplexer 39 are applied to a data de-interleaver 40 as its input signal, and the de-interleaved data supplied from the data de-interleaver 40 are applied to a Reed-Solomon decoder 41. The data

de-interleaver 40 is often constructed within its own monolithic IC and is made so as to respond to the output indications from the pilot carrier presence detector 34 to select the de-interleaving algorithm suitable to the DTV signal currently being received, whether it be of QAM or VSB type; this is a mere matter of design. The

5 Reed-Solomon decoder 41 is often constructed within its own monolithic IC and is made so as to respond to the output indications from the pilot carrier presence detector 34 to select the appropriate Reed-Solomon decoding algorithm for the DTV signal currently being received, whether it be of QAM or VSB type; this also is a mere matter of design. Error-corrected data are supplied from the Reed-Solomon decoder

10 41 to a data de-randomizer 42, which responds to these data for regenerating a signal randomized prior to transmission to the DTV receiver, which regenerated signal comprises packets of data for a packet sorter 43. The data de-randomizer 42 is made so as to respond to the output indications from the pilot carrier presence detector 34 to select the appropriate data de-randomizing algorithm for the DTV signal currently

15 being received, whether it be of QAM or VSB type; the selection of these algorithms is a mere matter of design, too.

First data synchronization recovery circuitry 44 recovers the data synchronizing information included in the data output of the two-dimensional symbol decoding circuitry decoder 37, and second data synchronization recovery circuitry 45

20 recovers the data synchronizing information included in the data output of the one-dimensional symbol decoding circuitry 38. A data sync selector 46 selects between the data synchronizing information as provided by the data sync recovery circuitry 44 and as provided by the data sync recovery circuitry 45, the selection being controlled by the detector 34 for detecting the zero-frequency term of the real samples

25 from the VSB synchrodyne circuitry 30. When the zero-frequency term has essentially zero energy, indicating the absence of pilot carrier signal that accompanies a VSB signal, the data sync selector 46 selects for its output signals the data synchronizing information provided by the data sync recovery circuitry 44. When the zero-frequency term has substantial energy, indicating the presence of pilot carrier

30 signal that accompanies a VSB signal, the data sync selector 46 selects for its output

signals the data synchronizing information provided by the data sync recovery circuitry 45.

When the data sync selector 46 selects for its output signals the data synchronizing information provided by the data sync recovery circuitry 45, the initial
5 data lines of each data field are selected for application to the amplitude-and-group-delay equalizer 36 as training signal. The occurrences of the 511-sample PN sequence can be detected within the data sync recovery circuitry 45 to provide data-field indexing information to the data sync selector 46. Alternatively, the occurrences of two or three consecutive 63-sample PN sequences are detected
10 within the data sync recovery circuitry 45 to provide data-field indexing information to the data sync selector 46.

The standards for a QAM DTV signal are not as well defined at this time as the standards for a VSB DTV signal. A 32-state QAM signal provides sufficient capacity for a single HDTV signal, without having to resort to compression
15 techniques outside MPEG standards, but commonly some compression techniques outside MPEG standards are employed to encode the single HDTV signal as a 16-state QAM signal. Typically, the occurrence of a prescribed 24-bit word is detected by the data sync recovery circuitry 44 to generate data-field indexing information for application to the data sync selector 46. A multiplexer within the data
20 sync selector 46 selects between the data-field indexing information respectively supplied by the data sync recovery circuitry 44 and the data sync recovery circuitry 45; the data-field indexing information thus selected is supplied to the data de-interleaver 40, the Reed-Solomon decoder 41, and the data de-randomizer 42. At the time this
25 specification is written there is no training signal included in the QAM DTV signal. Accordingly, in response to the VSB pilot carrier presence detector 34 indicating the absence of pilot carrier, the amplitude-and-group-delay equalizer 36 is conditioned to use decision-directed equalization techniques that do not depend on a training signal; and the VSB training signal selected by the data sync recovery circuitry 45 is wired

through the data sync selector 46 without need for a multiplexer. Also, there is no data line synchronization signal for QAM DTV transmission, at least not a data line synchronization signal selected as a standard. The data sync recovery circuitry 44 includes counting circuitry for counting the samples in each data field to generate
5 intra-data-field synchronizing information. This intra-data-field synchronizing information and the intra-data-field synchronizing information (such as data line count) generated by the data sync recovery circuitry 45 are selected between by appropriate multiplexers in the data sync selector 46, for application to the data de-interleaver 40, the Reed-Solomon decoder 41, and the data de-randomizer 42, as
10 required.

Figure 2 of the U. S. patent No. 5,506,636 drawing shows a variant of the symbol decoding circuitry 37 in which variant the trellis decoding results and the symbol-decoded data synchronization are time-division-multiplexed onto a single bus for application to the data source selector 39 and to the first data sync recovery
15 circuitry 44. Figure 2 of the U. S. patent No. 5,506,636 drawing also shows a variant of the symbol decoding circuitry 38 in which variant the trellis decoding results and the symbol-decoded data synchronization are time-division-multiplexed onto a single bus for application to the data source selector 39 and to the second data sync recovery circuitry 45. As in the embodiment shown in FIGURE 2 of the drawing for this
20 specification, the first data sync recovery circuitry 44 and the second data sync recovery circuitry 45 perform data synchronization by match filtering of symbol decoding results. If the initial data segment of each data field per the ATSC specification for VSB broadcasting is simply recoded using the symbol codes for QAM cablecasting, data synchronization can be performed after symbol decoding the
25 QAM signal by looking for symbol-decoded PN sequence information. Data synchronization is shown in FIGURE 2 as being performed after symbol decoding the VSB signal; this is done by looking for symbol-decoded PN sequence information. If the initial data segment of each data field per the ATSC specification for VSB broadcasting is simply recoded using the symbol codes for QAM cablecasting, then,
30 in a modification of the FIGURE 2 DTV receiver circuitry, data synchronization can

be performed after symbol decoding using the same apparatus during both VSB signal reception and during QAM signal reception.

Data synchronization during VSB signal reception can alternatively be accomplished before symbol decoding, using match filters that generate spike
5 responses to the PN sequences in the decimator 35 response or in the equalizer 36 response. The filters that generate spike responses to synchronization code sequences are preferably supplied input signals at the decimated sample rate, rather than input signals being the undecimated responses of synchrodyne circuits 29 and 30, in order to reduce the number of samples in the respective kernel of each match filter. The
10 filters that generate spike responses to synchronization code sequences are preferably connected to receive the equalizer 36 response to reduce the effect that multi-path reception has on data synchronization.

FIGURE 13 shows a modification of the FIGURE 2 portions of the DTV receiver in which the data sync recovery circuitry 45 for recovering data
15 synchronization from symbol decoding results is replaced by second data sync recovery circuitry 450 employing match filters for recovering data synchronization from the equalizer 36 response. The initial data segment in each data field can be detected using a match filter for one of the PN sequences in those initial data segments, a match filter for the 511-sample PN sequence being preferred because of
20 the higher energy of its auto-correlation response providing better selectivity than the auto-correlation response of a match filter for the 63-sample PN sequence. The match filter for the PN sequence can serve dual purpose, being used to identify the positions of ghosts during the calculation of filter coefficients for the equalizer 36. U. S. patent No. 5,594,506 issued 14 January 1997 to J. Yang and entitled LINE SYNC
25 DETECTOR FOR DIGITAL TELEVISION RECEIVER describes a preferred form for detecting the 4-symbol segment sync code group located at the beginning of each data segment.

The packet sorter 43 sorts packets of data for different applications, responsive to header codes in the successive packets of data. Packets of data descriptive of the

audio portions of the DTV program are applied by the packet sorter 43 to a digital sound decoder 47. The digital sound decoder 47 supplies left-channel and right-channel stereophonic sound signals to a plural-channel audio amplifier 48 that drives the plurality of loudspeakers 49, 50. Packets of data descriptive of the video portions of the DTV program are applied by the packet sorter 43 to an MPEG decoder 51, such as of MPEG-2 type. The MPEG decoder 51 supplies horizontal (H) and vertical (V) synchronizing signals to kinescope deflection circuitry 52 that provides for the raster scanning of the viewing screen of a kinescope 53. The MPEG decoder 51 also supplies signals to the kinescope driver amplifiers 54 for applying amplified red (R), green (G) and blue (B) drive signals to the kinescope 53. In variations of the DTV receiver shown in FIGURES 1 and 2, a different display device may be used instead of or in addition to the kinescope 53, and the sound recovery system may be different, consisting of but a single audio channel, or being more elaborate than a simple stereophonic reproduction system.

Referring back to FIGURE 1, in order that ROMs 27 and 31 can be used to generate digital complex-number descriptions of the QAM and VSB signal carriers as translated to respective final intermediate frequencies, in response to addressing generated by counting first clock signals, provision must be made to lock the one those final intermediate frequencies that is the carrier of the currently received DTV signal to a submultiple of a multiple of the first clock signal frequency. That is, those final intermediate frequencies must be in whole number ratios with the first clock signal frequency. An automatic phase and frequency control (AFPC) signal is developed in the digital circuitry following the analog-to-digital converter 22 and is used to control the frequency and phase of one of the local oscillators 11, 16 and 20 in the tuner. Preferably, in order that alignment of the second IF signal with the second SAW filter 18 can be readily assured, a fixed-frequency third local oscillator 20 is used, and the frequency and phase of the oscillations the second local oscillator 16 provides are controlled. The second SAW filter 18 usually includes traps for adjacent-channel signal components, in which case proper alignment of the second IF signal between these traps is important for preserving its integrity. The symbol

clocking is made to exhibit a high degree of frequency stability. By locking the carrier of the final intermediate-frequency (IF) signal in frequency and phase to a submultiple of a multiple of the symbol clock frequency, the AFPC for correcting frequency and phase error in the carrier as translated to a final intermediate frequency
5 invariably operates to correct dynamic symbol phase error as well, eliminating the need for a separate phase tracker to correct dynamic symbol phase error.

FIGURE 1 denominates a digital multiplexer 55 as "AFPC selector". The multiplexer 55 responds to the pilot carrier presence detector 34 indicating that a pilot carrier is included in the currently received DTV signal for selecting, as an input
10 signal for a digital lowpass filter 56, the imaginary output signal of the baseband response of the VSB synchrodyne circuitry 30. The response of lowpass filter 56 is a digital AFPC signal supplied as input signal to a digital-to-analog converter (DAC)
15 57. The output signal from the DAC 57 is an analog AFPC signal, which is subjected to further lowpass filtering in an analog lowpass filter 58, the response of which filter 58 is used for controlling the frequency and phase of the oscillations that the second local oscillator 16 provides. Analog lowpass filtering is advantageous to use for realizing long-time-constant lowpass filtering because there is reduced need for active devices as compared to digital lowpass filtering. Since the shunt capacitor of a resistance-capacitance lowpass filter section can be at the interface between a tuner 5
20 IC and the IC containing the digital synchrodyning circuitry, the analog lowpass filtering can be done without any cost in IC pin-out. Doing some digital lowpass filtering is advantageous, however, since the digital lowpass filter response can be subsampled to the DAC 57; the reduced speed requirements on the digital-to-analog conversion reduces the cost of the DAC 57. This procedure is similar to that used in
25 the AGC circuitry described at the end of this specification with reference to FIGURE 12 of the drawing, and the third clock signal developed for the AGC circuitry can be used by the DAC 57 and can be used to reset an accumulator the digital lowpass filter 56 includes for averaging samples of filter input signal.

The multiplexer 55 responds to the pilot carrier presence detector 34 indicating that a pilot carrier is not included in the currently received DTV signal for selecting the input signal for the digital lowpass filter 56 from the circuitry for processing a QAM DTV signal. FIGURE 1 shows the product output signal of a digital multiplier 29 being provided for such selection. The digital multiplier 29 multiplies together the real and imaginary output signals of the QAM synchrodyne circuitry 25 to generate an unfiltered digital AFPC signal. The generation of the unfiltered digital AFPC signal is very similar to that in the well-known Costas loop. In the Costas loop the AFPC signal is used to control the frequency and phase of the digital local oscillations used for synchrodyning received signals to baseband. The FIGURE 1 arrangement departs from this procedure, the AFPC signal being used instead to control the frequency and phase of the analog oscillations generated by the second local oscillator 16. This regulates the frequency and phase of the final IF signal supplied to the ADC 22 for digitization and for subsequent synchrodyning to baseband in the digital regime. As is the case with the Costas loop, the multiplier 29 is preferably of especial design in which the real signal is converted to a ternary signal for multiplying the imaginary signal; this simplifies the digital multiplier and improves the pull-in characteristics of the AFPC loop.

The second intermediate-frequency amplifier 19, the third local oscillator 20 (except for its outboard crystal and other frequency selection components), and the third mixer 21 are advantageously constructed within the confines of a monolithic IC; since the output signal of the third mixer 21 is at a different frequency than the input signal to the second IF amplifier 19, the second IF amplifier 19 can have high gain without attendant high risk of unwanted regeneration. The first IF amplifier 14, the second local oscillator 16 (except for its outboard crystal and other frequency selection components) and the second mixer 17 can be constructed within the confines of the same IC, or they may be constructed otherwise – e.g., within other integrated circuitry. The analog-to-digital converter (ADC), as customary, will be a flash type with at least ten bits resolution and is preferably constructed within the confines of a different monolithic IC than the IF amplifiers. The analog lowpass filter at the input

of the converter isolates the sampling circuitry, with its associated switching transients, from the IC in which the high-gain second IF amplifier 19 is located (and in some cases, in which the first IF amplifier 14 is also located). This reduces the likelihood of unwanted regeneration in the tuner 5. Considerable die area is required
5 for the resistance ladder used in establishing the quantizing levels and for the large number of analog comparators involved in an ADC of flash type, so often such an ADC does not share a monolithic IC with other elements anyway.

The elements 23 - 35, 55 and 56 are advantageously constructed within the confines of a single monolithic integrated circuit (IC), to reduce the number of wiring
10 connections made outside the confines of a monolithic IC. The synchrodyning circuits 25 and 30 both receive input signals from the real-to-complex sample converter 24, and portions of their respective address generators 28 and 32 can usually be provided by circuitry shared in common. It is advantageous that this single monolithic IC and the circuitry that follows this IC include all the circuitry for
15 automatically selecting the appropriate mode of reception for the DTV transmission currently being received. Such practice avoids the need for operating the third local oscillator at two markedly different frequencies, depending on whether a DTV signal is of QAM type or is of VSB type. Operation of the third local oscillator at two markedly different frequencies is normally associated with the use of two different
20 crystals for setting those frequencies. Operating the third local oscillator at essentially the same frequency, no matter whether the DTV signal is of QAM type or is of VSB type, saves the cost of the extra crystal and of the electronic switching circuitry involved with the use of two crystals. Furthermore, the reliability of the tuner 5 is improved by the reduction in the amount of circuitry located outside the monolithic
25 integrated circuitry.

If the ADC is not constructed within an IC, all or substantially all its own, it is advantageous to include it in the IC that contains the circuitry for synchrodyning VSB DTV signals and the circuitry for synchrodyning QAM DTV signals to baseband, since the signals for clocking the sampling of the final IF signal by the ADC are to be

generated within that IC. Furthermore, the analog lowpass filter at the input of the converter still isolates the sampling circuitry, with its associated switching transients, from the IC(s) in which high-gain IF amplification is done.

FIGURE 3 shows in more detail the digital circuitry 25 for synchrodyning
5 QAM DTV signals to baseband. The QAM synchrodyning circuitry 25 includes the
QAM in-phase synchronous detector 250 for generating the real portion of its output
signal and the QAM quadrature-phase synchronous detector 255 for generating the
imaginary portion of its output signal. The QAM synchrodyning circuitry 25 includes
a digital adder 256, a digital subtractor 257, and respective first, second, third and
10 fourth digital multipliers 251-254. The QAM in-phase synchronous detector 250
includes the multiplier 251, the multiplier 252, and the adder 256 for adding the
product output signals of the multipliers 251 and 252 to generate the real portion of
the output signal of the QAM synchrodyning circuitry 25. The first digital multiplier
251 multiplies the real digital samples of final IF signal supplied from the
15 real-to-complex-sample converter 24 by digital samples descriptive of the cosine of
the QAM carrier that are read from the look-up table 271 in the ROM 27, and the
second digital multiplier 252 multiplies the imaginary digital samples of final IF
signal supplied from the real-to-complex-sample converter 24 by digital samples
descriptive of the sine of the QAM carrier that are read from the look-up table 272 in
20 the ROM 27. The QAM quadrature-phase synchronous detector 255 includes the
multiplier 253, the multiplier 254, and the subtractor 257 for subtracting the product
output signal of the multiplier 253 from the product output signal of the multiplier 254
to generate the imaginary portion of the output signal of the QAM synchrodyning
circuitry 25. The third digital multiplier 253 multiplies the real digital samples of
25 final IF signal supplied from the real-to-complex-sample converter 24 by digital
samples descriptive of the sine of the QAM carrier that are read from the look-up table
272 in the ROM 27, and the fourth digital multiplier 254 multiplies the imaginary
digital samples of final IF signal supplied from the real-to-complex-sample converter
24 by digital samples descriptive of the cosine of the QAM carrier that are read from
30 the look-up table 271 in the ROM 27.

FIGURE 3 also shows in more detail the digital circuitry 30 for synchrodyning VSB DTV signals to baseband. The VSB synchrodyning circuitry 30 includes the VSB in-phase synchronous detector 300 for generating the real portion of its output signal and the VSB quadrature-phase synchronous detector 305 for generating the imaginary portion of its output signal. The VSB synchrodyning circuitry 30 includes a digital adder 306, a digital subtractor 307, and respective first, second, third and fourth digital multipliers 301-304. The VSB in-phase synchronous detector 300 includes the multiplier 301, the multiplier 302, and the adder 306 for adding the product output signals of the multipliers 301 and 302 to generate the real portion of the output signal of the VSB synchrodyning circuitry 30. The first digital multiplier 301 multiplies the real digital samples of final IF signal supplied from the real-to-complex-sample converter 24 by digital samples descriptive of the cosine of the VSB carrier that are read from the look-up table 311 in the ROM 31, and the second digital multiplier 302 multiplies the imaginary digital samples of final IF signal supplied from the real-to-complex-sample converter 24 by digital samples descriptive of the sine of the VSB carrier that are read from the look-up table 312 in the ROM 31. The VSB quadrature-phase synchronous detector 305 includes the multiplier 303, the multiplier 304, and the subtractor 307 for subtracting the product output signal of the multiplier 303 from the product output signal of the multiplier 304 to generate the imaginary portion of the output signal of the VSB synchrodyning circuitry 30. The third digital multiplier 303 multiplies the real digital samples of final IF signal supplied from the real-to-complex-sample converter 24 by digital samples descriptive of the sine of the VSB carrier that are read from the look-up table 312 in the ROM 31, and the fourth digital multiplier 304 multiplies the imaginary digital samples of final IF signal supplied from the real-to-complex-sample converter 24 by digital samples descriptive of the cosine of the VSB carrier that are read from the look-up table 311 in the ROM 31.

FIGURE 4 shows in detail a representative construction of the sample clock generator 23. This construction includes a voltage-controlled oscillator 230 that generates cissoidal oscillations nominally of 21.52 MHz frequency. The oscillator

230 is a controlled oscillator, the frequency and phase of its oscillations being controlled by an automatic frequency and phase control (AFPC) signal voltage. This AFPC signal voltage is generated by an automatic frequency and phase control (AFPC) detector 231, which compares frequency-divided response to the oscillations of the oscillator 230 with a 10.76 MHz reference carrier supplied from a digital-to-analog converter (DAC) 232. Preferably, oscillator 230 is of a type using a crystal for stabilizing the natural frequency and phase of its oscillations. A symmetrical clipper or limiter 233 generates an essentially squarewave response to these cissoidal oscillations, which is used as the first clock signal for timing the sampling of the final IF signal in the ADC 22. A frequency-divider flip-flop 234 responds to transitions of the first clock signal in a prescribed sense for generating another square wave with a fundamental frequency of 10.76 MHz, half the frequency of the oscillations of the oscillator 230. This frequency-divided response to the oscillations of the oscillator 230 is supplied to the AFPC detector 231 for comparison with the 10.76 MHz reference carrier supplied from the DAC 232. The frequency-divider flip-flop 234 also supplies squarewave output signal with a fundamental frequency of 10.76 MHz to an AND circuit 235 to be ANDed with the first clock signal for generating a second clock signal used by the 2:1 decimator 35 shown in FIGURE 1.

The 21.52 MHz reference carrier supplied from the digital-to-analog converter 232 is generated by extracting a component of the received DTV signal as synchrodynded to baseband, which component is of a frequency that is a subharmonic of the symbol frequency (or baud frequency), and multiplying that subharmonic of the symbol frequency by an appropriate factor in frequency multiplier circuitry. As evidenced by the article "Understanding Timing Recovery and Jitter in Digital Transmission Systems – Part 1" by Kenneth J. Bures published in the October 1992 issue of *RF Design*, there was knowledge in the prior art that it is possible in the analog regime to recover symbol timing information from certain types of symbol code in which the baud frequency is absent, by subjecting the symbol code to narrow bandpass filtering centered on a subharmonic of the baud frequency followed by

squaring or other non-linear procedure that will generate harmonics from which the baud frequency may be extracted by frequency-selective filtering. The narrow bandpass filters used for lower symbol code rates include LC filters and phase-locked loops (PLLs), while SAW filters are preferred for higher symbol code rates. What is
5 unusual about the symbol recovery procedure in the sample clock generator 23 shown in FIGURES 4 and 5 is that this method for recovering symbol timing information that is generally known is modified for use in the digital regime, using a finite-impulse-response digital bandpass filter having its elements clocked by the sample clock generator itself for selecting a prescribed submultiple of the symbol frequency
10 in the digitized symbol codestream. Prospectively considered there was no assurance that this modified method would in fact work, since the effects of the digital sampling process are difficult to evaluate, particularly when the sampling rate is itself subject to control by the result of the modified method.

The modified method does work, however, as long as the frequencies used for
15 generating AFPC error signal fall within the passbands of bandpass FIR digital filters which center on submultiples of the VCO 230 oscillation frequency, so that the AFPC loop can pull the VCO 230 into frequency and phase lock. In fact, the modified method is advantageous in that the bandpass FIR digital filters perform as tracking filters, being clocked by the sample clock generator. After frequency and phase lock
20 of the VCO 230, there are no phase shift effects caused by the symbol rate subharmonics and harmonics not falling exactly at the center frequencies of the bandpass filters. The modified method will now be specifically described, first presuming the received DTV signal is a VSB signal with a 10.76 MHz symbol frequency, and then presuming the received DTV signal is a QAM signal with a 5.38
25 MHz symbol frequency.

A digital multiplexer 236 responds to the pilot carrier presence detector 34 detecting pilot carrier accompanying the received DTV signal, which is indicative that the received DTV signal is a VSB signal, to select the real samples of this signal supplied from a VSB in-phase synchronous detector 300 for application to a bandpass

FIR digital filter 237 that provides a selective response centered at 5.38 MHz, which selects the first subharmonic of symbol frequency from the VSB signal. The filter 237 response is squared by a squaring circuit 238, which generates harmonics of the filter 237 response including a strong 10.76 MHz component as second harmonic of 5.38 MHz. A bandpass FIR digital filter 239 that provides a selective response centered at 10.76 MHz selects this second harmonic for application to the DAC 232 as its digital input signal descriptive of its 10.76 MHz reference carrier analog output signal.

The digital multiplexer 236 responds to the pilot carrier presence detector 34 not detecting pilot carrier accompanying the received DTV signal, which is indicative that the received DTV signal is a QAM signal, to select the output signal of a squaring circuit 23A for application to the bandpass filter 237 that provides a selective response centered at 5.38 MHz. A bandpass FIR digital filter 23B that provides a selective response centered at 2.69 MHz for selecting the 2.69 MHz first subharmonic of the symbol frequency of a baseband QAM signal supplies input signal to the squaring circuit 23A, which generates harmonics of the filter 23B response including a strong 5.38 MHz component. This baseband QAM signal can be supplied either from the QAM in-phase synchronous detector 250, as shown in FIGURE 4, or from the QAM quadrature-phase synchronous detector 255.

The squaring circuit 238 is shown in FIGURE 4 as a digital multiplier receiving the filter 237 response both as multiplier and multiplicand; and the squaring circuit 23A is shown as a digital multiplier receiving the filter 23B response both as multiplier and multiplicand. Each of the squaring circuits 238 and 23A can be constructed from logic gates as a digital multiplier, but for the sake of speedier operation is better provided by a ROM storing a look-up table of squares. An absolute-value circuit can be used as a substitute for the squaring circuit in generating harmonics of the response of a preceding filter, but produces weaker second harmonics and so is not preferred.

FIGURE 4 also shows in more detail a representative construction of the first address generator 28, which supplies addresses to a cosine look-up table portion 271 and a sine look-up table portion 272 of the ROM 27 that provides complex-number digital descriptions of two phasings of the QAM carrier, as translated to a final intermediate frequency and in quadrature relationship with each other. Transitions of the first clock signal are counted by a first address counter 281 in the first address generator 28 to generate a basic first address signal. This basic first address signal is applied as a first summand to a digital adder 282. A first address correction signal, which is applied to the adder 282 as a second summand, adds to the basic first address signal in the adder 282 for generating as a sum output signal a corrected first address signal for addressing both the cosine look-up table portion 271 and the sine look-up table portion 272 of the ROM 27. A symbol-clock-rotation detector 283 responds to the sequence of real samples of QAM signal as synchrodyne to baseband by the QAM in-phase synchronous detector 250 and to the sequence of imaginary samples of QAM signal as synchrodyne to baseband by the QAM quadrature-phase synchronous detector 255. The symbol-clock-rotation detector 283 detects the misphasing between symbol clocking done at the receiver in accordance with the first clock signal and symbol clocking done at the transmitter, as evidenced in the received QAM signal heterodyne to a final intermediate frequency that is a submultiple of its symbol frequency. Several types of symbol-clock-rotation detector 283 are described and background literature describing certain of them are catalogued in U. S. patent No. 5,115,454 issued 19 May 1992 to A. D. Kucar, entitled **METHOD AND APPARATUS FOR CARRIER SYNCHRONIZATION AND DATA DETECTION**, and incorporated herein by reference. A digital lowpass filter 284 averages over many samples (e. g., several million) the misphasing of the symbol clocking done at the receiver as detected by the symbol-clock-rotation detector 283 to generate the first address correction signal supplied to the adder 282 to correct the basic first address. Averaging over so many samples can be done by procedures which accumulate lesser numbers of samples and dump them forward at a reduced

sample rate for further accumulation, accumulation and subsampling being repeated a few times with progressively lower subsampling rates.

FIGURE 4 also shows in more detail a representative construction of the second address generator 32, which supplies addresses to a cosine look-up table portion 311 and a sine look-up table portion 312 of the ROM 31 that provides
5 complex-number digital descriptions of two phasings of the VSB carrier, as translated to a final intermediate frequency and in quadrature relationship with each other. Transitions of the first clock signal are counted by a second address counter 321 in the second address generator 32 to generate a basic second address signal. This basic
10 second address signal is applied as a first summand to a digital adder 322. A second address correction signal, which is applied to the adder 322 as a second summand, adds to the basic second address signal in the adder 322 for generating as a sum output signal a corrected second address signal for addressing both the cosine look-up table portion 311 and the sine look-up table portion 312 of the ROM 31.

15 FIGURE 4 shows a clocked digital delay line 323 for delaying the samples from the in-phase synchronous detector 300 by a prescribed number of sample periods prior to their being applied as input signal to a quantizer 324, which supplies the quantization level most closely approximated by the sample currently received by the quantizer 324 as input signal. The quantization levels can be inferred from the energy
20 of the pilot carrier accompanying the VSB signal or can be inferred from the result of envelope detection of the VSB signal. The closest quantization level selected by the quantizer 324 as its output signal has the corresponding quantizer 324 input signal subtracted therefrom by a digital adder/subtractor 325, which is operated as a clocked element by including a clocked latch at its output. The difference output signal from
25 the adder/ subtractor 325 describes the departure of the symbol levels actually recovered from those that should be recovered, but whether the polarity of the departure is attributable to symbol misphasing being leading or lagging remains to be resolved.

The samples from the in-phase synchronous detector 300 applied as input signal to the clocked digital delay line 323 are applied without delay as input signal to a mean-square-error gradient detection filter 326. The filter 326 is a finite-impulse-response (FIR) digital filter having a $(-1/2)$, 1, 0, (-1) , $(+1/2)$ kernel, the operation of which is clocked by the first sampling clock. The prescribed number of sample periods of delay provided by the clocked digital delay line 323 is such that filter 326 response is in temporal alignment with the difference signal from the adder/subtractor 325. A digital multiplier 327 multiplies the difference signal from the adder/subtractor 325 with the filter 326 response to resolve this issue. The sign bit and the next most significant bit of the two's complement filter 326 response suffice for the multiplication, which permits simplification of the digital multiplier 327 structure. The samples of the product signal from the digital multiplier 327 are indications of the misphasing of the symbol clocking done at the receiver that are averaged over many samples (e. g., several million) by a digital lowpass filter 328 for generating the second address correction signal supplied to the adder 322 to correct the basic second address.

The symbol synchronization techniques used in the second address generator 32 shown FIGURE 4 are of the same general type as S. U. H. Qureshi describes for use with pulse amplitude modulation (PAM) signals in his paper "Timing Recovery for Equalized Partial-Response Systems, *IEEE Transactions on Communications*, Dec. 1976, pp. 1326-1330. These symbol synchronization techniques as used in connection with symbol synchronization for VSB signals are specifically described by the inventors in their earlier-filed applications referenced earlier in this specification. In preferred designs of the general type of second address generator 32 shown in FIGURES 4 and 5, the clocked digital delay line 323 does not exist as a separate element; instead, an input signal to the quantizer 324 with the requisite number of sample periods of delay for the difference signal from the adder/subtractor 325 being temporally aligned with the filter 326 response is taken from the tapped digital delay line included in the filter 326 for supplying differentially delayed samples to be

weighted by the $(-1/2)$, 1, 0, (-1) , $(+1/2)$ kernel before being summed to generate the filter 326 response.

The carrier of a QAM DTV signal and the carrier of a VSB DTV signal are translated to respective final intermediate frequencies that are separated 2.69 MHz
5 from each other, since the carrier of the QAM DTV signal is at the center of a 6-MHz-wide TV channel, but the carrier of the VSB DTV signal is only 310 kHz above the lowest frequency of a 6-MHz-wide TV channel. The frequencies of the local oscillators 11, 16 and 20 in the tuner 5 of FIGURE 1 can be chosen so that the intermediate frequency to which the carrier of a VSB DTV signal is translated is
10 higher than that to which the carrier of a QAM DTV signal is translated, with the vestigial and full sidebands of the VSB DTV signal being respectively above and below its carrier. Alternatively, the frequencies of the local oscillators 11, 16 and 20 can be chosen so that the intermediate frequency to which the carrier of a VSB DTV signal is translated is lower than that to which the carrier of a QAM DTV signal is
15 translated, with the vestigial and full sidebands of the VSB DTV signal being respectively below and above its carrier.

Preferably the lowest frequency of the final IF signal is above 1 MHz, to keep the ratio of the highest frequency of the final IF signal thereto substantially below 8:1 and thereby ease the filtering requirements for the real-to-complex-sample converter
20 24. To satisfy this preference in regard to the QAM signal alone, the lowest carrier frequency for the QAM carrier in the final IF signal is 3.69 MHz. To satisfy this preference in regard to the VSB signal alone, the lowest the carrier frequency for the VSB carrier in the final IF signal could be is 1.31 MHz, presuming its full sideband to be above its vestigial sideband in frequency, or 6.38 MHz, presuming its full
25 sideband to be below its vestigial sideband in frequency. Presuming the full sideband of the VSB signal to be above its vestigial sideband in frequency, since the carrier frequency of the VSB carrier must be at least 1.31 MHz, the carrier frequency of the QAM carrier must be at least 4.00 MHz. Presuming the full sideband of the VSB signal to be below its vestigial sideband in frequency, since the carrier frequency of

the VSB carrier must be at least 6.38 MHz, the carrier frequency of the QAM carrier must still be at least 3.69 MHz.

If the sample rate in the ADC 22 is established by the first clock signal from the sample clock generator 23 to be 21.52×10^6 samples per second, preferably the
5 intermediate frequency to which the carrier of a QAM DTV signal is translated is not higher than 5.38 MHz, so that it can be sampled at least four times per cycle. Presuming the full sideband of the VSB signal to be above its vestigial sideband in frequency, this preference constrains the lowest frequency in the final IF signal to being no higher than 2.38 MHz and the carrier of the VSB signal being no higher than
10 2.69 MHz. FIGURE 11 illustrates how, for these presumed conditions, the VSB carrier is constrained to the band 1.31 - 2.69 MHz, and the QAM carrier is constrained to the band 4.00 - 5.38 MHz.

Presuming the full sideband of the VSB signal to be below its vestigial sideband in frequency, the QAM carrier is constrained to the band 3.69 - 5.38 MHz.
15 Accordingly, the carrier of the VSB signal is constrained to the band 6.38 - 8.07 MHz in order that the 2.69 MHz offset between carriers is maintained. FIGURE 12 illustrates the case where the QAM carrier is constrained to the band 3.69 - 5.38 MHz and the VSB carrier is constrained to the band 6.38 - 8.07 MHz.

The final intermediate frequency to which the QAM carrier is translated must
20 be a submultiple of a multiple of the 21.52 MHz sampling rate in order that this carrier can be described on a continuous basis relying on a sine-cosine look-up table in the ROM 27. The final intermediate frequency to which the VSB carrier is translated must be a submultiple of a multiple of the 21.52×10^6 samples-per-second sampling rate in order that this carrier can be described on a
25 continuous basis relying on a sine-cosine look-up table in the ROM 31. The final intermediate frequency (m/n) times the 21.52 MHz sampling rate, to which the carrier is translated, preferably has a small value of n, to keep the number of values in the sine-cosine look-up tables stored in ROM reasonably small. (Note that the variables m

and n referred to here have no relationship to the variables M and N referred to in the SUMMARY OF INVENTION.)

One can search for respective intermediate frequencies to which the carrier of a QAM DTV signal and the carrier of a VSB DTV signal are to be translated, which
5 frequencies meet the criteria set forth above, by following procedure taught in U. S. patent No. 5,506,636. A table of subharmonics of successive harmonics of the 10.76 MHz VSB symbol rate, which the sampling clock rate is harmonically related to, is constructed for the frequency ranges of interest. Then pairs of subharmonics of the same harmonic which exhibit the desired 2.69 MHz difference in frequency between
10 them are considered with regard to their relative advantages as carriers.

The third and seventh subharmonics of 21.52 MHz at 5.38 MHz and at 2.39 MHz exhibit substantially the desired 2.69 MHz offset and are appropriate for use as QAM carrier and a VSB carrier with its full sideband above its vestigial sideband in frequency. The 2.69 MHz offset between these subharmonics is one-quarter the
15 symbol rate of 10,762,237.762 samples per second, or 2,690,559.4 Hz, rather than the 2,690,122.4 Hz offset between the QAM and VSB carriers required to offset the VSB carrier from a co-channel interfering NTSC video carrier by 59.75 times the nominal NTSC horizontal scanning frequency. This small 437 Hz frequency discrepancy is easily accommodated by the automatic frequency and phase control of the controlled
20 local oscillator 16 in the tuner 5 of FIGURE 1. The addressing of ROMs 27 and 31 is greatly simplified when the QAM and VSB carriers are translated to be close to the third and seventh subharmonics of 21.52 MHz in final IF signals, since advantage can be taken of repetitive symmetries in the stored sine and cosine functions, to reduce the number of bits in the addresses applied to ROM.

25 The second harmonic of the 21.52 MHz sampling frequency is 43.05 MHz, and its subharmonics can be searched, looking for a pair offset from each other in frequency by an amount substantially equal to 2.69 MHz. The seventh and fifteenth subharmonics of 43.05 MHz are the third and seventh subharmonics of 21.52 MHz which have already been considered. The ninth and twenty-sixth subharmonics of

43.05 MHz at 4.305 MHz and at 1.594 MHz exhibit a 20 kHz or 0.74% error in regard to the desired 2.69 MHz offset and could respectively serve as QAM carrier and as VSB carrier. This error is within the 30 kHz or so mistuning tolerated in past commercial designs for NTSC TV receivers. The ROM 31 storing sine-cosine
5 look-up tables for the twenty-sixth subharmonic of 43.05 MHz has to store an excessive number of samples, however; and the ROM 27 storing sine-cosine look-up tables for the ninth subharmonic of 43.05 MHz has to store an appreciable number of samples, too.

The third harmonic of the 21.52 MHz sampling frequency is 64.57 MHz, and
10 its subharmonics can be searched, looking for a subharmonic offset in frequency from a subharmonic of 43.05 MHz or from another subharmonic of 64.57 MHz by an amount substantially equal to 2.69 MHz. The twelfth subharmonic of 64.57 MHz, 4.967 MHz, and the eighteenth subharmonic of 43.05 MHz, 2.265 MHz, exhibit a 12 kHz or 0.45% error in regard to the desired 2.69 MHz offset and could respectively
15 serve as QAM carrier and as a VSB carrier with its full sideband above its vestigial sideband in frequency. This error is well within the 30 kHz or so of mistuning tolerated in past commercial designs for NTSC TV receivers. However, the ROM 27 storing sine-cosine look-up tables for the twelfth subharmonic of 64.57 MHz has to store an excessive number of samples; and the ROM 31 storing sine-cosine look-up
20 tables for the eighteenth subharmonic of 43.05 MHz has to store an excessive number of samples, too.

The seventh subharmonic of 64.57 MHz is 8.07 MHz, offset almost exactly the desired 2.69 MHz from the third subharmonic of 21.52 MHz. This third subharmonic of 21.52 MHz, 5.38 MHz, and the seventh subharmonic of 64.57 MHz,
25 8.07 MHz, are appropriate for use as QAM carrier and a VSB carrier with its full sideband below its vestigial sideband in frequency.

It appears preferable that the frequencies of the local oscillators 11, 16 and 20 in the tuner 5 of FIGURE 1 be chosen so that the intermediate frequency to which the carrier of a QAM DTV signal is translated is 5.38 MHz, the presumed symbol rate for

the QAM DTV signal and half the standard symbol rate for the VSB DTV signal. Accordingly, if the VSB carrier is translated in frequency so as to have its full sideband above its vestigial sideband in frequency in the final IF signal, the preferred frequency of the VSB carrier in the final IF signal is 2.69 MHz. Alternatively, if the
5 VSB carrier is translated in frequency so as to have its full sideband below its vestigial sideband in frequency in the final IF signal, the preferred frequency of the VSB carrier in the final IF signal is 8.07 MHz.

It is noted in passing that all the subharmonics of 43.05 MHz and all the subharmonics of 64.57 MHz are subharmonics of 129.15 MHz, the third harmonic of
10 43.05 MHz and the second harmonic of 64.57 MHz. The 2.69 MHz, 5.68 MHz and 8.07 MHz frequencies are the forty-seventh, twenty-third and fifteenth subharmonics, respectively, of 129.15 MHz. It is also noted that while the harmonic relationship between carriers have been considered in terms of harmonics of the 21.52 MHz sampling rate that is the second harmonic of the 10.76 MHz VSB symbol rate, the
15 consideration thusfar can be viewed as involving the even harmonics of the 10.76 MHz symbol rate. A more complete consideration of the possible harmonic relationships between carriers also includes consideration of odd harmonics, at least third, of the 10.76 MHz VSB symbol rate. The 2.69 MHz, 5.68 MHz and 8.07 MHz frequencies are respectively the eleventh, fifth and third subharmonics of 32.29 MHz,
20 32.29 MHz being three times the 10.76 MHz symbol rate of the VSB signal.

One skilled in the art of designing analog-to-digital conversion circuitry for digital systems will appreciate that the sampling of analog signals for digitization can use various widths of sampling window. Thusfar, it has been presumed that $21.52 * 10^6$ samples per second are taken with the duration of each sampling window
25 extending over half a cycle of 21.52 MHz. The pulses from the limiter 233 can be stretched to nearly twice this duration, if desired. Another alternative that is possible is to design the analog-to-digital converter to use two staggered sets of sampling windows with each sampling window extending over half a cycle of 21.52 MHz and to digitize on a staggered-phase basis at a $43.05 * 10^6$ samples per second combined

rate. The digitization of final IF signal at a $43.05 \text{ MHz} * 10^6$ samples per second improves automatic phase and frequency control accuracy.

FIGURE 5 shows a modification of the FIGURE 4 circuitry that is possible when the third and the seventh subharmonics of 21.52 MHz are used as the final intermediate frequencies to which the QAM and VSB DTV carriers are respectively converted. In a modification 320 of the second address generator 32 described above, second address counter 321 is arranged to count modulo eight when sampling rate is $21.52 * 10^6$ samples per second, thereby to generate two cycles of ROM 27 addressing and the one cycle of addressing for a ROM 310 that replaces the ROM 31; and the less significant bits of the output count from the second address counter 321 are made available for replacing the basic first address from the first address counter 281. In a modification 280 of the first address generator 28 described above, the first address counter 281 is dispensed with, and the less significant bits of the second address counter 321 are applied to the adder 282 as basic first address instead of the count from the first address counter 281. The VSB complex carrier ROM 31 is replaced with a ROM 310 that comprises a portion 313 that stores only one-half cycle of VSB carrier cosine values and a portion 314 that stores only one-half cycle of VSB carrier sine values. These portions 313 and 314 of the ROM 310 are addressed by the less significant bits of the adder 322 sum output signal. A selective bits complementor 315 exclusive-ORs the most significant bit of the adder 322 sum output signal with each of the bits of the VSB carrier cosine values read from the portion 313 of the ROM 310 for generating a first summand input for a digital adder 317, and the most significant bit of the adder 322 sum output signal is provided with zero extension in the direction of increased significance for generating a second summand input for the adder 317. The sum output from the adder 317 provides eight cosine values of VSB carrier over eight first clock periods to define a complete cycle of VSB carrier. A selective bits complementor 316 exclusive-ORs the most significant bit of the adder 322 sum output signal with each of the bits of the VSB carrier sine values read from the portion 314 of the ROM 310 for generating a first summand input for a digital adder 318, and the most significant bit of the adder 322 sum output signal with

zero extension in the direction of increased significance is also applied as a second summand input for the adder 318. The sum output from the adder 318 provides eight sine values of VSB carrier over eight first clock periods to define a complete cycle of VSB carrier.

5 The FIGURE 5 or the FIGURE 4 circuitry can also be used when the fifth and third subharmonics of 32.29 MHz are used as the final intermediate frequencies to which the QAM and VSB DTV carriers are respectively converted. The contents of the portions 313 and 314 of the ROM 310 are modified for the higher-frequency 8.07 MHz VSB carrier, of course.

10 One skilled in the art of digital circuit design will understand that other hardware savings can be made in the FIGURE 4 read-only memory circuitry taking advantage of symmetries in the cosine and sine functions or the 90° offset in the respective phases of these two functions. One skilled in the art of digital circuit design and acquainted with the foregoing description will understand that
15 modifications of the FIGURE 4 and FIGURE 5 circuitry are possible that have an AFPC detector for the VCO 230 in which the oscillations from the VCO 230 as converted to square waves by the symmetrical clipper 233 are compared in frequency with frequency doubler response to the 10.76 MHz signal selected by the digital bandpass filter 237.

20 One skilled in the art of digital circuit design will be enabled by acquaintance with the foregoing description to implement circuitry in which the ADC 22 samples at a 43.05×10^6 samples per second sample rate during digitization. The VCO 230 is replaced by a VCO supplying 43.05 MHz oscillations; and, by way of example, oscillations from the VCO 230 as converted to square waves by the symmetrical
25 clipper 233 and frequency divided by the flip-flop 234 are compared in frequency with frequency doubler response to the 10.76 MHz signal selected by the digital bandpass filter 237. The 2:1 decimator 35 can be replaced by a 4:1 decimator, and the squarewave output signal from the flip-flop 234 can be divided by another factor of

two by a further flip-flop to provide support for generating a reduced-rate sample clock signal for the 4:1 decimator.

FIGURE 6 shows a form that the circuitry 24 can take, which comprises:

- 5 (a) a linear-phase, finite-impulse-response (FIR) digital filter 60 that generates imaginary (Im) digital samples as a Hilbert transform response to the real (Re) digital samples; and
- 10 (b) compensating, clocked digital delay of the real digital samples to compensate for the latency time of the Hilbert transformation filter 60, which clocked digital delay can be provided by clocked latch elements 61-66 included in the Hilbert transformation filter 60.

The use of such circuitry for implementing in-phase and quadrature-phase sampling procedures on bandpass signals is described by D. W. Rice and K. H. Wu in their article "Quadrature Sampling with High Dynamic Range" on pp. 736-739 of **IEEE TRANSACTIONS ON AEROSPACE AND ELECTRONIC SYSTEMS**, Vol. AES-18, No. 4 (Nov 1982). Since the frequency band 6 MHz wide occupied by the final IF signal has a lowest frequency of at least a megaHertz or so, it is possible to use as few as seven non-zero-weighted taps in the FIR filter 60 used for Hilbert transformation.

The seven-tap Hilbert transformation filter 60 includes a cascade connection of one-sample delay elements 61, 62, 63, 64, 65 and 66 from which samples taken to be weighted and summed to generate the Hilbert transform response. The Hilbert transform is linear phase in nature so the tap weights of the FIR filter 60 exhibit symmetry about median delay. Accordingly, a digital adder 67 sums the input signal to delay element 61 and the output signal from the delay element 66 to be weighted in common, a digital adder 68 sums the output signal from the delay element 61 and the output signal from the delay element 65 to be weighted in common, and a digital adder 69 sums the output signal from the delay element 62 and the output signal from the delay element 64 to be weighted in common. The output signal from the delay

element 64 is applied as input address to a read-only memory 70, which multiplies that signal by an appropriate weight W_0 magnitude. The sum output signal from the digital adder 69 is applied as input address to a read-only memory 71, which multiplies that signal by an appropriate weight W_1 magnitude. The sum output signal from the digital adder 68 is applied as input address to a read-only memory 72, which multiplies that signal by an appropriate weight W_2 magnitude. The sum output signal from the digital adder 67 is applied as input address to a read-only memory 73, which multiplies that signal by an appropriate weight W_3 magnitude. The use of the ROMs 70, 71, 72 and 73 as fixed-multiplicand multipliers keeps the delay associated with multiplication negligibly short. The output signals of the ROMs 70, 71, 72 and 73 are combined by a tree of signed digital adders 74, 75 and 76 operated as adders or subtractors, as required to appropriately assign signs to the magnitudes of the weights W_0 , W_1 , W_2 and W_3 stored in the ROMs 70, 71, 72 and 73. The adders 67, 68, 69, 74, 75 and 76 are assumed to be clocked adders each exhibiting one-sample latency, which results in the seven-tap FIR filter 60 exhibiting a six-sample latency. Delay of the filter 60 input signal that compensates for this latency is provided by the cascade connection of the six one-sample delay elements 61, 62, 63, 64, 65 and 66. The input address to the read-only memory 70 is taken from the output of the delay element 64, rather than from the output of the delay element 63, so the one-sample delay of delay element 64 compensates for the one-sample delays in the adders 67, 68 and 69.

C. M. Rader in his article "A Simple Method for Sampling In-Phase and Quadrature Components", IEEE TRANSACTIONS ON AEROSPACE AND ELECTRONIC SYSTEMS, Vol. AES-20, No. 6 (Nov 1984), pp. 821-824, describes improvements in complex synchronous detection carried out on digitized bandpass signals. Rader replaces the Hilbert-transform FIR filter and the compensating-delay FIR filter of Rice and Wu with a pair of all-pass digital filters designed based on Jacobian elliptic functions and exhibiting a constant $\pi/2$ difference in phase response for the digitized bandpass signals. A preferred pair of such all-pass digital filters, which are of infinite-impulse-response (IIR) type, has the following system functions:

$$H_1(z) = z^{-1}(z^2 - a^2) / (1 - a^2 z^2) \quad a^2 = 0.5846832$$

$$H_2(z) = -(z^2 - b^2) / (1 - b^2 z^2) \quad b^2 = 0.1380250$$

Rader describes filter configurations which require only two multiplications, one by a^2 and one by b^2 .

5 FIGURE 7 shows an alternative form that the circuitry 24 can take, which comprises a pair of all-pass digital filters 80 and 90 of a type described by C. M. Rader and designed based on Jacobian elliptic functions. The filters 80 and 90 exhibit a constant $\pi/2$ difference in phase response for digitized bandpass signals. Since oversampled real samples better provide for symbol synchronization when
10 synchrodyning VSB signals, the inventors prefer not to use the all-pass filters also described by Rader that exploit sub-sampling to provide further reductions in the delay network circuitry.

 The construction of the filter 80, which provides the system function $H_1(z) = z^{-1}(z^2 - a^2) / (1 - a^2 z^2)$, where $a^2 = 0.5846832$ in decimal arithmetic, is shown in
15 FIGURE 7 to be as follows. The samples from the ADC 22 are delayed by one ADC sample clock duration in a clocked delay element 88 for application to a node 89. The signal at node 89 is further delayed by two ADC sample clock durations in cascaded clocked delay elements 81 and 82, for application as first summand signal to a digital adder 83. The sum output signal of the adder 83 provides the real response from the
20 filter 80. The sum output signal of the adder 83 is delayed by two ADC sample clock durations in cascaded clocked delay elements 84 and 85, for application as minuend input signal to a digital subtractor 86 that receives the signal at node 89 as its subtrahend input signal. The resulting difference output signal from the digital subtractor 86 is supplied as multiplier input signal to a digital multiplier 87 for
25 multiplying an a^2 multiplicand signal, using a binary arithmetic. The resulting product output signal is applied to the digital adder 83 as its second summand signal.

 The construction of the filter 90, which provides the system function $-H_2(z) = (z^2 - b^2) / (1 - b^2 z^2)$, where $b^2 = 0.1380250$ in decimal arithmetic, is shown in

FIGURE 7 to be as follows. The samples from the ADC 22 are delayed by two ADC sample clock durations in cascaded clocked delay elements 91 and 92, for application as first summand signal to a digital adder 93. The sum output signal of the adder 93 provides the imaginary response from the filter 90. The sum output signal of the
5 adder 93 is delayed by two ADC sample clock durations in cascaded clocked delay elements 94 and 95, for application to a digital subtractor 96 as its minuend signal. The subtractor 96 receives the samples from the ADC 22 as its subtrahend input signal. The resulting difference output signal from the digital subtractor 96 is supplied as multiplier input signal to a digital multiplier 97 for multiplying a b^2
10 multiplicand signal, using a binary arithmetic. The resulting product output signal is applied to the digital adder 93 as its second summand signal.

FIGURE 8 shows a complex-signal filter resulting from modifying the FIGURE 7 complex-signal filter as follows. The position of the clocked delay element 88 is shifted so as to delay the sum output signal of the adder 83, rather than
15 to delay the digital output signal of the ADC 22, and the digital output signal of the ADC 22 is applied to the node 89 without delay, thereby to cause real response to be provided at the output port of the shifted-in-position clocked delay element 88. The real response provided at the output port of the shifted-in-position clocked delay element 81 is the same as the response provided at the output port of the clocked delay
20 element 84. So, the real response is provided from the output port of the clocked delay element 84 instead of from the output port of the shifted-in-position clocked delay element 81; and the shifted-in-position clocked delay element 81, being no longer required, is dispensed with.

FIGURE 9 shows a complex-signal filter resulting from modifying the
25 FIGURE 8 complex-signal filter as follows. The first summand signal for the adder 83 is then taken from the cascaded clocked delay elements 91 and 92, rather than from the cascaded clocked delay elements 81 and 82. The cascaded clocked delay elements 81 and 82, being no longer required, are dispensed with. The FIGURE 9

complex-signal filter is preferred over the complex-signal filters of FIGURE 7 and 8 in that redundant clocked delay elements are eliminated.

FIGURE 10 is a detailed block schematic diagram of a complex-signal filter developing a constant $\pi/2$ difference in phase between a real response Re and an
5 imaginary response Im to the digitized bandpass signals, that is similar the complex-signal filter described by T. F. S. Ng in United Kingdom patent application 2 244 410 A published 27 November 1991 and entitled QUADRATURE
DEMODULATOR. The Ng filters are finite-impulse-response (FIR) digital filters, rather than IIR filters as described by Rader. The FIGURE 10 complex-signal filter
10 differs from the filters described by Ng in that 2:1 decimation is done following filtering, rather than before.

This permits the real and imaginary filtering to be supported by a shared tapped delay line. FIGURE 10 shows this shared tapped delay line composed of cascaded single-clock-delay elements 100-114, such as latches that like the ADC 22
15 are clocked at four times symbol transmission rate. The single-clock-delay element 100 may be dispensed with or subsumed into the ADC 22 in some designs. Digital adders and subtractors in the FIGURE 6 complex filter are assumed to be clocked at four times symbol transmission rate, with each having a single-clock-duration latency. The digital multipliers are assumed to be a wired place shift in the case of a
20 multiplication by an integral power of two or to be provided from read-only memory (ROM), so there is zero latency in each of the multiplications insofar as clocked operation is concerned. At least the eight-bit resolution in the filter results per Ng is presumed.

In order to generate the real response $H_1(z)$, the real-response filter is presumed
25 to apply tap weights $W_0 = 4$, $W_1 = 0$, $W_2 = -12$, $W_3 = -72$, $W_4 = 72$, $W_5 = 12$, $W_6 = 0$ and $W_7 = -4$ per the example described by Ng. The real-response filter, in addition to the single-clock-delay elements 100-114, includes a digital subtractor 121 for subtracting the response of the delay element 114 from the response of the delay element 100, a digital multiplier 122 for weighting the differential response of the

subtractor 121 by a factor of four, a digital subtractor 125 for subtracting the response of the delay element 103 from the response of the delay element 109, a digital multiplier 126 for weighting the differential response of the subtractor 125 by a factor of twelve, a digital subtractor 127 for subtracting the response of the delay element
5 105 from the response of the delay element 107, a digital multiplier 128 for weighting the differential response of the subtractor 127 by a factor of seventy-two, a digital adder 129 for summing the products from the digital multipliers 126 and 128, a digital adder 130 for summing the product from the digital multiplier 122 with the sum output signal from the adder 129, and a 2:1 decimator 131 for generating the real filter
10 response Re in decimated response to the sum output signal from the adder 130.

The subtractor 121 subtracts the response of the delay element 114 from the response of the delay element 100, rather than subtracting the response of the delay element 113 from the output signal of the ADC 22, to introduce single-clock-duration delay to compensate for the latency of the adder 129. Since $W_1 = 0$ and $W_6 = 0$, there
15 is no digital subtractor 123 for subtracting the response of the delay element 111 from the response of the delay element 101 or digital multiplier 124 for weighting the differential response of the subtractor 123. Consequently, there is no digital adder for summing product from the multiplier 124 with the product from the multiplier 122. This gives rise to the need to compensate for the latency of the adder 129.

20 In order to generate the imaginary response $H_i(z)$, the imaginary-response filter is presumed to apply tap weights $W_8 = 8$, $W_9 = 14$, $W_{10} = 22$, $W_{11} = 96$, $W_{12} = 22$, $W_{13} = 14$, $W_{14} = 8$ corrected from the example described by Ng. The imaginary-response filter, in addition to the single-clock-delay elements 100-112, includes a digital adder 141 for adding the response of the delay element 112 with the
25 response of the delay element 100, a digital multiplier 142 for weighting the sum response of the adder 141 by a factor of eight, a digital adder 143 for adding the response of the delay element 110 with the response of the delay element 102, a digital multiplier 144 for weighting the sum response of the adder 143 by a factor of fourteen, a digital adder 145 for adding the response of the delay element 108 with the

response of the delay element 104, a digital multiplier 146 for weighting the sum
response of the adder 145 by a factor of twenty-two, a digital multiplier 147 for
weighting the response of the delay element 107 by a factor of ninety-six, a digital
adder 148 for summing the products from the digital multipliers 142 and 144, a digital
5 adder 149 for summing the products from the digital multipliers 146 and 147, a digital
adder 150 for summing the sum output signals from the adders 148 and 149, and a 2:1
decimator 151 for generating the imaginary filter response I_m in decimated response
to the sum output signal from the adder 150.

The digital multiplier 147 weights the response of the delay element 107 by a
10 factor of ninety-six, rather than the response of the delay element 106, in order to
introduce single-clock-duration delay to compensate for the single-clock-duration
latency of each of the adders 141 143 and 145.

Less preferred embodiments of the invention are contemplated in which the
trellis-decoded output signals of the two-dimensional symbol decoding circuitry 37
15 and of the one-dimensional symbol decoding circuitry 38 are supplied to respective
data de-interleavers, with data source selection being deferred until data
de-interleaving is completed. Other less preferred embodiments of the invention are
contemplated in which embodiments the trellis-decoded output signal of the
two-dimensional symbol decoding circuitry 37 is de-interleaved by a respective data
20 de-interleaver and then decoded by a respective Reed-Solomon decoder to generate a
first stream of error-corrected data, in which embodiments the trellis-decoded output
signal of the one-dimensional symbol decoding circuitry 38 is de-interleaved by a
respective data de-interleaver and then decoded by a respective Reed-Solomon
decoder to generate a second stream of error-corrected data, and in which
25 embodiments data source selection is made between the first and second streams of
error-corrected data. In modifications of these other less preferred embodiments of
the invention the first and second streams of error-corrected data are supplied to
separate data de-randomizers before data source selection is made. In other variants
separate Reed-Solomon decoders are used for the QAM and VSB signals, but one data

de-interleaver is used for both the QAM and VSB signals, or one data de-randomizer is used for both the first and second streams of error-corrected data.

The 2:1 decimator 35 of FIGURE 1 is replaced by a 4:1 decimator in embodiments of the invention in which the ADC 22 samples at a 43.05×10^6 samples per second sample rate during digitization, rather than a 21.52×10^6 samples per second sample rate. Such change requires appropriate modifications to the sample clock generator 23, of course. A sample rate higher than 21.52×10^6 samples per second is used when the synchrodyne circuitry 25 or 30 must synchrodyne to baseband a DTV signal having a carrier frequency higher than 5.38 MHz. Such a situation obtains when the synchrodyne circuitry 30 must synchrodyne to baseband a VSB signal having its vestigial sideband at frequencies greater than those in its full sideband. Decimators which decimate a baseband signal by a factor N more than two are better designed not to merely omit samples but rather to pre-filter the baseband signal and then to omit samples of the pre-filter response.

The preferred embodiments of the invention described supra use QAM synchrodyning circuitry and VSB synchrodyning circuitry of digital type. Digitizing final IF signals rather than baseband signals, as done in preferred embodiments of the invention reduces the number of analog-to-digital conversion procedures that must be done and avoids any problem with tracking the conversion characteristics of two analog-to-digital converters used in the QAM synchrodyning circuitry.

However, in other embodiments of the invention synchrodyning of the QAM signal to baseband is done using in-phase and quadrature-phase analog synchronous detectors, which are followed by analog-to-digital conversion circuitry for digitizing response from the in-phase analog synchronous detector to generate a real sample stream of interleaved QAM symbol code and for digitizing response from the quadrature-phase analog synchronous detector to generate an imaginary sample stream of interleaved QAM symbol code.

In other embodiments of the invention, adapted from the DTV receiver type used in field testing during the development of the ATSC standard, synchrodyning of the VSB signal to baseband is done using an analog synchronous detector, which is followed by an analog-to-digital converter (ADC) for digitizing response from the analog synchronous detector to generate a sample stream of interleaved VSB symbol code and then by a baseband phase tracker. In these other embodiments of the invention the decimation filter takes its input signal directly from the response of the baseband phase tracker.

The preferred embodiments of the invention use digital synchrodyning procedures to achieve "wrap-around" of symbol phase adjustment. The adjustment of symbol phase takes place in a bandpass transform of the baseband, so if the ROMs storing digital carrier are addressed suitably, symbol phase adjustment takes place on a closed cycle of adjustment range, rather than on an open linear adjustment range. If there is only an open linear adjustment range for symbol phase, which is all that is available at baseband, when the limit of adjustment range is reached symbol phasing will jump in time displacement. This jump in time will cause repetition of symbols in the symbol coding stream or will cause loss of symbols in the symbol coding stream, depending on whether the jump in time displacement is backward or is forward. These effects undesirably interfere with symbol counting within the data line in which the jump in time displacement occurs, causing temporary loss of data synchronization.

Television engineers are currently considering using the digital transmission system for HDTV for transmitting other types of television signals – for example, four television signals with resolution similar to present-day NTSC signals that are simultaneously transmitted. The invention is suitable for use in receivers for these alternative transmission schemes, and the claims which follow should be construed broadly enough to include such receivers within their scope.

In the claims which follow, the word "said" is used whenever reference is made to an antecedent, and the word "the" is used for grammatical purposes other than to refer back to an antecedent.



WHAT IS CLAIMED IS:

1. A digital television (DTV) signal receiver comprising:

a radio receiver portion for selecting a channel for reception, for converting DTV signal in the selected channel to intermediate frequencies for filtering and amplification, and for synchrodyning an analog final intermediate-frequency output
5 signal resulting from said filtering and amplification to baseband thereby to generate a baseband signal;

an analog-to-digital converter (ADC) included in said radio receiver portion for sampling one of said signals therein and digitizing it, so that said baseband signal is supplied from said radio receiver portion as a first stream of digital samples
10 descriptive of said baseband signal;

a sample clock generator for supplying a sample clock signal to time the sampling by said ADC so that said first stream of digital samples has a sample rate substantially equal to a prescribed multiple MN times the symbol rate of said DTV signal, MN being the product of a positive number M greater than one and of a
15 positive integer N at least two;

an $N:1$ decimator connected for receiving said first stream of digital samples and generating in response thereto a second stream of digital samples in which only every N^{th} one of said first stream of digital samples is reproduced at a sample rate one N^{th} that of said first stream of digital samples;

20 a channel equalizer for performing channel equalization on said second stream of digital samples to generate a channel equalizer response; and

symbol decoding circuitry for decoding symbols in said channel equalizer response, as corrected for symbol phase error, to recover groups of bits corresponding to decoded symbols.



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2. A DTV signal receiver as set forth in claim 1, wherein said sample clock generator comprises:

an oscillator for supplying oscillations at a frequency controlled by an automatic frequency and phase control signal;

5 circuitry for generating said sample clock signal at a rate responsive to said oscillation frequency;

an FIR filter for supplying a bandpass response to said first stream of digital samples which bandpass response is centered on a subharmonic of the symbol rate of said DTV signal;

10 a frequency multiplier for multiplying the frequency of a component of said bandpass response at said subharmonic of the symbol rate of said DTV signal to generate a harmonic of the symbol rate of said DTV signal; and

an automatic frequency and phase control detector for detecting frequency and phase error between the sampling rate of said ADC and said harmonic of the
15 symbol rate of said DTV signal, for application to said oscillator as its said automatic frequency and phase control signal.

3. A DTV signal receiver as set forth in claim 2, wherein N equals 2.

4. A DTV signal receiver as set forth in claim 2, wherein M equals 1 and N equals 2.

5. A DTV signal receiver as set forth in claim 1, wherein N equals 2.



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6. A DTV signal receiver as set forth in claim 1, wherein M equals 1 and N equals 2.
7. A DTV signal receiver as set forth in claim 1, further comprising:
 - data synchronization recovery circuitry for detecting data synchronization information extracted from said second stream of digital samples;
 - a de-interleaver for said bit groups;
- 5 a Reed-Solomon decoder receiving the response of said de-interleaver as its input signal; and
 - a de-randomizer responsive to the results from said Reed-Solomon decoder for restoring a signal randomized prior to transmission to said DTV receiver.
8. A DTV signal receiver as set forth in claim 7, wherein said data synchronization recovery circuitry is of a type for detecting data synchronization responsive to groups of bits said symbol decoder decodes from symbols in said channel equalizer.
9. A DTV signal receiver as set forth in claim 7, wherein said data synchronization recovery circuitry is of a type employing match filters for detecting data synchronization responsive to said second stream of digital samples.



10. A DTV signal receiver as set forth in claim 9, wherein said data synchronization recovery circuitry is connected to receive said second stream of digital samples after said channel equalizer has performed channel equalization thereon.

11. A DTV signal receiver as set forth in claim 1, wherein said ADC is connected for sampling said analog final intermediate-frequency output signal, and wherein the synchrodyning of said analog final intermediate-frequency output signal to baseband is done by digital synchrodyning apparatus for QAM digital television signals.

12. A DTV signal receiver as set forth in claim 11, further comprising:

data synchronization recovery circuitry for detecting data synchronization responsive to groups of bits said symbol decoder decodes from symbols in said channel equalizer response;

5 a de-interleaver for said bit groups;

a Reed-Solomon decoder receiving the response of said de-interleaver as its input signal; and

a de-randomizer responsive to the results from said Reed-Solomon decoder for restoring a signal randomized prior to transmission to said DTV receiver.



13. A DTV signal receiver as set forth in claim 11, further comprising:

data synchronization recovery circuitry employing match filters for detecting data synchronization responsive to said second stream of digital samples;

a de-interleaver for said bit groups;

5 a Reed-Solomon decoder receiving the response of said de-interleaver as its input signal; and

a de-randomizer responsive to the results from said Reed-Solomon decoder for restoring a signal randomized prior to transmission to said DTV receiver.

14. A DTV signal receiver as set forth in claim 13, wherein said data synchronization recovery circuitry is connected to receive said second stream of digital samples after said channel equalizer has performed channel equalization thereon.

15. A DTV signal receiver as set forth in claim 11, wherein said sample clock generator comprises:

an oscillator for supplying oscillations at a frequency controlled by an automatic frequency and phase control signal;

5 circuitry for generating said sample clock signal at a rate responsive to said oscillation frequency;

an FIR filter for supplying a bandpass response to said first stream of digital samples which bandpass response is centered on a subharmonic of the symbol rate of said DTV signal;



10 a frequency multiplier for multiplying the frequency of a component of said bandpass response at said subharmonic of the symbol rate of said DTV signal to generate a harmonic of the symbol rate of said DTV signal; and

 an automatic frequency and phase control detector for detecting frequency and phase error between the sampling rate of said ADC and said harmonic of the
15 symbol rate of said DTV signal, for application to said oscillator as its said automatic frequency and phase control signal.

16. A DTV signal receiver as set forth in claim 15, further comprising:

 data synchronization recovery circuitry for detecting data synchronization responsive to groups of bits said symbol decoder decodes from symbols in said channel equalizer response;

5 a de-interleaver for said bit groups;

 a Reed-Solomon decoder receiving the response of said de-interleaver as its input signal; and

 a de-randomizer responsive to the results from said Reed-Solomon decoder for restoring a signal randomized prior to transmission to said DTV receiver.

17. A DTV signal receiver as set forth in claim 15, further comprising:

 data synchronization recovery circuitry employing match filters for detecting data synchronization responsive to said second stream of digital samples;

 a de-interleaver for said bit groups;

5 a Reed-Solomon decoder receiving the response of said de-interleaver as its input signal; and



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a de-randomizer responsive to the results from said Reed-Solomon decoder for restoring a signal randomized prior to transmission to said DTV receiver.

18. A DTV signal receiver as set forth in claim 17, wherein said data synchronization recovery circuitry is connected to receive said second stream of digital samples after said channel equalizer has performed channel equalization thereon.

19. A DTV signal receiver as set forth in claim 1, wherein said ADC is connected for sampling said analog final intermediate-frequency output signal, and wherein the synchrodyning of said analog final intermediate-frequency output signal to baseband is done by digital synchrodyning apparatus for VSB digital television signals.

20. A DTV signal receiver as set forth in claim 19, further comprising:

data synchronization recovery circuitry for detecting data synchronization responsive to groups of bits said symbol decoder decodes from symbols in said channel equalizer response;

5 a de-interleaver for said bit groups;

a Reed-Solomon decoder receiving the response of said de-interleaver as its input signal; and

a de-randomizer responsive to the results from said Reed-Solomon decoder for restoring a signal randomized prior to transmission to said DTV receiver.



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21. A DTV signal receiver as set forth in claim 19, further comprising:

data synchronization recovery circuitry employing match filters for detecting data synchronization responsive to said second stream of digital samples;

a de-interleaver for said bit groups;

5 a Reed-Solomon decoder receiving the response of said de-interleaver as its input signal; and

a de-randomizer responsive to the results from said Reed-Solomon decoder for restoring a signal randomized prior to transmission to said DTV receiver.

22. A DTV signal receiver as set forth in claim 21, wherein said data synchronization recovery circuitry is connected to receive said second stream of digital samples after said channel equalizer has performed channel equalization thereon.

23. A DTV signal receiver as set forth in claim 19, wherein said sample clock generator comprises:

an oscillator for supplying oscillations at a frequency controlled by an automatic frequency and phase control signal;

5 circuitry for generating said sample clock signal at a rate responsive to said oscillation frequency;

an FIR filter for supplying a bandpass response to said first stream of digital samples which bandpass response is centered on a subharmonic of the symbol rate of said DTV signal;



10 a frequency multiplier for multiplying the frequency of a component of said bandpass response at said subharmonic of the symbol rate of said DTV signal to generate a harmonic of the symbol rate of said DTV signal; and

 an automatic frequency and phase control detector for detecting frequency and phase error between the sampling rate of said ADC and said harmonic of the
15 symbol rate of said DTV signal, for application to said oscillator as its said automatic frequency and phase control signal.

24. A DTV signal receiver as set forth in claim 23, further comprising:

 data synchronization recovery circuitry for detecting data synchronization responsive to groups of bits said symbol decoder decodes from symbols in said channel equalizer response;

5 a de-interleaver for said bit groups;

 a Reed-Solomon decoder receiving the response of said de-interleaver as its input signal; and

 a de-randomizer responsive to the results from said Reed-Solomon decoder for restoring a signal randomized prior to transmission to said DTV receiver.

25. A DTV signal receiver as set forth in claim 23, further comprising:

 data synchronization recovery circuitry employing match filters for detecting data synchronization responsive to said second stream of digital samples;

 a de-interleaver for said bit groups;

5 a Reed-Solomon decoder receiving the response of said de-interleaver as its input signal; and



a de-randomizer responsive to the results from said Reed-Solomon decoder for restoring a signal randomized prior to transmission to said DTV receiver.

26. A DTV signal receiver as set forth in claim 25, wherein said data synchronization recovery circuitry is connected to receive said second stream of digital samples after said channel equalizer has performed channel equalization thereon.

27. A DTV signal receiver for recovering baseband digital samples of symbol code from the DTV signal, including

an analog-to-digital converter for sampling the DTV signal in accordance with a first sample clock signal and a

5 a sample clock generator for generating said first sample clock signal, said sample clock generator comprising:

a controlled oscillator for supplying oscillations;

circuitry for supplying said first sample clock signal as timed by said oscillations;

10 a narrow bandpass, finite-impulse-response (FIR), first digital filter centered at a frequency that is a subharmonic of the symbol rate of said symbol code having substantial strength, said first digital filter connected for supplying a first digital filter response to said baseband digital samples of symbol code, which said first digital filter response contains said subharmonic of the symbol rate of said symbol code;

15 a frequency multiplier for supplying, in response to said first digital filter response, a frequency multiplier response that contains a multiple of said subharmonic of the symbol rate of said symbol code; and



automatic-frequency-and-phase-control circuitry responsive to said multiple of
said subharmonic of the symbol rate of said symbol code in said frequency multiplier
20 response and to a signal derived from the oscillations of said controlled oscillator for
developing an automatic-frequency-and-phase-control (AFPC) signal for said
controlled oscillator.

28. A DTV signal receiver as set forth in claim 27, wherein said controlled
oscillator is of a type supplying cissoidal oscillations at a frequency twice symbol
frequency, and wherein said circuitry for supplying said first sample clock signal as
timed by said oscillations comprises:

5 clipper circuitry for symmetrically clipping said cissoidal oscillations to
generate essentially square waves of said frequency twice symbol frequency, used as
said first sample clock signal.

29. A DTV signal receiver as set forth in claim 28, wherein said sample clock
generator further comprises:

a flip-flop connected as a frequency divider for responding to said essentially
square waves of said frequency twice symbol frequency to generate square waves of
5 said symbol frequency, said signal derived from the oscillations of said controlled
oscillator that said automatic-frequency-and-phase-control circuitry is responsive
corresponding to said square waves of said symbol frequency.

30. A DTV signal receiver as set forth in claim 29, further comprising:



a 2:1 decimator responsive to said baseband digital samples of symbol code from the DTV signal for supplying an output signal with half as many samples therein;

- 5 a channel equalization filter responsive to the output signal from said 2:1 decimator; and

an AND gate included in said sample clock generator for generating an AND response to said essentially square waves of said frequency twice symbol frequency from said clipper circuitry and to said square waves of said symbol frequency from
10 said flip-flop, said AND response being supplied as a second sample clock frequency to said 2:1 decimator for timing the samples in the output signal from said 2:1 decimator.

31. A DTV signal receiver as set forth in claim 30, wherein said frequency multiplier comprises:

a first squaring circuit for squaring said first digital filter response to develop a squared first digital filter response containing second harmonics of the components of
5 said first digital filter response; and

a narrow bandpass, finite-impulse-response (FIR), second digital filter centered at a frequency that corresponds to the symbol rate of said symbol code, said second digital filter connected for filtering said squared first digital filter response for supplying a second digital filter response.

32. A DTV signal receiver as set forth in claim 31, wherein said second digital filter response is applied to said automatic-frequency-and-phase-control circuitry as said multiple of said subharmonic of the symbol rate of said symbol code in said frequency multiplier response.



33. A DTV signal receiver as set forth in claim 31, wherein said frequency multiplier further comprises:

a second squaring circuit for squaring said second digital filter response to develop a squared second digital filter response containing second harmonics of the components of said second digital filter response; and

a narrow bandpass, finite-impulse-response (FIR), third digital filter centered at a frequency that corresponds to twice the symbol rate of said symbol code, said third digital filter connected for filtering said squared second digital filter response for supplying a third digital filter response applied to said automatic-frequency-and-phase-control circuitry as said multiple of said subharmonic of the symbol rate of said symbol code in said frequency multiplier response.

34. A DTV signal receiver as set forth in claim 27, wherein said frequency multiplier comprises:

a first squaring circuit for squaring said first digital filter response to develop a squared first digital filter response containing second harmonics of the components of said first digital filter response; and

a narrow bandpass, finite-impulse-response (FIR), second digital filter centered at a frequency that corresponds to the symbol rate of said symbol code, said second digital filter connected for filtering said squared first digital filter response for supplying a second digital filter response.

35. A DTV signal receiver as set forth in claim 34, wherein said second digital filter response is applied to said automatic-frequency-and-phase-control circuitry as



said multiple of said subharmonic of the symbol rate of said symbol code in said frequency multiplier response.

36. A DTV signal receiver as set forth in claim 34, wherein said frequency multiplier further comprises:

5 a second squaring circuit for squaring said second digital filter response to develop a squared second digital filter response containing second harmonics of the components of said second digital filter response; and

10 a narrow bandpass, finite-impulse-response (FIR), third digital filter centered at a frequency that corresponds to twice the symbol rate of said symbol code, said third digital filter connected for filtering said squared second digital filter response for supplying a third digital filter response applied to said automatic-frequency-and-phase-control circuitry as said multiple of said subharmonic of the symbol rate of said symbol code in said frequency multiplier response.