(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
7 March 2002 (07.03.2002)

PCT

(10) International Publication Number
WO 02/19112 A1

(51) International Patent Classification[7]: G06F 11/20

(21) International Application Number: PCT/US01/09997

(22) International Filing Date: 28 March 2001 (28.03.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/651,472 30 August 2000 (30.08.2000) US

(71) Applicant *(for all designated States except US)*: **MICRON TECHNOLOGY, INC.** [US/US]; 8000 South Federal Way, Boise, ID 83716-9632 (US).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **SANTIN, Giovanni** [IT/IT]; 10, via D'Aquilio, I-2010 Santa Rufina (IT).

(74) Agent: **VIKSNINS, Ann, S.**; Schwegman, Lundberg, Woessner & Kluth, P.O. Box 2938, Minneapolis, MN 55402 (US).

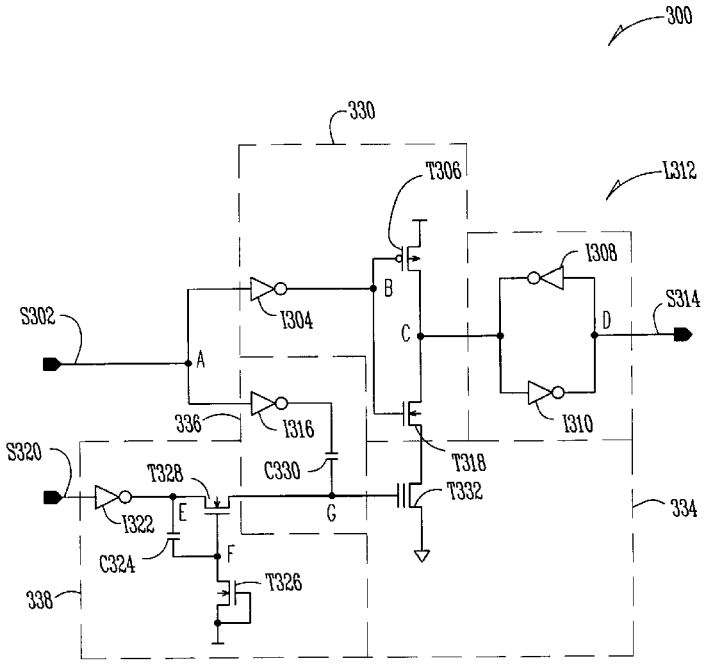
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

[Continued on next page]

(54) Title: FUSE CONFIGURATIONS FOR LOW-VOLTAGE FLASH MEMORIES



(57) Abstract: An enhanced fuse circuit is discussed that advances redundancy techniques in integrated circuits. The enhanced fuse circuit uses a single nonvolatile fuse and a latch that is coupled at a desired time. One embodiment of the invention discusses a fuse circuit that includes a volatile latch and a nonvolatile fuse. The nonvolatile fuse adapts to operate with a voltage supply greater than about 1.65 volts. The voltage supply is boosted at a desired time to a predetermined leve and for a predetermined duration so that the nonvolatile fuse transfers its data to the volatile latch.

WO 02/19112 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.