

DESCRIPTION

**TITLE: CARRIER COMPRISING AN ELECTRICAL-CHARGE-TRAPPING LAYER
FOR A COMPOSITE SUBSTRATE AND METHOD OF SELECTING SUCH A
CARRIER.**

FIELD OF THE INVENTION

The invention relates to a carrier having an electrical-charge-trapping layer, the carrier being intended to receive a thin crystalline layer through a layer-transfer technique. A composite substrate formed of such a carrier is applicable in the field of integrated electronic components, in particular of radio-frequency (RF) components processing signals the frequency of which may typically be between 20 kHz and 300 GHz, or more. In addition to the carrier itself, the invention also relates to a method of selecting a carrier substrate.

TECHNOLOGICAL BACKGROUND OF THE INVENTION

For reasons of simplicity of implementation, the electrical-charge-trapping layer (more concisely referred to as the "trapping layer" in the remainder of this description) is generally formed by depositing a layer of polycrystalline silicon on a base substrate, as illustrated in particular by documents US7585748 and US9293473.

The boundaries of the silicon grains making up the polycrystalline layer form traps for any electrical charge capable of flowing. These traps may be formed at these boundaries by incomplete or dangling chemical bonds. Electrical conduction is thus prevented in the trapping layer, which therefore has a high resistivity, typically one higher than 1000 ohms.cm.

In general, the prior art reveals the need for an electrical-charge-trapping layer which has a high resistivity and which is temperature-stable. This temperature stability is an important characteristic because the manufacture of a composite substrate involves heat treatments which typically raise the temperature of the carrier to more than 1000°C, this tending to cause the desired characteristics to be lost through recrystallization of the trapping layer and removal of the structural defects of this layer.

In order to preserve the polycrystalline quality of the trapping layer during the heat treatments to which the carrier may be subjected, provision may advantageously be made for an amorphous layer, made of silicon dioxide for example, on the base substrate before the trapping layer is deposited, as proposed by documents US8765571 and US9129800. However, the presence of this amorphous layer is not always enough to prevent the recrystallization of a trapping layer and/or the removal of its structural defects.

The applicant observed that the good temperature resistance of a trapping layer was closely related to the formation parameters of this layer. However, it is not currently possible to correlate the formation parameters of this layer (or measurable characteristics of this layer) with this property of temperature resistance. The only possible evaluation is made by a posteriori characterization of the radio-frequency (RF) performance of the composite substrate in which it is integrated, after the trapping layer has been subjected to the heat treatments for manufacturing this substrate.

SUBJECT OF THE INVENTION

One object of the invention is to at least partly address this problem. More precisely, one object of the invention is to be able to determine in advance, simply, whether a trapping layer of a carrier is capable of receiving the heat treatments of a method for manufacturing a composite substrate without excessively recrystallizing, and thus preserve its trapping qualities in the composite substrate. One object of the invention is therefore to determine characteristics of a trapping layer which is temperature-stable. Another object of the invention is to make use of these characteristics to select a carrier provided with a trapping layer with a view to forming a composite substrate.

BRIEF DESCRIPTION OF THE INVENTION

With a view to achieving this object, the subject of the invention proposes a carrier for a composite substrate, the carrier comprising a base substrate and a trapping layer of polycrystalline silicon disposed on the base substrate.

According to the invention, the trapping layer has electrical traps of a first type and of a second type.

The electrical traps of the first type have an activation energy of 0.383 eV to within 0.008 eV and an effective capture cross section for holes and for electrons that is less than 10^{-16} cm². The electrical traps of the second type have an activation energy of 0.428 eV to within 0.016 eV and an effective capture cross section for holes and for electrons that is less than 10^{-16} cm².

According to other advantageous and non-limiting features of the invention, taken alone or according to any technically feasible combination:

- the electrical traps of the first type have an effective capture cross section for holes that is $1.7 \cdot 10^{-17}$ to within $0.1 \cdot 10^{-17}$ and an effective capture cross section for electrons that is $5.4 \cdot 10^{-17}$ to within $0.2 \cdot 10^{-17}$;
- the electrical traps of the second type have an effective capture cross section for electrons that is $1.8 \cdot 10^{-17}$ to within $1.1 \cdot 10^{-17}$ and an effective capture cross section for holes that is $5.7 \cdot 10^{-17}$ to within $3.7 \cdot 10^{-18}$;
- the trapping layer is free of electrical traps of a third type, the electrical traps of the third type having an activation energy of 0.485 eV to within 0.015 eV and an effective capture cross section for holes and for electrons that is greater than 10^{-16} cm^2 ;
- the electrical traps of the third type have an effective capture cross section for electrons that is $1.0 \cdot 10^{-15}$ to within $0.1 \cdot 10^{-15}$ and an effective capture cross section for holes that is $3.3 \cdot 10^{-16}$ to within $0.2 \cdot 10^{-16}$;
- the trapping layer further comprises electrical traps of a fourth type and of a fifth type, the electrical traps of the fourth type having an activation energy of 0.392 eV to within 0.018 eV and an effective capture cross section for holes and for electrons that is less than 10^{-16} cm^2 , the electrical traps of the fifth type having an activation energy of 0.371 eV to within 0.025 eV and an effective capture cross section for holes and for electrons that is less than 10^{-16} cm^2 ;

- the electrical traps of the fourth type have an effective capture cross section for electrons that is $3.8 \cdot 10^{-17}$ to within $0.3 \cdot 10^{-17}$ and an effective capture cross section for holes that is $1.2 \cdot 10^{-17}$ to within $0.1 \cdot 10^{-17}$;
- the electrical traps of the fifth type have an effective capture cross section for electrons that is $6.9 \cdot 10^{-17}$ to within $0.7 \cdot 10^{-17}$ and an effective capture cross section for holes that is $2.2 \cdot 10^{-17}$ to within $0.2 \cdot 10^{-17}$;
- the trapping layer is free of electrical traps of a sixth type and of a seventh type, the electrical traps of the sixth type having an activation energy of 0.474 eV to within 0.032 eV and an effective capture cross section for holes that is greater than 10^{-16} cm^2 , the electrical traps of the seventh type having an activation energy of 0.416 eV to within 0.017 eV and an effective capture cross section for holes that is greater than 10^{-16} cm^2 ;
- the electrical traps of the sixth type have an effective capture cross section for holes that is $5.2 \cdot 10^{-16}$ to within $0.5 \cdot 10^{-16}$;
- the electrical traps of the seventh type have an effective capture cross section for holes that is $1.7 \cdot 10^{-16}$ to within $0.1 \cdot 10^{-16}$.

According to another aspect, the subject of the invention proposes a method of selecting a carrier, the method comprising:

- a step of providing the carrier comprising a base substrate and a trapping layer of polycrystalline silicon disposed on the base substrate, the trapping layer comprising electrical traps;

- a characterization step comprising measuring an activation energy and an effective hole and/or electron capture cross section of the electrical traps of the trapping layer, the characterization step also comprising identifying different types of electrical traps present in the trapping layer;
- a selection step during which the carrier is selected if the trapping layer has electrical traps of a first type and of a second type, the electrical traps of the first type having an activation energy of 0.383 eV to within 0.008 eV and an effective capture cross section for holes and for electrons that is less than 10^{-16} cm^2 , the electrical traps of the second type having an activation energy of 0.428 eV to within 0.016 eV and an effective capture cross section for holes and for electrons that is less than 10^{-16} cm^2 .

According to other advantageous and non-limiting features of this aspect of the invention, taken alone or according to any technically feasible combination:

- during the selection step the carrier is selected if the trapping layer is also free of electrical traps of a third type, the electrical traps of the third type having an activation energy of 0.485 eV to within 0.015 eV and an effective capture cross section for holes and for electrons that is greater than 10^{-16} cm^2 ;
- during the selection step the carrier is selected if the trapping layer also comprises electrical traps of a fourth type and of a fifth type, the electrical traps of the fourth type having an activation energy of 0.392 eV to within 0.018 eV and an effective capture cross section for holes and for electrons that is less than 10^{-16} cm^2 , the electrical traps of the fifth type having an activation energy of 0.371

eV to within 0.025 eV and an effective capture cross section for holes and for electrons that is less than 10^{-16} cm²;

- during the selection step the carrier is selected if the trapping layer is also free of electrical traps of a sixth type and of a seventh type, the electrical traps of the sixth type having an activation energy of 0.474 eV to within 0.032 eV and an effective capture cross section for holes that is greater than 10^{-16} cm², the electrical traps of the seventh type having an activation energy of 0.416 eV to within 0.017 eV and an effective capture cross section for holes that is greater than 10^{-16} cm².

BRIEF DESCRIPTION OF THE FIGURES

Other features and advantages of the invention will become apparent from the detailed description of the invention that follows, with reference to the appended figures, in which:

[Fig. 1] [Fig. 2]

Figures 1 and 2 show seven types of electrical traps (T1 to T7) present in trapping layers of polycrystalline silicon;

[Fig. 3]

Figure 3 shows a carrier according to the invention;

[Fig. 4]

Figure 4 shows a composite substrate utilizing a carrier according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

To begin, it should be mentioned that some defects introduced into the crystal lattice of a semiconductor material may be electrically active and introduce energy levels in the forbidden band of this material. This is in particular the case for intrinsic defects of the crystal lattice: lacuna, self-interstitial, antisite, dislocations, interfaces, grain boundaries (for a polycrystalline material).

These energy levels are called electrical traps and the presence of these traps modifies the electrical properties of the semiconductor material by capturing electrons or holes that are free and/or by emitting electrons or holes that are trapped. Depending on the energy level of the traps, that is to say its position in the forbidden band, some transition probabilities become dominant, this giving particular characteristics to materials provided with such traps.

If the energy level places it between the minimum energy of the conduction band and the middle of the forbidden band, then the trap will tend to act as an electron trap. The probability of an electron being re-emitted by the trap will depend on its activation energy, which is the energy needed to overcome the barrier of potential created by the trap. This energy is equal to the difference between the minimum energy of the conduction band and the energy level of the trap. Similarly, if the energy level places a trap between the maximum energy of the valence band and the middle of the forbidden band, then the trap will act as a hole trap. The activation energy allowing the re-emission of this hole corresponds to the difference between the energy level of the trap and the maximum energy of the valence band.

The activation energy of a trap therefore forms an important characteristic of this trap. In addition to this level, an electrical trap may be characterized by its effective hole and/or electron capture cross section (generally expressed in cm^2). From a physical point of view, this cross section represents the effective area around the trap that a charge-carrier must pass through in order to be able to be captured. Charge-carriers move randomly through the crystal lattice of the material, and those which enter the effective area around the trap are close enough to be captured by the latter. The physically permissible values of an effective capture cross section may vary between 10^{-18} and 10^{-14} cm^2 .

Numerous methods exist for retrieving the characteristics of the electrical traps present in a material. The basic principle of these methods is often the same regardless of the material to be analysed, the test structure or the technique utilized. It consists in disturbing the electrical balance of the material by injecting (or by removing) charge-carriers. This may be accomplished, for example, by abruptly changing the reverse voltage of a Schottky diode or by illuminating the material. The return to the electrical balance of the material is then observed for different temperatures and/or under optical excitation. The change in occupancy in the traps is analysed by measuring the current or the capacitance (depending on the test structure used).

Photo-induced current transient spectroscopy is a well-known technique which is particularly effective when it comes to characterizing the electrical traps present in a trapping layer of polycrystalline silicon disposed on a base substrate. A detailed explanation of this technique can be found in the document "Deep level spectroscopy in high resistivity materials" (Appl. Phys. Lett. 32, 821 (1978); doi: 10.1063/1.89929) or in

the document "Characterization and Role of Deep Traps on the Radio Frequency Performances of High Resistivity Substrates" *J. Appl. Phys.* 7 June 2021; 129 (21): 215701. <https://doi.org/10.1063/5.0045306>.

According to this technique, the injection of charge-carriers is ensured by illuminating the sample of material to be analysed, and the signatures of the traps (activation level and effective capture cross section) are retrieved from a spectrum constructed from the measurement of the transient current coming from the thermally freed charge-carriers.

The inventors of the present application had the intuition that some defects in the crystal lattice of a trapping layer of polycrystalline silicon were more temperature-resistant than others. In an attempt to distinguish between all the possible defects, those that are temperature-resistant and those that are not, the inventors identified the types of traps present in a wide variety of trapping layers of polycrystalline silicon by measuring their electrical characteristics, then identified the types of traps associated with trapping layers that are temperature-resistant (unlikely to recrystallize entirely) and those associated with trapping layers that are not very temperature-resistant (and therefore likely to recrystallize entirely).

In particular, the applicant identified seven types of electrical traps, which are described below. To obtain this classification, the applicant carried out a series of experiments leading to the formation of a plurality of carriers by depositing layers of polycrystalline silicon (i.e. the trapping layer) on base substrates, the layers being produced according to different deposition techniques and parameters. The defects present in the trapping layer of each carrier were

characterized using the photo-induced current transient spectroscopy technique described above, in order to determine the activation energy and the effective electron and/or hole capture cross section thereof, this having made it possible to identify the different types of electrical traps. The carriers were subjected to a heat treatment at 1100°C for two hours and the trapping layer was then observed in order to determine whether or not its polycrystalline nature had been preserved.

The types of traps are characterized by their activation energy and by their effective cross sections. In some cases, the characterization method does not make it possible to determine whether the traps of a given type are hole traps, electron traps or mixed traps. For these types of traps, two characteristics for effective cross section have therefore been defined, one considering that it is a hole trap and the other considering that it is an electron trap.

Type 1 traps

The electrical traps of the first type which proved to be temperature-resistant have:

- an activation energy of 0.383 eV to within 0.008 eV.
- an effective capture cross section for electrons that is $5.4 \cdot 10^{-17}$ to within $0.2 \cdot 10^{-17}$.
- an effective capture cross section for holes that is $1.7 \cdot 10^{-17}$ to within $0.1 \cdot 10^{-17}$.

Type 2 traps

The electrical traps of the second type which proved to be temperature-resistant have:

- an activation energy of 0.428 eV to within 0.016 eV.
- an effective capture cross section for electrons that is $1.8 \cdot 10^{-17}$ to within $1.1 \cdot 10^{-17}$.

- an effective capture cross section for holes that is $5.7 \cdot 10^{-17}$ to within $3.7 \cdot 10^{-18}$.

Type 3 traps

The electrical traps of the third type are not found in the trapping layers of polycrystalline silicon, which proved to be temperature-resistant. These traps of the third type have:

- an activation energy of 0.485 eV to within 0.015 eV.
- an effective capture cross section for electrons that is $1.0 \cdot 10^{-15}$ to within $0.1 \cdot 10^{-15}$.
- an effective capture cross section for holes that is $3.3 \cdot 10^{-16}$ to within $0.2 \cdot 10^{-16}$.

Type 4 traps

The electrical traps of the fourth type which proved to be temperature-resistant have:

- an activation energy of 0.392 eV to within 0.018 eV.
- an effective capture cross section for electrons that is $3.8 \cdot 10^{-17}$ to within $0.3 \cdot 10^{-17}$.
- an effective capture cross section for holes that is $1.2 \cdot 10^{-17}$ to within $0.1 \cdot 10^{-17}$.

Type 5 traps

The electrical traps of the fifth type which proved to be temperature-resistant have:

- an activation energy of 0.371 eV to within 0.025 eV.
- an effective capture cross section for electrons that is $6.9 \cdot 10^{-17}$ to within $0.7 \cdot 10^{-17}$.
- an effective capture cross section for holes that is $2.2 \cdot 10^{-17}$ to within $0.2 \cdot 10^{-17}$.

Type 6 traps

The electrical traps of the sixth type are not found in the trapping layers of polycrystalline silicon, which proved to be temperature-resistant. These traps of the sixth type have:

- an activation energy of 0.474 eV to within 0.032 eV.
- an effective capture cross section for holes that is $5.2 \cdot 10^{-16}$ to within $0.5 \cdot 10^{-16}$.

Type 7 traps

The electrical traps of the seventh type are not found in the trapping layers of polycrystalline silicon, which proved to be temperature-resistant. These traps of the seventh type have:

- an activation energy of 0.416 eV to within 0.017 eV.
- an effective capture cross section for holes that is $1.7 \cdot 10^{-16}$ to within $0.1 \cdot 10^{-16}$.

It is noted that in addition to the nature of the traps, it is of course important that the cumulative density of all the traps is enough for the trapping effect to be present. At least a surface density of $2.0 \cdot 10^{11}$ traps.cm⁻², preferentially more than $1.0 \cdot 10^{12}$ traps.cm⁻², or even more than $1.0 \cdot 10^{13}$ traps.cm⁻², is required. For a layer with a thickness of 1 μm, this gives $2.0 \cdot 10^{15}$, $2.0 \cdot 10^{16}$ and $2.0 \cdot 10^{17}$ traps.cm⁻³, respectively.

Figure 1 shows the seven types of traps T1 to T7 according to their activation energy level EA. It is noted that it is not possible to distinguish between the types of traps which are present in the resistant trapping layers and the traps present in the non-resistant trapping layers on the basis of this activation energy level alone, and that the complete characterization (including the effective capture cross section value) is required for this. This can be seen in Figure 2 where it is noted that the effective capture cross section for holes

and for electrons is less than 10^{-16} cm² for all trap types found in a resistant trapping layer, and greater than this limit of 10^{-16} cm² otherwise.

Thus, and according to the invention, a carrier 1 formed of a base substrate 2 and a trapping layer 3a, intended for the production of a composite substrate, consists of a trapping layer 3a having electrical traps of the first type and of the second type. Advantageously, the trapping layer 3a is free of electrical traps of the third type. More advantageously, the trapping layer 3a further comprises electrical traps of the fourth type and of the fifth type, and it is free of electrical traps of the sixth type and of the seventh type.

Figure 3 thus shows a carrier 1 according to one of the modes of implementation. This carrier 1 is intended to receive, through a layer-transfer technique, a thin crystalline layer in order to form a composite substrate S, shown in Figure 4. Very generally, the carrier 1 comprises, disposed on a base substrate 2, a trapping layer 3a in contact with the base substrate 2. As shown in Figure 3, provision may be made for a dielectric layer 3b disposed on and in contact with the trapping layer 3a but this dielectric layer 3b is perfectly optional. When it is present, the dielectric layer 3b has a thickness typically of between 10 nm and 10 microns, essentially dictated by the need of the application of the composite substrate S that the carrier 1 is intended to form.

Conventionally, the carrier 1 may be in the form of a circular wafer, the diameter of which may be 100, 150, 200, 300 or even 450 mm.

The base substrate 2 of the carrier 1, on which the trapping layer 3a rests, typically has a thickness of several hundred

micrometres. Preferentially, the base substrate 2 has a high resistivity, higher than 1000 ohms.centimetres, and even more preferentially higher than 2000 ohms.centimetres. The density of the charges, i.e. holes or electrons, which are liable to move in the base substrate 2 is thereby limited. However, the invention is not limited to a base substrate 2 having such a resistivity, and it also provides advantages in terms of RF performance when the base substrate 2 has a more typical resistivity, of the order of a few hundred ohms.centimetres, for example lower than 1000 ohms.cm, or than 500 ohms.cm or even than 10 ohms.cm.

For reasons of availability and cost, the base substrate 2 is preferentially made of monocrystalline silicon. The base substrate 2 may alternatively be formed from another material: this may be, for example, sapphire, glass, quartz, silicon carbide, germanium, gallium nitride, indium phosphide, etc. In some circumstances, and in particular when the trapping layer 3a has a sufficient thickness, for example greater than 10 micrometres, the base substrate 2 may have a standard resistivity, of less than 1 kohm.cm.

In order to seek to preserve the properties of the trapping layer 3a during the heat treatments to which the carrier 1 may be subjected, provision may possibly be made for an amorphous layer, made of silicon dioxide for example, directly interposed between the base substrate 2 and the trapping layer 3a. When the base substrate 2 is made of silicon, this amorphous layer may be a native oxide layer present on the surface of this substrate or formed intentionally by chemical or thermal oxidation of the base substrate. However, the trapping layer 3a according to the present description is particularly temperature-stable, and the presence of the amorphous layer is perfectly optional.

The trapping layer 3a may have a thickness of between 10 nm and 50 micrometres. Preferentially, this thickness is less than 2 microns, or even less than 1 micron, in order to limit the quantity of material and any stresses that this layer may apply to the carrier 1 and which could deform it. However, this advantageous range of thickness is in no way limiting and it will be possible to choose to form a trapping layer 3a of any suitable thickness, depending on the needs of the intended application.

According to another aspect, the invention relates to a method of selecting a carrier. This method comprises a first step of providing a carrier comprising a base substrate and a trapping layer 3a of polycrystalline silicon disposed on the base substrate.

This provision step consists in forming, by any means known per se, the trapping layer 3a. This may involve HTCVD (High-Temperature Chemical Vapour Deposition) or else PECVD (Plasma-Enhanced Chemical Vapour Deposition). It may also involve LPCVD (Low-Pressure Chemical Vapour Deposition). These depositions may be made from any suitable silicon precursor gas, such as silane, dichlorosilane, trichlorosilane or TEOS (tetraethyl orthosilicate). In all cases, the trapping layer 3a comprises electrical traps which may be of a variety of types.

Experiments that have been carried out showed that the same deposition technique, but deploying precursors of different nature (for example dichlorosilane and trichlorosilane), led to the formation of trapping layers having different performance levels. Analysis of the traps present in these layers showed that they were very distinct from one layer to another, this confirming the benefit of a characterization method according to the invention.

In a subsequent step of the method which is the subject of the present description, a step of characterizing the trapping layer 3a is implemented. This step comprises measuring the activation energy and the effective hole and/or electron capture cross section of the electrical traps of the trapping layer.

This characterization step also comprises identifying different types of electrical traps present in the trapping layer, and in particular types T1 to T7 described in a previous section.

Finally, the method comprises a step of selecting the carrier 1, during which this carrier 1 is selected if the trapping layer 3a has electrical traps of the first type and of the second type.

Advantageously, during this selection step, a carrier 1 is retained only if the trapping layer 3a is free of electrical traps of the third type. Even more advantageously, a carrier is retained only if the trapping layer 3a further comprises electrical traps of the fourth type and of the fifth type, and if it is free of electrical traps of the sixth type and of the seventh type.

A selected carrier 1 may advantageously be used in a layer-transfer process aiming to transfer a thin crystalline film 4 onto the charge-trapping layer 3a or onto a dielectric layer 3b formed on this layer 3a. This film may in particular consist of or comprise silicon, silicon carbide, or a III-V or piezoelectric material.

Needless to say, the invention is not limited to the embodiments described, and implementation variants may be applied thereto without departing from the scope of the invention as defined by the claims

CLAIMS

1. Carrier (1) for a composite substrate (S), the carrier comprising a base substrate and a trapping layer (3a) of polycrystalline silicon disposed on the base substrate (2), the carrier (1) being characterized in that the trapping layer has electrical traps of a first type and of a second type, the electrical traps of the first type having an activation energy of 0.383 eV to within 0.008 eV and an effective capture cross section for holes and for electrons that is less than 10^{-16} cm^2 , the electrical traps of the second type having an activation energy of 0.428 eV to within 0.016 eV and an effective capture cross section for holes and for electrons that is less than 10^{-16} cm^2 .
2. Carrier (1) according to the preceding claim, wherein the electrical traps of the first type have an effective capture cross section for holes that is $1.7 \cdot 10^{-17}$ to within $0.1 \cdot 10^{-17}$ and an effective capture cross section for electrons that is $5.4 \cdot 10^{-17}$ to within $0.2 \cdot 10^{-17}$.
3. Carrier (1) according to either of the preceding claims, wherein the electrical traps of the second type have an effective capture cross section for electrons that is $1.8 \cdot 10^{-17}$ to within $1.1 \cdot 10^{-17}$ and an effective capture cross section for holes that is $5.7 \cdot 10^{-17}$ to within $3.7 \cdot 10^{-18}$.
4. Carrier (1) according to one of the preceding claims, wherein the trapping layer is free of electrical traps of a third type, the electrical traps of the third type having an activation energy of 0.485 eV to within 0.015 eV and an effective capture cross section for holes and for electrons that is greater than 10^{-16} cm^2 .

5. Carrier (1) according to the preceding claim, wherein the electrical traps of the third type have an effective capture cross section for electrons that is $1.0 \cdot 10^{-15}$ to within $0.1 \cdot 10^{-15}$ and an effective capture cross section for holes that is $3.3 \cdot 10^{-16}$ to within $0.2 \cdot 10^{-16}$.
6. Carrier (1) according to one of the preceding claims, wherein the trapping layer further comprises electrical traps of a fourth type and of a fifth type, the electrical traps of the fourth type having an activation energy of 0.392 eV to within 0.018 eV and an effective capture cross section for holes and for electrons that is less than 10^{-16} cm^2 , the electrical traps of the fifth type having an activation energy of 0.371 eV to within 0.025 eV and an effective capture cross section for holes and for electrons that is less than 10^{-16} cm^2 .
7. Carrier (1) according to the preceding claim, wherein the electrical traps of the fourth type have an effective capture cross section for electrons that is $3.8 \cdot 10^{-17}$ to within $0.3 \cdot 10^{-17}$ and an effective capture cross section for holes that is $1.2 \cdot 10^{-17}$ to within $0.1 \cdot 10^{-17}$.
8. Carrier (1) according to either of the two preceding claims, wherein the electrical traps of the fifth type have an effective capture cross section for electrons that is $6.9 \cdot 10^{-17}$ to within $0.7 \cdot 10^{-17}$ and an effective capture cross section for holes that is $2.2 \cdot 10^{-17}$ to within $0.2 \cdot 10^{-17}$.
9. Carrier (1) according to one of the preceding claims, wherein the trapping layer is free of electrical traps of a sixth type and of a seventh type, the electrical traps of the sixth type having an activation energy of 0.474 eV to within 0.032 eV and an effective capture cross section for

holes that is greater than 10^{-16} cm^2 , the electrical traps of the seventh type having an activation energy of 0.416 eV to within 0.017 eV and an effective capture cross section for holes that is greater than 10^{-16} cm^2 .

10. Carrier (1) according to the preceding claim, wherein the electrical traps of the sixth type have an effective capture cross section for holes that is $5.2 \cdot 10^{-16}$ to within $0.5 \cdot 10^{-16}$.
11. Carrier (1) according to either of the two preceding claims, wherein the electrical traps of the seventh type have an effective capture cross section for holes that is $1.7 \cdot 10^{-16}$ to within $0.1 \cdot 10^{-16}$.
12. Method of selecting a carrier (1), the method comprising:
 - a step of providing the carrier comprising a base substrate and a trapping layer (3a) of polycrystalline silicon disposed on the base substrate, the trapping layer comprising electrical traps;
 - a characterization step comprising measuring an activation energy and an effective hole and/or electron capture cross section of the electrical traps of the trapping layer, the characterization step also comprising identifying different types of electrical traps present in the trapping layer;
 - a selection step during which the carrier (1) is selected if the trapping layer has electrical traps of a first type and of a second type, the electrical traps of the first type having an activation energy of 0.383 eV to within 0.008 eV and an effective capture cross section for holes and for electrons that is less than 10^{-16} cm^2 , the electrical traps of the second type

having an activation energy of 0.428 eV to within 0.016 eV and an effective capture cross section for holes and for electrons that is less than 10^{-16} cm².

13. Selection method according to Claim 12, wherein during the selection step the carrier (1) is selected if the trapping layer is also free of electrical traps of a third type, the electrical traps of the third type having an activation energy of 0.485 eV to within 0.015 eV and an effective capture cross section for holes and for electrons that is greater than 10^{-16} cm².
14. Selection method according to either of Claims 12 and 13, wherein during the selection step the carrier (1) is selected if the trapping layer also comprises electrical traps of a fourth type and of a fifth type, the electrical traps of the fourth type having an activation energy of 0.392 eV to within 0.018 eV and an effective capture cross section for holes and for electrons that is less than 10^{-16} cm², the electrical traps of the fifth type having an activation energy of 0.371 eV to within 0.025 eV and an effective capture cross section for holes and for electrons that is less than 10^{-16} cm².
15. Selection method according to one of Claims 12 to 14, wherein during the selection step the carrier (1) is selected if the trapping layer is also free of electrical traps of a sixth type and of a seventh type, the electrical traps of the sixth type having an activation energy of 0.474 eV to within 0.032 eV and an effective capture cross section for holes that is greater than 10^{-16} cm², the electrical traps of the seventh type having an activation energy of 0.416 eV to within 0.017 eV and an effective capture cross section for holes that is greater than 10^{-16} cm².