CAPACITORLESS DRAM ON BULK SILICON

FIELD OF THE INVENTION

[0001] This invention relates generally to a localized silicon-on-insulator ("SOI") semiconductor design, and, more particularly, to the creation of localized oxide in the array of dynamic random access memories ("DRAM").

BACKGROUND OF THE INVENTION

[0002] Use of a silicon-on-insulator, or SOI, substrate generally enables the manufacture of typical circuit elements over an insulator, such as oxide. In one application, capacitorless DRAMs may be formed on SOI. Use of the SOI design versus a traditional silicon substrate increases the floating body effect for the access transistors of these capacitorless DRAMs, yielding far more effective storage. The programming of the floating bodies in such DRAMs may be done either by impact ionization ("II") or by gate induced drain leakage ("GIDL"). The sensing is non-destructive and is done using a resistance or current sensing method at a lower voltage. Further description of capacitorless DRAM via GIDL may be found in Yoshida *et al.*, *A Design of a Capacitorless 1T-DRAM Cell Using Gate-induced Drain Leakage (GIDL) Current for Low-power and High-speed Embedded Memory*, *Technical Digest - International Electron Devices Meeting 2003*, pp. 913-916 (IEEE Cat. No. 03CH37457, 2003), the contents of which are incorporated herein in its entirety.

SUMMARY OF THE INVENTION

[0003] According to one embodiment of the invention, a method of forming capacitorless DRAM over localized silicon-on-insulator is disclosed. The method comprises the following steps: A silicon substrate is provided, and an array of silicon studs is defined within the silicon substrate. An insulator layer is defined atop at least a portion of the silicon substrate, and between the silicon studs. A silicon-over-insulator layer is defined surrounding the silicon studs atop the insulator layer, and a capacitorless DRAM is formed within and above the silicon-over-insulator layer.

[0004] According to another embodiment of the invention, a method of forming a memory chip is disclosed. The method comprises the following steps: A periphery region and a memory array region are defined on the memory chip. At least one silicon-over-insulator region is formed in the memory array region, without forming a

silicon-over-insulator region in the periphery region. At least one capacitorless DRAM is formed on and within the at least one silicon-over-insulator region.

[0005] According to another embodiment of the invention, a memory device is disclosed. The memory device comprises a source and a drain. The memory device further comprises a floating body formed between the source and the drain, the floating body defined within a localized silicon-over-insulator. The memory device further comprises a gate adjacent the floating body.

[0006] According to another embodiment of the invention, an integrated circuit is disclosed. The integrated circuit comprises a periphery region, and an array region. At least one localized silicon-over-insulator is formed within the array region. The integrated circuit further comprises a source and a drain formed within the array region. A floating body is formed between the source and the drain within the at least one localized silicon-over-insulator. The integrated circuit further comprises a gate adjacent the floating body.

[0007] According to another embodiment of the invention, a system is disclosed. The system comprises a source, and a first drain and a second drain. The system further comprises a first floating body formed between the source and the first drain, and a second floating body formed between the source and the second drain, the floating bodies defined within a localized silicon-over-insulator. The system further comprises a first gate adjacent the first floating body, and a second gate adjacent the second floating body.

[0008] According to one embodiment of the invention, a method of operating a capacitorless DRAM is disclosed. The method comprises the following steps: A floating body is placed in a first state, and the first state is detected by measuring a first current at a source of the capacitorless DRAM. The floating body is defined within a localized silicon-over-insulator.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figure 1 is a schematic cross-sectional view of a portion of a memory device on which a first step of a process for forming localized SOI according to one embodiment of the present invention has been performed.

[0010] Figure 2 illustrates the memory device of Figure 1 on which a second step of a process for forming localized SOI according to one embodiment of the present invention has been performed.

[0011] Figure 3 illustrates the memory device of Figure 1 on which a third step of a process for forming localized SOI according to one embodiment of the present invention has been performed.

[0012] Figure 4 illustrates the memory device of Figure 1 on which a fourth step of a process for forming localized SOI according to one embodiment of the present invention has been performed.

[0013] Figure 5 illustrates the memory device of Figure 1 on which a fifth step of a process for forming localized SOI according to one embodiment of the present invention has been performed.

[0014] Figure 6 illustrates a capacitorless DRAM built over the localized SOI substrate of Figure 5.

[0015] Figure 7 is a partial top-down plan view of the capacitorless DRAM of Figure 6.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0016] While the preferred embodiments of the present invention illustrate localized SOI in combination with capacitorless DRAM, it should be understood that these methods of forming localized SOI may be incorporated into the fabrication of other integrated circuits as well. In addition, while the following methods are described in terms of particular DRAM fabrication techniques, as would be well known to those of skill in the art, such techniques may be replaced by other methods of fabricating and modifying semiconductor materials.

[0017] SOI is typically created by a uniform layer transfer. Thus, in order to manufacture capacitorless DRAM over SOI, for example, the entire surface of the array and periphery of the memory device incorporates a SOI substrate. However, while the SOI is desirable within the array, where the insulator enhances floating body effects, it adversely affects performance of the chip in the periphery.

[0018] Moreover, the creation of SOI via layer transfer is a difficult, time-consuming and expensive process. The fusion of different silicon and insulative layers poses many technical problems and must be performed at particular temperatures under particular conditions.

[0019] Therefore, there is a need in the art to create localized areas of SOI by conventional semiconductor fabrication techniques while leaving the rest of the chip unmodified. There is a further need for a method of making capacitorless DRAM using

bulk silicon by conventional DRAM fabrication techniques. Thus, the advantages of capacitorless DRAM might be achieved without the expense and difficulty of creating SOI via layer transfer.

[0020] Figures 1 through 5 illustrate one method for forming localized SOI inexpensively and efficiently. According to this method, the SOI structure(s) may be formed solely within the array of a memory chip, leaving the periphery to be formed on and within a typical semiconductor substrate.

[0021] Although not shown in any figure, the following method of forming localized SOI may be performed using any typical substrate 10, often formed from a silicon wafer. In other embodiments, the substrate 10 may comprise other suitable materials (*e.g.*, other group III-IV materials), or epitaxial layers formed over single crystal wafers.

[0022] With reference initially to Figure 1, a thin, thermally-grown dielectric layer (not shown), comprising pad oxide in a preferred embodiment, is preferably first formed over the substrate 10. A hard mask layer 12, such as silicon nitride, may then be deposited over the substrate 10 and dielectric layer. The hard mask layer 12 may be formed by any well-known deposition process, such as sputtering, chemical vapor deposition (CVD) or spin-on deposition, among others. Although the hard mask layer 12 comprises silicon nitride in a preferred embodiment, it must be understood that it may also be formed from silicon oxide, for example, or other materials that can protect underlying substrate during a substrate etch and also withstand additional processing, as will be apparent from the fabrication steps described further below.

[0023] In a step also not illustrated in the figures, the hard mask layer 12 may then be patterned using a photoresist layer formed over the hard mask layer 12. The photoresist layer may be patterned to form a mask using conventional photolithographic techniques, and the hard mask layer 12 may be anisotropically etched through the patterned photoresist to obtain a plurality of hard mask islands 14 within the array region of the memory device. The photoresist layer may then be removed by conventional techniques, such as by using an oxygen-based plasma. In alternative embodiments, the hard mask layer 12 may be anisotropically etched to obtain a hard mask grid, which can generally provide similar functionality (namely, protecting portions of the substrate 10 that will serve to seed lateral epitaxial overgrowth) as the hard mask islands 14 discussed at length below.

[0024] As shown in Figure 1, which illustrates a cross-sectional view of a portion of the array, the silicon of the substrate 10 is then selectively etched back. The etch process selectively etches the substrate 10 relative to the material forming the hard mask layer 12. For example, a selective wet etch may be used that strips silicon relative to silicon nitride. In another embodiment, ion milling or reactive ion etching may be used. Thus, the array of the memory device becomes an array of silicon studs 16, preferably with one centered on each active area region. Each of these silicon studs 16 is defined beneath the hard mask islands 14. Meanwhile, at least a portion of the periphery of the memory device is preferably left untouched, protected by unpatterned regions of the hard mask 12.

[0025] In an alternative embodiment, only one silicon stud 16 need be formed for a plurality of active areas. For example, one silicon stud 16 may be formed for every five active areas. However, in such an embodiment, some of the steps below, such as the lateral epitaxial growth of silicon shown in Figure 3, may take much longer. As will be understood by the skilled artisan, steps not shown in the figures are typically performed to separate the active areas. For example, in one embodiment, a field oxide could be defined surrounding each active area to prevent interference between adjacent active areas. Separate field isolation steps, on the other hand, may be omitted where localized or pseudo-SOI is formed individually for each active area, as illustrated.

[0026] In Figure 2, the portions of the array stripped according to the steps above are shown filled by an insulator layer 18, preferably an oxide. In a preferred embodiment, the insulator layer 18 is blanket deposited over the array at least up to the height of the top surface of the silicon studs 16. After deposition of a sufficient amount of insulator, the excess that may have formed over the islands 14 and other portions of the device may be removed by any of a number of processes well-known to those of skill in the art. For example, the surface of the device may be planarized to the top surface of the hard mask islands 14, as shown in Figure 2. Any suitable planarization process, such as, for example, chemical mechanical polishing ("CMP"), may be used.

[0027] Thus, the array preferably comprises a plurality of silicon studs 16 surrounded by insulator 18, whereas the periphery will simply remain in its original configuration with a hard mask layer 12 overlying the dielectric layer (e.g., pad oxide, not shown) covering the substrate 10.

[0028] Turning to Figure 3, another masking process, such as that described above, may be used within the array to open the insulator layer 18 around the silicon studs 16, at least in the regions where active areas are desired. In the illustrated embodiment, each active area has its own trench 20, such that unetched portions of the insulator 18 between trenches 20 serve as field isolation. As described above, this process is preferably performed using photoresist patterned according to conventional photolithographic techniques, optionally with a hard mask. In a preferred embodiment, a selective etching process may then be used to selectively recess the insulator layer 18 relative to the hard mask layer 12 and substrate 10, thereby forming trenches 20 in the memory device surrounding the silicon studs 16. This etching process is preferably continued until the trench 20 within the insulator layer 18 achieves a depth greater than the height of the hard mask layer 12 but less than the height of the silicon studs 16, thereby exposing a portion of the silicon substrate 10 forming silicon studs 16. Preferably, the trench 20 has a depth between about 200 Å and 1,000 Å.

[0029] In a preferred embodiment, a few layers of silicon 22 may then be epitaxially grown from the silicon stud 16, using the silicon as a seed layer. As is well-known to those of skill in the art, the epitaxial growth produces silicon extensions 22 with the same crystalline structure as the silicon substrate 10. Preferably, selective epitaxy is employed to avoid the need for subsequent removal of polysilicon from the exposed oxide and nitride surfaces. Preferably between about 50 Å and 500 Å of silicon (or other semiconductor) is grown.

[0030] As shown in Figure 4, a layer of amorphous silicon 24 may then be deposited within the trench 20 formed around the silicon stud 16. In a preferred embodiment, the amorphous silicon 24 may be blanket deposited over the array, filling the trenches 20. After deposition of a sufficient amount of silicon, the excess may be removed by any of a number of processes well-known to those of skill in the art. As shown in Figure 4, the surface of the device is preferably planarized to the top surface of the hard mask islands 14. Any suitable planarization process, such as, for example, CMP, may be used. In another embodiment, the silicon extensions 22 may instead be extended by epitaxial deposition in order to fill the trenches 20. In still another arrangement, planarization may follow the crystallization step described below.

[0031] In a preferred embodiment, a thin oxide 23, shown in Figure 4, may then be grown over the surface of the silicon layer 24, which may further facilitate the

crystallization of the filler silicon 24 using the epitaxially deposited silicon extension 22 as a seed layer.

[0032] The preferred silicon and oxide deposition is followed by an annealing process, whereby the amorphous silicon 24 has a tendency to take on a crystalline orientation similar to that of the epitaxially grown silicon extensions 22. Preferably, the amorphous silicon 24 takes an ordered crystalline pattern. Such conversion is a species of solid phase epitaxy (SPE) known as epitaxial lateral overgrowth (ELO).

[0033] Finally, as shown in Figure 5, the hard mask islands 14 may be removed, and the silicon layer 24 (preferably now crystallized) may be recessed. In a preferred embodiment, a selective etch may be used that etches the silicon 24 and the hard mask layer 14 far more effectively than the insulator layer 18, thereby exposing the silicon stud 16 for further processing steps. Further selective epitaxial deposition can then be conducted to achieve the desired thickness. Alternatively, the whole wafer can be planarized.

[0034] According to the above-described process, a localized silicon-over-insulator may be formed using relatively inexpensive fabrication techniques on a conventional polysilicon substrate. Figures 6 and 7 show an arrangement where two memory cells share a single transistor source. In particular, these figures illustrate capacitorless DRAM formed on and within this SOI substrate. Of course, in other embodiments, other DRAM schemes are also contemplated

[0035] In Figure 6, a completed capacitorless DRAM structure is shown formed over localized SOI created according to the steps set forth above. As illustrated, the silicon stud 16 remains beneath the common source and is connected by contacts 26 to a conductive digit or bit line 28. The drains 30 are located at the farthest ends of the crystallized silicon layer 24 and are also electrically connected by contacts 32 with sense lines 34. Floating bodies 36 form part of the channels that separate the drains 30 and the source (at the top of the pillar 16) in the preferred embodiment, and these floating bodies 36 are directly adjacent an inner pair of word lines 38. This inner pair of word lines 38 preferably separates the source 16 and the drains 30, as may be seen in Figure 6, serving as dual gates. While referred to hereinabove as drains 30 and source 16, it will be understood that these are mere labels used for convenience and for ready comparison to traditional capacitor-based DRAM designs. The labels can be reversed; whether the

voltage is at a higher level at the source or the drain depends upon whether a read or a write operation is being performed, as described in more detail below.

[0036] The structure shown in Figure 6 may be formed according to a number of deposition, pattern and etch steps well known to those of skill in the art. While configured for capacitorless DRAM operation, the illustrated scheme, whereby two memory cells share a common bit line 28 and bit line contact 26, is otherwise similar to the scheme in U.S. Patent No. 6,660,584, issued to Tran, the disclosure of which is incorporated herein by reference in its entirety. The '584 patent describes a "$6F^2$" arrangement in which pairs of memory cells share a common bit line and source region with independent pairs of word lines, drains and capacitors. The process used to form the structure shown in Figure 6 will differ, of course, from that in U.S. Patent No. 6,660,584 to the extent that the structure of Figure 6 lacks capacitors.

[0037] Preferably, a gate oxide is first grown over the silicon layer, followed by a gate stack deposition and etching. The necessary doping implants may then be formed to define the source, drain and channel regions. Spacers 40 may be deposited and etched, in a typical spacer fabrication process well known to those of skill in the art, before some of the doping steps. The bit line and cell side junctions are then formed, followed by formation of the metallic contacts and bit lines. Sense regions and other metallic contacts may then also be formed. Such processes may be carried out in a number of ways, but the capacitorless DRAM thus formed is particularly effective as a result of its formation over localized SOI. As a result of the SOI, the floating bodies 36 function particularly well, isolated as they are within the insulator layer 18, and the devices of the periphery surrounding the array can be tied to the bulk substrate 10.

[0038] In a preferred embodiment, the capacitorless DRAM shown in Figure 6 operates using gate-induced drain leakage (GIDL) current, although in other embodiments impact ionization current may also be used. As would be well understood by those skilled in the art, capacitorless DRAM uses the floating bodies 36 to store information regarding the state of the transistor. In particular, in order to write a logical "1" value to the transistor shown in Figure 6, a "drain" 30 is placed at an elevated voltage relative to an adjacent gate (*i.e.*, one of the word lines 38). The voltages of the drain 30 and gate 38 are controlled by the sense lines 34 and the word lines 38 respectively. As a result of electron tunneling, electrons flow to the drain 30, while generated holes flow to the floating bodies 36 underlying the gates.

[0039] As the holes accumulate in a floating body 36, the threshold voltage of the transistor is reduced, and the source current is thereby increased. Thus, a digital oscilloscope may be used, typically during the design of the capacitorless DRAM, to measure the source current and thereby the state of the transistor. In the illustrated embodiment, this source current may be detected along the raised bit line 28. In order to write a logical "0" value to one of the transistors, the adjacent gate takes an elevated voltage relative to the drain 30. Thus, the holes in the floating body 36 are forced out, the threshold voltage increases again, and the source current is reduced. Again, a digital oscilloscope may be used to detect this change in source current in determining appropriate operational thresholds. More information regarding how such capacitorless DRAM functions may be found in the article cited and incorporated above written by Eijiag Yoshida and Tetsu Tanaka.

[0040] As illustrated, each active area of the capacitorless DRAM forms part of a pair of memory cells comprising two floating bodies 36, and a transistor having a single source 16 shared by the memory cells, two gates and two drains 30. The pair of memory cells, therefore, has two addressable locations, the floating bodies 36, that can each store one bit of data. This preferred embodiment functions generally as described above. However, in one application, the pair of memory cells may provide redundancy because, if either of the floating bodies 36 is storing a "1" bit, the source current at the bit line 28 is elevated. Thus, in one embodiment, the read and write operations using the illustrated pair of memory cells will take place simultaneously to both floating bodies 36, thereby reducing errors.

[0041] Alternatively, the pair of memory cells may have three possible states. In one state, both floating bodies 36 store a "0" bit, and the source current through the conductive line 28 is at its lowest level. In a second state, one and only one of the floating bodies 36 stores a "1" bit, and the source current through the bit line 28 is at a higher level. Note that in this second state, the elevated source current through the bit line 28 yields only the information that one of the floating bodies 36 is storing a "1" bit, and does not indicate which of the floating bodies 36 is in this elevated state. In a third state, both of the floating bodies 36 store a "1" bit, and the source current through the bit line 28 is at its highest level. Thus, a sensitive oscilloscope, for example, will be able to differentiate between these three states.

[0042] A schematic plan view of this capacitorless DRAM is shown in Figure 7. Of course, this capacitorless DRAM design is shown by way of example only, and the localized SOI method described above with reference to Figures 1-5 may be used in any number of semiconductor environments.

[0043] While certain embodiments of the inventions have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the invention. Indeed, the novel methods and devices described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and devices described herein may be made without departing from the spirit of the invention. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the invention.

WE CLAIM:

1. A method of forming capacitorless DRAM over localized silicon-on-insulator, the method comprising:

providing a silicon substrate;

defining an array of silicon studs within the silicon substrate;

defining an insulator layer atop a portion of the silicon substrate, and between the silicon studs;

defining a silicon-over-insulator layer surrounding the silicon studs atop the insulator layer; and

forming at least one capacitorless DRAM cell within and above the silicon-over-insulator layer, wherein one silicon-over-insulator layer is formed for every two capacitorless DRAM cells.

2. The method of claim 1, wherein defining the array of silicon studs comprises etching the silicon substrate using photolithographic techniques.

3. The method of claim 1, wherein defining the insulator layer comprises:

depositing an insulator material over the silicon substrate to a height at least equal to a height of the silicon studs; and

planarizing the insulator material and silicon substrate.

4. The method of claim 3, wherein defining the silicon-over-insulator layer comprises:

etching at least a portion of the insulator layer surrounding the silicon studs to define trenches surrounding the silicon studs; and

exposing at least some silicon material comprising the silicon studs.

5. The method of claim 4, wherein defining the silicon-over-insulator layer further comprises:

depositing silicon extensions adjacent sidewalls of the silicon studs by selective epitaxy.

6. A method of forming capacitorless DRAM over localized silicon-on-insulator, the method comprising:

providing a silicon substrate;

defining an array of silicon studs within the silicon substrate;

defining an insulator layer atop at least a portion of the silicon substrate, and between the silicon studs;

defining a silicon-over-insulator layer surrounding the silicon studs atop the insulator layer; and

forming a capacitorless DRAM within and above the silicon-over-insulator layer;

wherein defining the insulator layer comprises depositing an insulator material over the silicon substrate to a height at least equal to a height of the silicon studs, and planarizing the insulator material and silicon substrate;

wherein defining the silicon-over-insulator layer comprises etching at least a portion of the insulator layer surrounding the silicon studs to define trenches surrounding the silicon studs, exposing at least some silicon material comprising the silicon studs, and depositing silicon extensions adjacent sidewalls of the silicon studs by selective epitaxy; and

wherein defining the silicon-over-insulator layer further comprises depositing additional silicon within the trenches and converting the additional silicon by lateral epitaxial overgrowth.

7. The method of claim 4, wherein defining the silicon-over-insulator layer further comprises:

depositing silicon within the trenches and converting the silicon by lateral epitaxial overgrowth.

8. The method of claim 6, wherein forming the capacitorless DRAM comprises:

forming a common source shared by a pair of memory cells, the memory cells further comprising two floating bodies, two gates and two drains.

9. The method of claim 8, wherein forming the capacitorless DRAM further comprises:

forming the two floating bodies within the silicon-over-insulator layer.

10. A method of forming a memory chip, the method comprising:

defining a periphery region and a memory array region on the memory chip;

forming at least one silicon-over-insulator region in the memory array region, without forming a silicon-over-insulator region in at least part of the periphery region; and

forming at least one capacitorless DRAM cell on and within the at least one silicon-over-insulator region;

wherein one silicon-over-insulator region is formed for every two DRAM cells in the memory array region.

forming the two floating bodies within the silicon-over-insulator layer.

11. The method of claim 10, wherein forming the at least one capacitorless DRAM cell further comprises defining at least one floating body within the at least one silicon-over-insulator region.

12. The method of claim 11, wherein forming the at least one capacitorless DRAM cell further comprises defining a single, shared source in the memory array region for every two floating bodies.

13. The method of claim 10 where forming at least one silicon-over-insulator region comprises forming a silicon 60 layer over an insulator by lateral epitaxial overgrowth.

14. The method of claim 13, wherein forming at least one silicon-over-insulator region further comprises forming a silicon pillar protruding through the insulator prior to lateral epitaxial overgrowth.

15. The method of claim 14, wherein forming at least one silicon-over-insulator region comprises etching a recess with the pillar therein and depositing the insulator into the recess.

16. The method of claim 14, further comprising recessing the insulator such that the pillar protrudes above the insulator prior to lateral epitaxial overgrowth.

17. The method of claim 10 wherein forming the capacitorless DRAM cell comprises defining two floating bodies within the silicon-over-insulator region, wherein the two floating bodies share a common source.

18. A method of forming a memory chip, the method comprising:

defining an active region on the memory chip;

forming a silicon pillar in the active region;

filling a trench surrounding the silicon pillar with an insulating layer;

recessing the insulating layer to expose an upper portion of the silicon pillar;

forming epitaxial silicon over the recessed insulating layer around the silicon pillar, wherein forming epitaxial silicon comprises growing about 50Å and 500Å of silicon over the recessed insulating layer;

forming at least one capacitorless DRAM cell on and within the epitaxial silicon; defining two floating bodies within the epitaxial silicon;

defining a single, common source at the top of the silicon pillar for every two floating bodies, wherein each floating body separates the common source from a drain; and

defining a bit line connected to the common source.

19. The method of claim 18, further comprising defining word lines adjacent to the floating bodies, wherein the word lines separate the common source from a drain.

20. A method of forming capacitorless DRAM over localized silicon-on-insulator, the method comprising:

providing a silicon substrate;

defining an array of silicon studs within the silicon substrate;

defining an insulator layer atop a portion of the silicon substrate, and between the silicon studs;

defining a plurality of silicon-over-insulator layers atop the insulator layer, each of the silicon-over-insulator layers surrounding a corresponding one of the silicon studs such that each of the silicon studs extends through the insulator layer from the silicon substrate to the corresponding silicon-over-insulator layer; and

forming a plurality of capacitorless DRAM cells, each of the capacitorless DRAM cells formed within and above a corresponding one of the silicon-over-insulator layers.

21. The method of Claim 20, wherein defining the array of silicon studs comprises etching the silicon substrate using photolithographic techniques.

22. The method of Claim 20, wherein defining the insulator layer comprises:

depositing an insulator material over the silicon substrate to a height at least equal to a height of the silicon studs; and

planarizing the insulator material and silicon substrate.

23. The method of Claim 20, wherein defining the silicon-over-insulator layers comprises:

etching at least a portion of the insulator layer between the silicon studs to define trenches surrounding each silicon stud; and

exposing at least some silicon material comprising the silicon studs.

24. The method of Claim 23, wherein defining the silicon-over-insulator layers further comprises:

depositing silicon extensions adjacent sidewalls of each silicon stud by selective epitaxy.

25. The method of Claim 23, wherein defining the silicon-over-insulator layers further comprises:

depositing silicon within the trenches and converting the silicon by lateral epitaxial overgrowth.

26. The method of Claim 20, wherein forming the capacitorless DRAM cells comprises:

for each silicon-over-insulator layer, forming a common source shared by a pair of memory cells, the memory cells further comprising two floating bodies, two gates and two drains.

27. The method of Claim 26, wherein forming the capacitorless DRAM cells further comprises:

forming the two floating bodies within each silicon-over-insulator layer.

28. A method of forming capacitorless DRAM, the method comprising:

providing a silicon substrate;

defining an insulator layer atop a portion of the silicon substrate;

defining a silicon-over-insulator structure atop at least a portion of the silicon substrate wherein the silicon-over-insulator structure surrounds a silicon stud such that the silicon stud extends through the insulator layer from the silicon substrate to the silicon-over-insulator structure; and

forming a capacitorless DRAM within and above the silicon-over-insulator structure.

29. The method of Claim 28, wherein forming the capacitorless DRAM comprises defining two floating bodies within the silicon-over-insulator structure, wherein the two floating bodies share a common source.

30. The method of Claim 28, wherein defining the silicon-over-insulator structure comprises forming silicon epitaxial extensions laterally over a deposited insulator by laterally extending single crystal silicon from the silicon stud.

31. A system, comprising:

a silicon substrate;

an insulator layer positioned over a portion of the silicon substrate;

a localized silicon-over-insulator layer positioned over and laterally surrounded by the insulator layer;

a semiconductor stud extending through the insulator layer from the silicon substrate to the silicon-over-insulator layer;

a source;

a first drain and a second drain;

a first floating body formed between the source and the first drain, and a second floating body formed between the source and the second drain, the floating bodies defined within the localized silicon-over-insulator layer, wherein the insulator surrounds the source; and

a first gate adjacent the first floating body, and a second gate adjacent the second floating body;

wherein at least one capacitorless DRAM cell is formed within and above the silicon-over-insulator layer.

32. The system of claim 31, wherein the first and second floating bodies are redundant.

33. The system of claim 32, wherein the source is configured to conduct a current having values indicative of three states, the three states comprising:

a first state, in which the first and second floating bodies store a "0" bit;

a second state, in which one of the first and second floating bodies stores a "0" bit, and the other of the first and second floating bodies stores a "1" bit; and

a third state, in which the first and second floating bodies store a "1" bit, and wherein the second and third states are not differentiated upon detection of the current.

34. The system of claim 33, wherein the first floating body is configured to attain the first state when the first drain is placed at a first elevated voltage relative to the first gate.

35. The system of claim 34, wherein the first floating body is configured to attain the second state when the first gate is placed at a second elevated voltage relative to the first drain.

36. The system of claim 35, wherein the first state causes an increased source current at the source, and the second state causes a decreased source current at the source.

37. The system of claim 32, wherein the floating bodies operate by gate-induced drain leakage currents.

38. The system of claim 31, wherein the source is configured to conduct a current having values indicative of three states, the three states comprising:

a first state, in which the first and second floating bodies store a "0" bit;

a second state, in which one of the first and second floating bodies stores a "0" bit, and the other of the first and second floating bodies stores a "1" bit; and

a third state, in which the first and second floating bodies store a "1" bit, and wherein the second and third states are not differentiated upon detection of the current.

39. The system of claim 38, wherein the first floating body is configured to attain the first state when the first drain is placed at a first elevated voltage relative to the first gate.

40. The system of claim 39, wherein the first floating body is configured to attain the second state when the first gate is placed at a second elevated voltage relative to the first drain.

41. The system of claim 40, wherein the first state causes an increased source current at the source, and the second state causes a decreased source current at the source.

42. The system of claim 38, wherein the floating bodies operate by gate-induced drain leakage currents.

43. The system of claim 38, wherein the second floating body is configured to attain the first state when the second drain is placed at a first elevated voltage relative to the second gate.

44. The system of claim 43, wherein the second floating body is configured to attain the second state when the second gate is placed at a second elevated voltage relative to the second drain.

45. The system of claim 44, wherein the first state causes an increased source current at the source, and the second state causes a decreased source current at the source.

46. A system comprising:

a silicon substrate;

an insulator layer positioned over a portion of the silicon substrate;

a localized silicon-over-insulator layer positioned over and surrounded by the insulator layer;

a semiconduetor stud extending through the insulator layer from the silicon substrate to the silicon-over-insulator layer;

a source;

a drain;

a floating body formed between the source and the drain, the floating body defined within the localized silicon-over-insulator layer, wherein the insulator surrounds the source; and

a gate adjacent the floating body;

wherein at least one capacitorless DRAM cell is formed within and above the silicon-over-insulator layer.