CLAIMS:

1. An electronics package, comprising:

an interposer comprising silicon, the interposer comprising vias, a first lateralmost sidewall and a second lateralmost sidewall, wherein the vias provide connections between pads on a bottom of the interposer and a redistribution layer on a top of the interposer, and wherein the first lateralmost sidewall is opposed the second lateralmost sidewall of the interposer;

at least one cavity passing through the top and the bottom of the interposer, and located between the first and the second lateralmost sidewalls of the interposer;

a first die over the interposer, the first die coupled to the redistribution layer of the interposer by first interconnects;

a second die over the interposer and laterally spaced apart from the first die, the second die coupled to the redistribution layer of the interposer by second interconnects;

a first mold layer between the first die and the interposer and between the second die and the interposer, the first mold layer laterally between and in contact with the first die and the second die, and the first mold layer in contact with the first interconnects and with the second interconnects;

bumps on the pads on the bottom of the interposer and vertically beneath the vias of the interposer, the bumps vertically beneath the first die and vertically beneath the second die; and

a second mold layer beneath the interposer and in contact with the first lateralmost sidewall of the interposer, the second mold layer in contact with the bumps and with the pads on the bottom of the interposer.

2. The electronics package of claim 1, wherein the first mold layer has an uppermost surface at a same level as an uppermost surface of the first die.

3. The electronics package of claim 2, wherein the uppermost surface of the first mold layer is at a same level as an uppermost surface of the second die.

4. The electronics package of claim 1, wherein the second mold layer is in contact with a second lateralmost sidewall of the interposer.

5. The electronics package of claim 1, wherein the second mold layer has an edge in vertically alignment with an edge of the first mold layer.

6. The electronics package of claim 1, further comprising:

an underfill material between the interposer and the first mold layer.

7. The electronics package of claim 6, wherein the second mold layer is in contact with less than an entirety of the first lateralmost sidewall of the interposer, and with less than an entirety of the second lateralmost sidewall of the interposer.

8. A method of fabricating an electronics package, the method comprising:

coupling a first die to a redistribution layer of an interposer with first interconnects, the interposer comprising:

vias,

a first lateralmost sidewall,

a second lateralmost sidewall,

wherein the first lateralmost sidewall is opposed the second lateralmost sidewall,

wherein at least one cavity passes through a top and a bottom of the interposer, and is located between the first and the second lateralmost sidewalls of the interposer, and

wherein the vias provide connections between pads on the bottom of the interposer and the redistribution layer on the top of the interposer;

coupling a second die to the redistribution layer of the interposer with second interconnects;

forming a first mold layer between the first die and the interposer and between the second die and the interposer, the first mold layer laterally between and in contact with the first die and the second die, and the first mold layer in contact with the first interconnects and with the second interconnects;

forming bumps on the pads on the bottom of the interposer and vertically beneath the vias of the interposer, the bumps vertically beneath the first die and vertically beneath the second die; and

forming a second mold layer beneath the interposer and in contact with the first lateralmost sidewall of the interposer, the second mold layer in contact with the bumps and with the pads on the bottom of the interposer.

9. The method of claim 8, wherein the first mold layer has an uppermost surface at a same level as an uppermost surface of the first die.

10. The method of claim 9, wherein the uppermost surface of the first mold layer is at a same level as an uppermost surface of the second die.

11. The method of claim 8, wherein the second mold layer is in contact with a second lateralmost sidewall of the interposer.

12. The method of claim 8, wherein the second mold layer has an edge in vertically alignment with an edge of the first mold layer.

13. The method of claim 8, further comprising:

forming an underfill material between the interposer and the first mold layer.

14. The method of claim 13, wherein the second mold layer is in contact with less than an entirety of the first lateralmost sidewall of the interposer, and with less than an entirety of the second lateralmost sidewall of the interposer.

15. An electronic system, comprising:

a board;

a package substrate coupled to the board; and

an electronics package coupled to the package substrate, the electronics package comprising:

an interposer comprising silicon, the interposer comprising vias, a first lateralmost sidewall and a second lateralmost sidewall, wherein the vias provide connections between pads on a bottom of the interposer and a redistribution layer on a top of the interposer, and wherein the first lateralmost sidewall is opposed to the second lateralmost sidewall of the interposer;

at least one cavity passing through the top and the bottom of the interposer, and located between the first and the second lateralmost sidewalls of the interposer;

a first die over the interposer, the first die coupled to the redistribution layer of the interposer by first interconnects;

a second die over the interposer and laterally spaced apart from the first die, the second die coupled to the redistribution layer of the interposer by second interconnects;

a first mold layer between the first die and the interposer and between the second die and the interposer, the first mold layer laterally between and in contact with the first die and the second die, and the first mold layer in contact with the first interconnects and with the second interconnects;

bumps on the pads on the bottom of the interposer and vertically beneath the vias of the interposer, the bumps vertically beneath the first die and vertically beneath the second die; and

a second mold layer beneath the interposer and in contact with the first lateralmost sidewall of the interposer, the second mold layer in contact with the bumps and with the pads on the bottom of the interposer.

16. The electronic system of claim 15, further comprising:
a battery coupled to the board.

17. The electronic system of claim 15, further comprising:
a camera coupled to the board.

18. The electronic system of claim 15, further comprising:
a display coupled to the board.

19. The electronic system of claim 15, further comprising:
a Global Positioning System coupled to the board.

20. The electronic system of claim 15, further comprising:
a communication chip coupled to the board.