

**METHODS FOR FORMING A SILICON SUBSTRATE WITH REDUCED
GROWN-IN NUCLEI FOR EPITAXIAL DEFECTS AND METHODS
FOR FORMING AN EPITAXIAL WAFER**

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of U.S. Provisional Patent Application No. 63/112,424, filed November 11, 2020, which is incorporated herein by reference in its entirety.

FIELD OF THE DISCLOSURE

[0002] The field of the disclosure relates to preparation of single crystal silicon substrates for epitaxial growth and to methods for forming an epitaxial wafer.

BACKGROUND

[0003] Epitaxial wafers include a single crystal silicon substrate with an epitaxial layer deposited on the front surface of the substrate. Epitaxial wafers may be used to form electronic devices suitable in microelectronic (integrated circuits or power applications) or photovoltaic use.

[0004] Epitaxial wafers may have surface defects which degrade their performance. Some defects formed in the silicon substrate are not dissolved during the epitaxial process and are believed to lead to grown-in defect sites in the epitaxial layer (e.g., epi-stacking faults or "hillocks") following epitaxial deposition. Defect propagation through the epitaxial layer is believed to cause these grown-in defects to form. A thicker epitaxial layer, instead of covering the substrate defects, enlarges the size of the starting substrate

surface defects due to the silicon epitaxial growth mode along <111> crystallographic planes, causing larger and more visible epitaxial defects to form with increasing epitaxial layer thickness.

[0005] A need exists for methods for reducing the number of grown-in nuclei for epitaxial defects in substrate wafers and for related methods for forming an epitaxial wafer.

[0006] This section is intended to introduce the reader to various aspects of art that may be related to various aspects of the disclosure, which are described and/or claimed below. This discussion is believed to be helpful in providing the reader with background information to facilitate a better understanding of the various aspects of the present disclosure. Accordingly, it should be understood that these statements are to be read in this light, and not as admissions of prior art.

SUMMARY

[0007] One aspect of the present disclosure is directed to a method for forming a silicon substrate with reduced grown-in nuclei for epitaxial defects. The silicon substrate is boron doped at a concentration of at least 2.8×10^{18} atoms/cm³. An initial charge of polycrystalline silicon is added to a crucible. The crucible comprising the initial charge of polycrystalline silicon is heated to cause a silicon melt to form in the crucible. Boron is added to the crucible to produce a doped silicon melt. A silicon seed crystal is contacted with the doped silicon melt. The silicon seed crystal is withdrawn to grow a single crystal silicon ingot having a constant diameter

portion. A segment of the constant diameter portion of the ingot has a boron concentration of at least about 2.8×10^{18} atoms/cm³. When the segment has a boron concentration from 2.8×10^{18} atoms/cm³ to 5.4×10^{18} atoms/cm³, (i) a growth velocity, v , and/or (ii) an axial temperature gradient, G , is controlled during the growth of the segment such that v/G is less than $0.20 \text{ mm}^2/(\text{min} \cdot \text{K})$. When the segment has a boron concentration from 5.4×10^{18} atoms/cm³ to 8.0×10^{18} atoms/cm³, (i) a growth velocity, v , and/or (ii) an axial temperature gradient, G , is controlled during the growth of the segment such that v/G is less than $0.25 \text{ mm}^2/(\text{min} \cdot \text{K})$. When the segment has a boron concentration greater than 8.0×10^{18} atoms/cm³, (i) a growth velocity, v , and/or (ii) an axial temperature gradient, G , are operated at any value of v/G . The segment of the constant diameter portion of the ingot is cooled from its solidification temperature to 950°C or less. The dwell time the segment of the constant diameter portion of the ingot is in the temperature range from 1150°C to 950°C is less than 160 minutes.

[0008] Yet another aspect of the present disclosure is directed to a method for forming a silicon substrate with reduced grown-in nuclei for epitaxial defects. An initial charge of polycrystalline silicon is added to a crucible. The crucible comprising the initial charge of polycrystalline silicon is heated to cause a silicon melt to form in the crucible. Boron is added to the crucible to prepare a doped silicon melt having a boron concentration of at least 3.8×10^{18} atoms/cm³. A silicon seed crystal is contacted with the doped silicon melt. The silicon seed crystal is withdrawn to grow a single crystal silicon ingot. The ingot has a constant diameter portion. The method further includes controlling (i) a growth velocity,

v, and/or (ii) an axial temperature gradient, G, during the growth of a segment of the constant diameter portion of the ingot such that the ratio v/G is less than a critical v/G . The segment of the constant diameter portion of the ingot is cooled from its solidification temperature to 950°C or less. The dwell time the segment of the constant diameter portion of the ingot is in the temperature range from 1150°C to 950°C is less than 160 minutes.

[0009] Various refinements exist of the features noted in relation to the above-mentioned aspects of the present disclosure. Further features may also be incorporated in the above-mentioned aspects of the present disclosure as well. These refinements and additional features may exist individually or in any combination. For instance, various features discussed below in relation to any of the illustrated embodiments of the present disclosure may be incorporated into any of the above-described aspects of the present disclosure, alone or in any combination.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 is a cross-section of an ingot puller apparatus before silicon ingot growth;

[0011] FIG. 2 is a cross-section of an ingot puller apparatus of Figure 1 during silicon ingot growth;

[0012] FIG. 3 are schematic cross-section views of a single crystal silicon ingot showing the axial trend in vacancy-rich and interstitial-rich regions for three boron doping levels (increasing from (a) to (c));

[0013] FIG. 4 is a graph of epitaxial defect counts as a function of the axial position of the substrate wafer in the single crystal ingot with a relatively long time in the temperature range from 1150°C to 950°C;

[0014] FIG. 5 is a graph of epitaxial defect counts as a function of the axial position of the substrate wafer in the single crystal ingot with a relatively short time in the temperature range from 1150°C to 950°C;

[0015] FIG. 6 is a graph of the defect counts as a function of dwell time the ingot segment in the temperature range from 1150°C to 950°C; and

[0016] FIG. 7 is a graph of the dwell time over the crystal length for various single crystal silicon ingots.

[0017] Corresponding reference characters indicate corresponding parts throughout the drawings.

DETAILED DESCRIPTION

[0018] Provisions of the present disclosure relate to methods for forming a silicon substrate with reduced grown-in nuclei for epitaxial defects (i.e., defects that occur after epitaxial silicon growth on a silicon substrate). In accordance with embodiments of the present disclosure, the ratio (v/G) of the growth velocity (v) and the axial temperature gradient (G) may be controlled during growth of a segment or all of the constant diameter portion of the ingot and the period of time at which the segment is at the temperature range from 1150°C to 950°C is controlled to be 160 minutes or less to reduce the nuclei that lead to defects during epitaxial

growth. The resulting substrate is suitable for epitaxial silicon growth with the epitaxial layer grown on the substrate having reduced or being substantially free of grown-in defects.

[0019] The methods of the present disclosure may generally be carried out in any ingot puller apparatus that is configured to pull a single crystal silicon ingot. An example ingot puller apparatus (or more simply "ingot puller") is indicated generally at "100" in FIG. 1. The ingot puller apparatus 100 includes a crucible 102 for holding a melt 104 of semiconductor or solar-grade material, such as silicon, supported by a susceptor 106. The ingot puller apparatus 100 includes a crystal puller housing 108 that defines a growth chamber 152 for pulling a silicon ingot 113 (Fig. 2) from the melt 104 along a pull axis A.

[0020] The crucible 102 includes a floor 129 and a sidewall 131 that extends upward from the floor 129. The sidewall 131 is generally vertical. The floor 129 includes the curved portion of the crucible 102 that extends below the sidewall 131. Within the crucible 102 is a silicon melt 104 having a melt surface 111 (i.e., melt-ingot interface).

[0021] In some embodiments, the crucible 102 is layered. For example, the crucible 102 may be made of a quartz base layer and a synthetic quartz liner disposed on the quartz base layer.

[0022] The susceptor 106 is supported by a shaft 105. The susceptor 106, crucible 102, shaft 105 and

ingot 113 (Fig. 2) have a common longitudinal axis A or "pull axis" A.

[0023] A pulling mechanism 114 is provided within the ingot puller apparatus 100 for growing and pulling an ingot 113 from the melt 104. Pulling mechanism 114 includes a pulling cable 118, a seed holder or chuck 120 coupled to one end of the pulling cable 118, and a silicon seed crystal 122 coupled to the seed holder or chuck 120 for initiating crystal growth. One end of the pulling cable 118 is connected to a pulley (not shown) or a drum (not shown), or any other suitable type of lifting mechanism, for example, a shaft, and the other end is connected to the chuck 120 that holds the seed crystal 122. In operation, the seed crystal 122 is lowered to contact the melt 104. The pulling mechanism 114 is operated to cause the seed crystal 122 to rise. This causes a single crystal ingot 113 (FIG. 2) to be withdrawn from the melt 104.

[0024] During heating and crystal pulling, a crucible drive unit 107 (e.g., a motor) rotates the crucible 102 and susceptor 106. A lift mechanism 112 raises and lowers the crucible 102 along the pull axis A during the growth process. For example, as shown in Figure 1, the crucible 102 may be at a lowest position (near the bottom heater 126) in which an initial charge of solid-phase polycrystalline silicon previously added to the crucible 102 is melted. Crystal growth commences by contacting the melt 104 with the seed crystal 122 and lifting the seed crystal 122 by the pulling mechanism 114. As the ingot grows, the silicon melt 104 is consumed and the height of the melt in the crucible 102 decreases. The

crucible 102 and susceptor 106 may be raised to maintain the melt surface 111 at or near the same position relative to the ingot puller apparatus 100 (FIG. 2).

[0025] A crystal drive unit (not shown) may also rotate the pulling cable 118 and ingot 113 (FIG. 2) in a direction opposite the direction in which the crucible drive unit 107 rotates the crucible 102 (e.g., counter-rotation). In embodiments using iso-rotation, the crystal drive unit may rotate the pulling cable 118 in the same direction in which crucible drive unit 107 rotates the crucible 102. In addition, the crystal drive unit raises and lowers the ingot 113 relative to the melt surface 111 as desired during the growth process.

[0026] The ingot puller apparatus 100 may include an inert gas system to introduce and withdraw an inert gas such as argon from the growth chamber 152. The ingot puller apparatus 100 may also include a dopant feed system (not shown) for introducing dopant into the melt 104.

[0027] According to the Czochralski single crystal growth process, a quantity of polycrystalline silicon, or polysilicon, is charged to the crucible 102. The initial semiconductor or solar-grade material that is introduced into the crucible is melted by heat provided from one or more heating elements to form a silicon melt in the crucible. The ingot puller apparatus 100 includes bottom insulation 110 and side insulation 124 to retain heat in the puller apparatus. In the illustrated embodiment, the ingot puller apparatus 100 includes a bottom heater 126 disposed below the crucible floor 129. The crucible 102 may be moved to be in relatively close

proximity to the bottom heater 126 to melt the polycrystalline charged to the crucible 102.

[0028] To form the ingot, the seed crystal 122 is contacted with the surface 111 of the melt 104. The pulling mechanism 114 is operated to pull the seed crystal 122 from the melt 104. Referring now to Figure 2, the ingot 113 includes a crown portion 142 in which the ingot transitions and tapers outward from the seed crystal 122 to reach a target diameter. The ingot 113 includes a constant diameter portion 145 or cylindrical "main body" of the crystal which is grown by increasing the pull rate. The main body 145 of the ingot 113 has a relatively constant diameter. The ingot 113 includes a tail or end-cone (not shown) in which the ingot tapers in diameter after the main body 145. When the diameter becomes small enough, the ingot 113 is then separated from the melt 104.

[0029] The ingot puller apparatus 100 includes a side heater 135 and a susceptor 106 that encircles the crucible 102 to maintain the temperature of the melt 104 during crystal growth. The side heater 135 is disposed radially outward to the crucible sidewall 131 as the crucible 102 travels up and down the pull axis A. The side heater 135 and bottom heater 126 may be any type of heater that allows the side heater 135 and bottom heater 126 to operate as described herein. In some embodiments, the heaters 135, 126 are resistance heaters. The side heater 135 and bottom heater 126 may be controlled by a control system (not shown) so that the temperature of the melt 104 is controlled throughout the pulling process.

[0030] The ingot puller apparatus 100 may include a heat shield 151. The heat shield 151 may shroud

the ingot 113 and may be disposed within the crucible 102 during crystal growth (FIG. 2).

[0031] In some embodiments, the silicon substrate that is produced by the methods described herein is doped (e.g., relatively heavily doped) with boron. For example, the silicon melt may be doped with boron to produce a doped silicon ingot having a boron concentration of at least 2.8×10^{18} atoms/cm³. Boron doping of the melt at a concentration of at least 3.8×10^{18} atoms/cm³ may be used to achieve an ingot with a concentration of at least 2.8×10^{18} atoms/cm³ at the seed end. The resulting ingot (and sliced wafers) may have a concentration of boron of at least 2.8×10^{18} atoms/cm³. In some embodiments, the melt is not doped with carbon (and in some embodiments no dopant other than boron is used).

[0032] In accordance with embodiments of the present disclosure, a silicon substrate having a reduced amount of grown-in nuclei for epitaxial defects or even a substrate substantially free of such grown-in nuclei may be produced by (1) controlling the ratio of the crystal pull-rate (v) to the magnitude of the axial temperature gradient (G) in the vicinity of the melt-crystal interface and (2) controlling the period of time (i.e., dwell time) at which the segment is at the temperature range from 1150°C to 950°C to be 160 minutes or less.

[0033] By controlling the ratio of v/G during silicon growth, the type of dominant defect may be controlled. At a higher v/G , the convection of the point defects dominates their diffusion, and vacancies remain the incorporated dominant point defects, as the vacancy concentration at the interface is higher than the

interstitial concentration. At a lower v/G , the diffusion dominates the convection, allowing the incorporation of the fast diffusing interstitials as the dominant point points. At a v/G close to its critical value (i.e., the transition between vacancy and interstitial dominated material), both the point defects are incorporated in very low and comparable concentrations.

[0034] In accordance with embodiments of the present disclosure, (i) a growth velocity, v , and/or (ii) an axial temperature gradient, G , may be controlled during the growth of an axial segment of the constant diameter portion of the ingot such that the ratio v/G is below the critical value of v/G to cause vacancy concentrations in the ingot to be reduced (or even controlled to be less than a value slightly above the critical v/G).

[0035] The critical v/G generally changes based on the amount of boron doping. Boron shifts the equilibrium to the interstitial regime. With increasing boron concentration (i.e., decreasing resistivity), the vacancy-dominated region shrinks until it disappears entirely at the crystal center (FIG. 3C). In boron doped ingots, it is believed that the vacancy-dominated region may be eliminated at boron doping greater than 8.0×10^{18} atoms/cm³ (e.g., resistivity of less than 10 mΩ*cm) at all ratios of v/G .

[0036] For boron concentrations of 8.0×10^{18} atoms/cm³ or less, v/G may be controlled to be below the critical v/G (or even below a value that is slightly above the critical v/G). In accordance with some embodiments of the present disclosure, when the segment of the constant diameter portion of the ingot has a boron concentration

from 2.8×10^{18} atoms/cm³ to 5.4×10^{18} atoms/cm³, (i) the growth velocity, v , and/or (ii) the axial temperature gradient, G , is controlled such that v/G is less than $0.20 \text{ mm}^2/(\text{min} \cdot \text{K})$. When the segment of the constant diameter portion of the ingot has a boron concentration from 5.4×10^{18} atoms/cm³ to 8.0×10^{18} atoms/cm³, (i) the growth velocity, v , and/or (ii) the axial temperature gradient, G , is controlled during the growth of the segment such that v/G is less than $0.25 \text{ mm}^2/(\text{min} \cdot \text{K})$.

[0037] As noted above, when the segment is doped at a concentration of greater than 8.0×10^{18} atoms/cm³, v/G need not be controlled as interstitials are the dominant point defect throughout the segment over all ranges of v/G (i.e., any technologically feasible v/G may be used).

[0038] As v/G is generally highest at the center of the ingot, the ranges of v/G provided herein are generally measured at the center of the ingot to ensure that v/G is below the upper limit across the entire radius of the ingot.

[0039] As the ingot is withdrawn from the melt, the ingot cools from solidification (about 1412°C) to room temperature. In accordance with embodiments of the present disclosure, during growth of the ingot and control of v/G (v/G being controlled for boron doping at 8.0×10^{18} atoms/cm³ or less, i.e., resistivities above $10 \text{ m}\Omega \cdot \text{cm}$), the cooling rate of the ingot is controlled such that the dwell time at which the segment (e.g., each portion of the segment) is in the temperature range from 1150°C to 950°C is minimized. In this regard, all ingots may be controlled in this manner regardless of the boron doping

concentration. In accordance with some embodiments, the cooling rate of the ingot is controlled such that the period of time at which the segment is in the temperature range from 1150°C to 950°C is less than 160 minutes.

[0040] The hot zone of the ingot puller may be arranged and/or modified to achieve such a cooling rate through this range of temperatures (e.g., cooling rate at least 1.25°C/minute, at least 1.5°C/minute, at least 2.0°C/min, at least 2.5°C/min, at least 3.0°C/min, or at least 3.5°C/min through the 1150°C to 950°C temperature range). Hot zones that may achieve such cooling may include any combination of one or more of the following: (1) active cooling elements (e.g., water cooling) near the ingot surface, (2) increasing thermal insulation between the crystal surface and the melt to reduce heat radiation from the melt to the crystal, (3) application of a jet of cold inert gas near the melt-ingot interface, (4) use of a conical heat shield (e.g., reflective material such as molybdenum) that surrounds the ingot to reflect heat irradiated by the ingot toward the ingot puller apparatus walls. In other embodiments, the cooling rate of the ingot is controlled such that the period of time at which the segment is in the temperature range from 1150°C to 950°C is less than 120 minutes, less than 90 minutes or less than 60 minutes.

[0041] As noted above, v/G may be controlled such that interstitials are the dominant intrinsic point defect and with the cooling rate being controlled such that the ingot segment is in the temperature range from 1150°C to 950°C for less than 160 minutes for at least a segment (e.g., axial segment) of the ingot. This segment of the

ingot may have a length that is at least 0.5 times the length (D) of the constant diameter portion of the ingot ($0.5 \cdot D$). In other embodiments, the length of the segment is at least $0.75 \cdot D$ or at least $0.9 \cdot D$. In some embodiments, the segment is the entire constant diameter portion of the ingot.

[0042] Once the ingot has been grown, the ingot is sliced into substrates (i.e., wafers). The resulting wafers have a reduced amount of grown-in nuclei for epitaxial defects that form during epitaxial growth.

[0043] Once the wafers have been sliced from the ingot and processed (e.g., various smoothing and/or reduction in surface roughness), an epitaxial layer may be deposited on the front surface of the substrate by contacting the front surface with a silicon-containing gas that decomposes and forms an epitaxial silicon layer on the substrate. Generally, any of the methods available to those of skill in the art for depositing a silicon epitaxial layer on a silicon substrate may be used unless stated otherwise. Silicon may be deposited by epitaxy to any suitable thickness depending on the device application. For example, the silicon may be deposited using metalorganic chemical vapor deposition (MOCVD), physical vapor deposition (PVD), chemical vapor deposition (CVD), low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), or molecular beam epitaxy (MBE). Silicon precursors (i.e., silicon-containing gases) for LPCVD or PECVD include methyl silane, silicon tetrahydride (silane), trisilane, disilane, pentasilane, neopentasilane, tetrasilane, dichlorosilane (SiH_2Cl_2), trichlorosilane (SiHCl_3), silicon tetrachloride

(SiCl₄), among others. For example, silicon may be deposited onto the surface oxidation layer by pyrolyzing silane (SiH₄) in a temperature range between about 550°C and about 690°C, such as between about 580°C and about 650°C. The chamber pressure may range from about 70 to about 400 mTorr.

[0044] A boron-containing gas may be introduced into the epitaxial reactor to dope the epitaxial layer with boron. In some embodiments, the resulting epitaxial structure (i.e., substrate and epitaxial layer) is doped with boron at concentrations sufficient to achieve a p/p+ epitaxial wafer. The epitaxial layer may have a reduced number of grown-in defects or may be substantially free of grown-in defects.

[0045] Compared to other methods for forming a substrate for silicon epitaxial growth and methods for forming an epitaxial wafer, the methods of the present disclosure have several advantages. Heavily doping the substrate with boron (e.g., a boron concentration of 2.8×10^{18} atoms/cm³ or more) has been found to suppress the formation of interstitial-type dislocation loops. Heavily doping the substrate with boron has also been found to enhance oxygen precipitation. In vacancy rich regions, oxygen precipitation is further enhanced (i.e. larger precipitates form). Enhancement increases with higher vacancy concentrations. It is believed that grown-in defects in the epitaxial layer deposited on a substrate heavily-doped with boron are significantly caused by large oxygen precipitates at the surface of the single crystal silicon substrate upon which the epitaxial layer is grown. These large oxygen precipitates, which may be associated with dislocation loops or tangles, are not dissolved during

the epitaxial process and are believed to lead to defect sites in the epitaxial layer (e.g., epi-stacking faults or "hillocks") following epitaxial deposition. By keeping v/G below the critical value (or in a slight excess) in the relatively heavily-doped substrate, vacancies are eliminated or reduced, respectively, which suppresses the formation of relatively large oxygen precipitates which do not dissolve during epitaxial deposition. Thus it may be seen that relatively high boron doping with control of v/G below threshold values thereby reduces defects attributable to interstitials and vacancies.

[0046] In embodiments in which the ingot segment has a boron concentration of greater than 8.0×10^{18} atoms/cm³, the segment is fully interstitial rich and any ratio of v/G may be used. By controlling the ratio of v/G instead of only the pull rate v , process productivity may be preserved (e.g., by use of hot zone configured to provide high values of the thermal gradient G).

[0047] By minimizing the time the ingot segment is in the temperature range from 1150°C to 950°C (e.g., a dwell time of 160 minutes or less), defects may be further reduced or eliminated regardless of the v/G value, even if vacancies are present.

EXAMPLES

[0048] The processes of the present disclosure are further illustrated by the following Examples. These Examples should not be viewed in a limiting sense.

Example 1: Axial Trends in Vacancy-Rich and Interstitial-Rich Regions of a Silicon Ingot at Different Boron Doping Levels

[0049] Figure 3 is a cross-section schematic view of a single crystal silicon ingot showing the axial trend in vacancy-rich and interstitial-rich regions for three boron doping levels. Figure 3(a) shows the axial trend of the vacancy-rich and interstitial-rich regions for a silicon crystal heavily doped with boron (e.g., relatively light doping at 2.8×10^{18} atoms/cm³ which corresponds to a target resistivity at the seed end of 22 mΩ*cm which is a typical specification for heavily boron doped silicon substrates). In the crystal of Figure 3(a), at the crystal seed end, the vacancy-rich region extends across the entire crystal radius, from center to edge, and shrinks gradually along the crystal length as the boron concentration increases axially due to the dopant segregation. At the V/I boundary, the position of the OISF ring is also shown. The OISF ring vanishes where the vacancy-rich region shrinks completely.

[0050] Figure 3(b) shows the axial trend of the vacancy-rich and interstitial-rich regions for a silicon crystal heavily doped with boron to an intermediate concentration (e.g., relatively intermediate doping at 4.5×10^{18} atoms/cm³ at the seed end which corresponds to a target resistivity at the seed end of 16 mΩ*cm which is a resistivity that represents a typical intermediate resistivity specification for heavily boron doped silicon substrates). In this example, the vacancy-rich region extends only until a certain distance from the center even at the crystal seed end. The vacancy-rich region gradually shrinks along the crystal length as the boron concentration

increases axially due to the dopant segregation and vanishes completely at some axial position. At the V/I boundary, the position of the OISF ring is also shown. The OISF ring vanishes where the vacancy-rich region shrinks completely.

[0051] Figure 3(c) shows the axial trend of the vacancy-rich and interstitial-rich regions for a silicon crystal heavily doped with boron (e.g., relatively high doping at 8.0×10^{18} atoms/cm³ at the seed end which corresponds to a target resistivity at the seed end of about 10 mΩ*cm which is a typical resistivity specification for heavily boron doped crystals used to cover the common p++ range of 5-10 mΩ*cm). The defect pattern of Figure 3(c) does not change for even lower resistivities such as 5 mΩ*cm. No vacancy-rich region is present and the crystal is fully interstitial rich. No OISF ring forms. At this high doping level, no impact of the v/G ratio is observed and it can be concluded that the defect nature is fully determined by the dopant concentration alone.

Example 2: Comparison of Epitaxial Defect Counts between Wafers from an Ingot Segment with a Relatively Long Time and a Relatively Short Time in the Temperature Range from 1150°C to 950°C

[0052] Figure 4 is a graph of epitaxial defect counts measured by a laser inspection tool as a function of the axial position of the substrate wafer in the single crystal ingot with a relatively long time in the temperature range from 1150°C to 950°C (labeled as "Example 1"). The data points to the left of Figure 4 are for crystals which were heavily doped with boron at relatively light doping (e.g., 2.8×10^{18} atoms/cm³) as shown in Figure 3(a). The data points to the right of Figure 4 are for

crystals which were heavily doped with boron at relatively intermediate doping (e.g., 4.5×10^{18} atoms/cm³) as shown in Figure 3(b).

[0053] Figure 5 is a graph of epitaxial defect counts measured by a laser inspect tool as a function of the axial position of the substrate wafer in the single crystal ingot with a relatively short time in the temperature range from 1150°C to 950°C (labeled as "Example 2"). The data points to the left of Figure 5 are for crystals which were heavily doped with boron at relatively light doping (e.g., 2.8×10^{18} atoms/cm³) as shown in Figure 3(a). The data points to the right of Figure 5 are for crystals which were heavily doped with boron at relatively intermediate doping such as (e.g., 4.5×10^{18} atoms/cm³) as shown in Figure 3(b).

[0054] As shown in Figures 4 and 5, shortening the period of time in the temperature range from 1150°C to 950°C reduced the number of defects, particularly for more lightly doped substrates.

[0055] The defect counts of Figures 4 and 5 are shown in Figure 6 as a function of dwell time the ingot segment in the temperature range from 1150°C to 950°C. Ingot segments with excess vacancy concentration are shown in rhombs and segments grown under a relatively lower vacancy concentration are shown by crosses. As shown in Figure 6, the epitaxial defects depend on the dwell time the ingot segment is in the temperature range from 1150°C to 950°C

[0056] Figure 7 shows the dwell time of various ingot segments in the temperature range between

1150°C to 950°C. Relatively low cooling is indicated as "Example 1" and relatively fast cooling is indicated as "Example 2". An ingot segment having a boron concentration of $4.32\text{--}4.61 \times 10^{18}$ atoms/cm³ and an oxygen concentration of 6.25×10^{17} atoms/cm³ was selected. v/G of the segment at its center was about 0.25 mm²/(min*K) which was more than the 0.20 mm²/(min*K) range specified above for the boron concentration of the segment. A segment having a 180 minute dwell time between 1150°C and 950°C was chosen. The segment was sliced in wafers and a silicon epitaxial layer was grown on the front surface of each substrate. The epitaxial wafers were measured by a laser inspection tool to determine the defect count. The average epitaxial defect count was 16 per wafer, much higher than the defect count of 3 per wafer that was achieved by embodiments of the present disclosure (see, e.g., FIGS. 5 and 6 and Table 1 below).

[0057] Figure 7 also shows data used to prepare Figure 4 ("Example 1") and Figure 5 ("Example 2").

Example 3: Defect Counts as a Function of v/G

[0058] Table 1 shows the boron concentration, oxygen concentration target, and dwell time spent in the temperature range from 1150°C to 950°C in the crystal segment for various test lots. An epitaxial silicon layer was deposited on each substrate and the epitaxial defect counts as measured with laser inspection tools were measured. In Table 1, "high" excess vacancies indicates that v/G was higher than the v/G ranges specified above (v/G was greater than 0.20 mm²/(min*K) for boron concentrations from 2.8×10^{18} atoms/cm³ to 5.4×10^{18} atoms/cm³ and was greater than 0.25 for boron concentrations

from 5.4×10^{18} atoms/cm³ to 8.0×10^{18} atoms/cm³). "Low" excess vacancies indicate that v/G was less than the v/G ranges specified above (v/G was less than 0.20 mm²/(min*K) for boron concentrations from 2.8×10^{18} atoms/cm³ to 5.4×10^{18} atoms/cm³ and was less than 0.25 for boron concentrations from 5.4×10^{18} atoms/cm³ to 8.0×10^{18} atoms/cm³).

Test Lot Number	Excess Vacancy Conc.	Boron Conc. (Lot Range) [at/cm ³]	Oxygen Conc. (target) [at/cm ³]	Dwell time 1150-950°C [min]	Epitaxial defect counts
1	high	$(4.60-4.75) \times 10^{18}$	6.45×10^{17}	128	< 3
2	high	$(4.67-4.81) \times 10^{18}$	6.25×10^{17}	128	< 3
3	high	$(4.32-4.61) \times 10^{18}$	6.25×10^{17}	160	>15
4	high	$(4.44-5.00) \times 10^{18}$	6.25×10^{17}	130	>5
5	high	$(4.51-5.19) \times 10^{18}$	6.45×10^{17}	132	>5
6	low	$(6.05-6.42) \times 10^{18}$	6.25×10^{17}	127	< 3
7	low	$(6.91-7.52) \times 10^{18}$	6.25×10^{17}	129	< 3
8	low	$(8.89-10.60) \times 10^{18}$	6.25×10^{17}	132	< 3
9	low	$(8.83-10.40) \times 10^{18}$	6.25×10^{17}	132	< 3
10	low	$(7.76-9.58) \times 10^{18}$	6.25×10^{17}	158	< 3
11	low	$(7.46-8.89) \times 10^{18}$	6.25×10^{17}	152	< 3
12	high	$(4.68-4.77) \times 10^{18}$	6.45×10^{17}	45	< 3
13	high	$(4.51-4.62) \times 10^{18}$	6.25×10^{17}	40	< 3
14	high	$(4.90-5.11) \times 10^{18}$	6.45×10^{17}	43	< 3
15	high	$(4.82-4.90) \times 10^{18}$	6.45×10^{17}	31	< 3
16	high	$(4.68-4.88) \times 10^{18}$	6.25×10^{17}	31	< 3
17	low	$(5.83-6.07) \times 10^{18}$	6.25×10^{17}	47	< 3
18	low	$(5.95-6.11) \times 10^{18}$	6.25×10^{17}	41	< 3
19	low	$(6.75-8.12) \times 10^{18}$	6.25×10^{17}	32	< 3

Table 1: Defect Counts as a Function of v/G (i.e., excess vacancy concentration)

[0059] As shown in Table 1, low defect counts may be achieved when the excess vacancy concentration is low or when the dwell time in the temperature range from

1150°C to 950°C is low (or a combination of these conditions).

[0060] As used herein, the terms "about," "substantially," "essentially" and "approximately" when used in conjunction with ranges of dimensions, concentrations, temperatures or other physical or chemical properties or characteristics is meant to cover variations that may exist in the upper and/or lower limits of the ranges of the properties or characteristics, including, for example, variations resulting from rounding, measurement methodology or other statistical variation.

[0061] When introducing elements of the present disclosure or the embodiment(s) thereof, the articles "a", "an", "the" and "said" are intended to mean that there are one or more of the elements. The terms "comprising," "including," "containing" and "having" are intended to be inclusive and mean that there may be additional elements other than the listed elements. The use of terms indicating a particular orientation (e.g., "top", "bottom", "side", etc.) is for convenience of description and does not require any particular orientation of the item described.

[0062] As various changes could be made in the above constructions and methods without departing from the scope of the disclosure, it is intended that all matter contained in the above description and shown in the accompanying drawing[s] shall be interpreted as illustrative and not in a limiting sense.

WHAT IS CLAIMED IS:

1. A method for forming a silicon substrate with reduced grown-in nuclei for epitaxial defects, the silicon substrate being boron doped at a concentration of at least 2.8×10^{18} atoms/cm³, the method comprising:

adding an initial charge of polycrystalline silicon to a crucible;

heating the crucible comprising the initial charge of polycrystalline silicon to cause a silicon melt to form in the crucible;

adding boron to the crucible to produce a doped silicon melt;

contacting a silicon seed crystal with the doped silicon melt;

withdrawing the silicon seed crystal to grow a single crystal silicon ingot, the ingot having a constant diameter portion;

wherein a segment of the constant diameter portion of the ingot has a boron concentration of at least about 2.8×10^{18} atoms/cm³; and

when the segment has a boron concentration from 2.8×10^{18} atoms/cm³ to 5.4×10^{18} atoms/cm³, (i) a growth velocity, v , and/or (ii) an axial temperature gradient, G , is controlled during the growth of the segment such that v/G is less than $0.20 \text{ mm}^2/(\text{min} \cdot \text{K})$;

when the segment has a boron concentration from 5.4×10^{18} atoms/cm³ to 8.0×10^{18} atoms/cm³, (i) a growth velocity, v , and/or (ii) an axial temperature gradient, G , is controlled during the growth of the segment such that v/G is less than $0.25 \text{ mm}^2/(\text{min} \cdot \text{K})$;

when the segment has a boron concentration greater than 8.0×10^{18} atoms/cm³, (i) a growth velocity, v , and/or (ii) an axial temperature gradient, G , are operated at any value of v/G ; and

cooling the segment of the constant diameter portion of the ingot from its solidification temperature to 950°C or less, wherein the dwell time the segment of the constant diameter portion of the ingot is in the temperature range from 1150°C to 950°C is less than 160 minutes.

2. The method as set forth in claim 1 wherein the constant diameter portion has a length D , the length of the segment being at least $0.5 \cdot D$, at least $0.75 \cdot D$, at least $0.9 \cdot D$ or the segment is the entire constant diameter portion of the ingot.

3. The method as set forth in claim 1 or claim 2 wherein the dwell time the segment of the constant diameter portion of the ingot is in the temperature range from 1150°C to 950°C is less than 120 minutes, less than 90 minutes or less than 60 minutes.

4. The method as set forth in any one of claims 1 to 3 wherein the segment has a boron concentration from 2.8×10^{18} atoms/cm³ to 5.4×10^{18} atoms/cm³.

5. The method as set forth in any one of claims 1 to 3 wherein the segment has a boron concentration from 5.4×10^{18} atoms/cm³ to 8.0×10^{18} atoms/cm³.

6. The method as set forth in any one of claims 1 to 3 wherein the segment has a boron concentration of greater than 8.0×10^{18} atoms/cm³.

7. The method as set forth in any one of claims 1 to 6 wherein the melt is not doped with carbon.

8. The method as set forth in any one of claims 1 to 7 further comprising slicing the single crystal silicon ingot into substrates.

9. A method for preparing an epitaxial structure, the method comprising:

forming a silicon substrate by the method of any one of claims 1 to 8; and

contacting a front surface of the silicon substrate with a silicon-containing gas, the silicon-containing gas decomposing to form an epitaxial silicon layer on the silicon substrate.

10. A method for forming a silicon substrate with reduced grown-in nuclei for epitaxial defects, the method comprising:

adding an initial charge of polycrystalline silicon to a crucible;

heating the crucible comprising the initial charge of polycrystalline silicon to cause a silicon melt to form in the crucible;

adding boron to the crucible to prepare a doped silicon melt having a boron concentration of at least 3.8×10^{18} atoms/cm³;

contacting a silicon seed crystal with the doped silicon melt;

withdrawing the silicon seed crystal to grow a single crystal silicon ingot, the ingot having a constant diameter portion;

controlling (i) a growth velocity, v , and/or (ii) an axial temperature gradient, G , during the growth of a segment of the constant diameter portion of the ingot such that the ratio v/G is less than a critical v/G ; and

cooling the segment of the constant diameter portion of the ingot from its solidification temperature to 950°C or less, wherein the dwell time the segment of the constant diameter portion of the ingot is in the temperature range from 1150°C to 950°C is less than 160 minutes.

11. The method as set forth in claim 10 wherein the constant diameter portion has a length D , the length of the segment being at least $0.5 \cdot D$, at least $0.75 \cdot D$, at least $0.9 \cdot D$ or the segment is the entire constant diameter portion of the ingot.

12. The method as set forth in claim 10 or claim 11 wherein the dwell time the segment of the constant diameter portion of the ingot is in the temperature range from 1150°C to 950°C is less than 120 minutes, less than 90 minutes or less than 60 minutes.

13. The method as set forth in any one of claims 10 to 12 wherein:

when the concentration of boron in the segment of the constant diameter portion is from 2.8×10^{18} atoms/ cm^3 to 5.4×10^{18} atoms/ cm^3 , the (i) a growth velocity, v , and/or (ii) an axial temperature gradient, G , is controlled such that v/G is less than $0.20 \text{ mm}^2/(\text{min} \cdot \text{K})$; and

when the concentration of boron in the segment of the constant diameter portion is from 5.4×10^{18} atoms/cm³ to 8.0×10^{18} atoms/cm³, the (i) a growth velocity, v , and/or (ii) an axial temperature gradient, G , is controlled such that v/G is less than $0.25 \text{ mm}^2/(\text{min} \cdot \text{K})$.

14. The method as set forth in any one of claims 10 to 13 wherein, when the concentration of boron in the segment of the constant diameter portion is greater than 8.0×10^{18} atoms/cm³, any technologically feasible value of v/G may be used.

15. The method as set forth in any one of claims 10 to 14 wherein the melt is not doped with carbon.

16. The method as set forth in any one of claims 10 to 15 further comprising slicing the single crystal silicon ingot into substrates.

17. A method for preparing an epitaxial structure, the method comprising:

forming a silicon substrate by the method of any one of claims 10 to 16; and

contacting a front surface of the silicon substrate with a silicon-containing gas, the silicon-containing gas decomposing to form an epitaxial silicon layer on the silicon substrate.