SOI DEVICE WITH REDUCED JUNCTION CAPACITANCE

FIELD OF THE INVENTION

The present invention relates to the field of silicon-on-insulator (SOI) field effect transistors (FETs); more specifically, it relates to an SOI FET having reduced junction area capacitance and the method of fabricating said device.

BACKGROUND OF THE INVENTION

In SOI technology, a thin silicon layer is formed over an insulating layer, such as silicon oxide, which in turn, is formed over a substrate. This insulating layer is often referred to as a buried oxide (BOX) layer or simply BOX. Transistor source and drains are formed, for example, by ion implantation of N and/or P dopant into the thin silicon layer with a body region between the source and drain. Gates are formed on top of the body region, for example, by deposition of a gate dielectric and conductor on a top surface of the thin silicon, followed by, photolithographic patterning, and etching.

FETs built in SOI technology have significant advantages over FETs built using bulk silicon technology. Among the advantages of SOI technology are reduced short channel effects, lower parasitic capacitance and increased drain on-current. However, as SOI FET dimensions are downscaled ever smaller to take advantage of, for example, reduced area junction capacitance of downscaled devices increases as the BOX is downscaled (thinned). Increased area junction capacitance causes device performance degradation.

Turning to FIG. 1, FIG. 1 is a partial cross-sectional view of an SOI FET illustrating the various active and parasitic capacitors. FET 100 comprises a silicon substrate 105, a BOX 110 formed on top of the substrate, and a thin silicon layer 115, formed on top of the BOX. FET 100 further comprises source/drains 120 formed in silicon layer 115 and a body region 125, also formed in the silicon layer, separating the source/drains. FET 100 still further comprises a gate dielectric 130, a gate conductor 135, and sidewall spacers 140 formed on sidewalls 145 of gate conductor 135. Extending from a top surface 150 of silicon layer

115, through the silicon layer, to BOX 110 is shallow trench isolation (STI) 155.

The active and parasitic capacitors are located as follows. A front-gate capacitor 160 exists between gate conductor 135 and body region 125. The dielectric for front- gate capacitor 160 is gate dielectric 130. Area junction capacitors 165 exist between each source/drain 120 and substrate 105. A back-gate capacitor 170 exists between body region 125 and substrate 105. The dielectric for area junction capacitors 165 and back- gate capacitor 170 is BOX 110. The capacitance of each of these capacitors is given by the well-known equation:

$$C = \frac{\mathcal{E}_0 \mathcal{E}_{ox}}{T_{ox}}$$

in which C is the capacitance, ϵ_o is the dielectric constant of free space, ϵ_{ox} is the dielectric constant of the dielectric and T_{ox} is the thickness of the dielectric. It is desirable for front-gate capacitor 160 to be large in order to increase the on-current and decrease the off-current. This is accomplished by either decreasing the thickness of gate dielectric 130 or by using a material with a high dielectric constant for the gate dielectric. It is desirable for area junction capacitors 165 to be small for reasons described above. However, it is desirable for back-gate capacitor 170 to be large at the same time. The reason a large back-gate capacitor 170 is desirable is to improve off-current control the threshold voltage control. Since the dielectric for area junction capacitors 165 and back- gate capacitor 170 is BOX 110, it is apparent that it is not possible to optimize the area junction capacitors and the back-gate capacitor at the same time.

FIG. 2 is a partial cross-sectional view of a double BOX SOI FET illustrating the various active and parasitic capacitors. The purpose of FIG. 2 is to illustrate that a double BOX SOI device still has the problem described above for a single BOX device. FET 200 comprises a silicon substrate 205, a thick first BOX 210 formed on top of the substrate, a thin first silicon layer 215, which is doped to about 10^{18} to 10^{19} atm/cm^3, formed on top of the first BOX, a thin second BOX 220 formed on top of the first silicon layer and a thin second silicon layer 225 formed on top of

the second BOX. FET 200 further comprises source/drains 230 formed in second silicon layer 225 and a body region 235, also formed in the second silicon layer, separating the source/drains. FET 200 still further comprises a gate dielectric 240, a gate conductor 245, and sidewall spacers 250 formed on sidewalls 255 of gate conductor 245. Extending from a top surface 255 of second silicon layer 225, through the second silicon layer, through second BOX 220, through first silicon layer 215 to first BOX 210 is STI 260.

The active and parasitic capacitors are located as follows. A front-gate capacitor 265 exists between gate 245 and body region 235. The dielectric for front-gate capacitor 265 is gate dielectric 240. Area junction capacitors 270 exist between each source/drain 230 and first silicon layer 215. A back-gate capacitor 275 exists between body region 235 and first silicon layer 215. The dielectric for area junction capacitors 270 and back- gate capacitor 275 is second BOX 220. A substrate capacitor 280 exists between first silicon layer 215 and substrate 205. The dielectric for substrate capacitor 280 is first BOX 210. While first BOX 210 may be thick to reduce the capacitance of substrate capacitor 280, again, since the dielectric for area junction capacitors 270 and back-gate capacitor 275 is second BOX 220, it is not apparent that it is possible to optimize the area junction capacitors and the back-gate capacitor at the same time.

Therefore, a method of fabricating an SOI FET having a small area junction capacitance and a large back-gate capacitance is required in order to obtain all the benefits of SOI technology when downscaling.

DISCLOSURE OF THE INVENTION

A first aspect of the present invention is a semiconductor structure comprising: a dielectric layer, the dielectric layer having a first and a second region, the first dielectric region having a first dielectric constant and the second dielectric region having a second dielectric constant different from the first dielectric constant.

A second aspect of the present invention is an SOI FET comprising: a silicon substrate having silicon layer on top of a buried oxide layer having doped regions and an undoped region, the undoped region having a dielectric constant different from a dielectric constant of the doped regions; source/drains in the silicon layer and separated by a body in the silicon layer, the source/drains aligned over the doped regions and the

body aligned over the undoped region; and a gate dielectric on top of the body and a gate conductor on top of the gate dielectric.

A third aspect of the present invention is a method of fabricating a semiconductor structure comprising: providing a dielectric layer; forming a first region in the dielectric layer, the first region having a first dielectric constant; and forming a second region in the second dielectric, the second region having a second dielectric constant different from the first dielectric constant.

A fourth aspect of the present invention is a method of fabricating an SOI FET comprising: providing a silicon substrate having silicon layer on top of a buried oxide layer; forming a gate dielectric on top of silicon layer; forming a gate conductor on top of the gate dielectric; forming source/drains in the silicon layer; the source drains separated by a body in the silicon layer, the body aligned under the gate; and forming doped regions in the buried oxide layer, the doped regions aligned under the source /drains and having a dielectric constant different from a dielectric constant of non-doped regions of the buried oxide layer.

BRIEF DESCRIPTION OF DRAWINGS

The features of the invention are set forth in the appended claims. The invention itself, however, will be best understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

FIG. 1 is a partial cross-sectional view of an SOI FET illustrating the various active and parasitic capacitors;

FIG. 2 is a partial cross-sectional view of a double BOX SOI FET illustrating the various active and parasitic capacitors;

FIGs. 3A through 3E are partial cross-sectional views illustrating the fabrication of an SOI FET according to a first embodiment of the present invention;

FIG. 4 is a partial cross-sectional view illustrating a double BOX SOI FET fabricated according to the first embodiment of the present invention;

FIGs. 5A through 5F are partial cross-sectional views illustrating the fabrication of an SOI FET according to a second embodiment of the present invention

FIG. 6 is a partial cross-sectional view illustrating a double BOX SOI FET fabricated according to the second embodiment of the present invention; and

FIG. 7 is a partial cross-sectional view illustrating the fabrication of an SOI FET according to a third embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to the drawings, FIGs. 3A through 3E are partial cross-sectional views illustrating the fabrication of an SOI FET device according to a first embodiment of the present invention. The fabrication method starts in FIG. 3A, with a silicon substrate 300 having a BOX 305 formed between a thin silicon layer 310 and the substrate. Extending from a top surface 315 of silicon layer 310, through the silicon layer, to BOX 305 is STI 320. STI 320 may be formed by a photolithographic step, followed by a reactive ion etch (RIE) of silicon substrate 300 to form a trench down to BOX 305, followed by deposition of an insulator to fill the trench so formed, followed by a chemical-mechanical-polish (CMP) process to planarize to form top surface 315. In one example, BOX 305 is formed by ion implantation of oxygen and comprises silicon oxide about 50 to 500 Å in thickness, and silicon layer 310 is 50 to 500 Å in thickness being either P or N doped to about 10^{16} to 10^{18} atm/cm^3. Formed on top of top surface 315 is a gate dielectric 325. In one example, gate dielectric 325 is silicon dioxide is formed by thermal oxidation or chemical vapor deposition (CVD) and is about 10 Å to 50 Å in thickness. In another example, gate dielectric 325 is silicon oxynitride formed by thermal oxidation followed by nitridation of the oxide by remote plasma nitration (RPN) or decoupled plasma nitridation (DPN.) In still another example, gate dielectric 325 is a high-K material such as aluminum oxide or hafnium oxide formed by CVD. Formed on top of gate dielectric 325 is gate conductor 330 and formed on top of the gate conductor is hard mask 335. In one example, gate conductor 330 is polysilicon formed by CVD and is about 500 Å to 2000 Å in thickness and hard mask 335 is silicon oxide, formed by oxidation or CVD, silicon nitride, formed by CVD or a combination thereof, and is 100 Å to 1000 Å in thickness. Hard mask 335 is used to prevent subsequent ion implantation processes, as illustrated in FIG. 3D, and described below from penetrating into gate conductor 330 or gate dielectric 325. Formed on hard mask 335 is photoresist 340. Photoresist 340 is patterned with an FET gate pattern and is aligned over silicon layer 310 between STI 320.

In FIG. 3B, the pattern of photoresist 340 is transferred to gate conductor 330 and hard mask 335 by an RIE process and then the photoresist is removed. Sidewall spacers 345 are formed on sidewalls 350 of gate 330/hard mask 335. Sidewall spacers 345 may be formed by conformal deposition of a dielectric followed by a RIE process. In one example, sidewall spacers 345 are silicon nitride and are about 100 to 2000 Å wide at the sidewall spacer 345/gate dielectric 325 interface 360.

In FIG. 3C, source/drains 365 have been formed in silicon layer 310 by ion implantation of either N or P dopant to a concentration of about 10^{19} to 10^{21} atm/cm^3 followed by a anneal process. Sidewall spacers 345 limit the extension of source/drains 365 under gate 330. The region of silicon layer 310 between source/drains 365 and under gate 330 is now a body region 370. Obviously, for a PFET, source/drain regions 365 are doped P type and body region 370 N type, while for an NFET, source/drain regions 365 are doped N type and body region 370 P type. It should be observed that FIG. 3C illustrates a fully depleted device, but could just as well illustrate a partially depleted device.

In FIG. 3D, a fluorine ion implantation is performed to produce fluorine rich oxide regions 375 in BOX 305. Sidewall spacers 345 limit the extension of fluorine rich oxide regions 375 under gate 330. The fluorine implantation is performed at an energy to place the implantation profile peak within BOX 305 and of sufficient dosage to lower the dielectric constant of BOX 305 by about 5 to 25% after the anneal step illustrated in FIG. 3E and described below. In one example, fluorine is implanted at a dose of about 1 X 10^{14} to 1 X 10^{17} atm/cm2 and energies of about 2 to 40 Kev.

In FIG. 3E, in order to activate the fluorine, an anneal of between 600 to 1100 °C under nitrogen or other inert gas is performed. Activation of the fluorine drives the fluorine into the silicon oxide lattice to produce fluorinated BOX 380. Fluorinated BOX 380 does not extend under body 370 any significant amount. In one example, BOX 305 has a dielectric constant of 3.9 and fluorinated BOX 380 has a dielectric constant of about 3.7 to 2.9. Referring to FIG. 1 and FIG. 3E, since T_{ox} for BOX 305 and fluorinated BOX 380 is the same but ϵ_{ox} of BOX 305 is higher than ϵ_{ox} of fluorinated BOX 380 it follows that the capacitance of the area junction capacitors formed from source/drains 365, fluorinated BOX 380 and

substrate 300 is lower than the capacitance of the back-gate capacitor formed from body 370, BOX 305 and substrate 300.

FIG. 4 is a partial cross-sectional view illustrating a double BOX SOI FET fabricated according to the first embodiment of the present invention and is similar to FIG 3E except for the addition of a second silicon layer 385 under BOX 305 and fluorinated BOX 380 and a second BOX 390 between the second silicon layer and substrate 300. In addition, STI 320 extends through fluorinated BOX 380, through second silicon layer 385 to second BOX 390.

FIGs. 5A through 5F are partial cross-sectional views illustrating the fabrication of an SOI FET according to a second embodiment of the present invention. FIGs. 5A through 5C are similar to FIGs. 3A through 3C described above. The fabrication method starts in FIG. 5A, with a silicon substrate 400 having a BOX 405 formed between a thin silicon layer 410 and the substrate. Extending from a top surface 415 of silicon layer 410, through the silicon layer, to BOX 405 is STI 420. In one example, BOX 405 comprises silicon oxide about 50 to 500 Å in thickness, and silicon layer 410 is 50 to 500 Å in thickness being either P or N doped to about 10^{15} to 10^{18} atm/cm^3. Formed on top of top surface 415 is a gate dielectric 425. In one example, gate dielectric 425 is silicon dioxide about 10 to 50 Å in thickness. Formed on top of gate dielectric 415 is gate conductor 430 and formed on top of gate conductor is hard mask 435. In one example, gate conductor 430 is polysilicon and is about 500 to 2000 Å in thickness and hard mask 435 is silicon oxide, silicon nitride or a combination thereof, and is 100 to 1000 Å in thickness. Hard mask 435 is used to prevent subsequent ion implantation processes, as illustrated in FIG. 5E, and described below from penetrating into gate conductor 430 or gate dielectric 425. Formed on hard mask 435 is photoresist 440. Photoresist 440 is patterned with an FET gate pattern and is aligned over silicon layer 410 between STI 420.

In FIG. 5C, source/drains 465 have been formed in silicon layer 410 by ion implantation of either N or P dopant to a concentration of about 10^{19} to 10^{21} atm/cm^3 followed by a anneal process. Sidewall spacers 445 limit the extension of source/drains 465 under gate 430. The region of silicon layer 410 between source/drains 465 and under gate 430 is now a body region 470. It should be observed that FIG. 5C illustrates a fully depleted device, but could just as well illustrate a partially depleted device.

In FIG. 5D, second sidewall spacers 475 are formed on sides 480 of first sidewall spacers 445. In one example, second sidewall spacers 475 are silicon nitride and are about 100 to 2000 Å wide at the second sidewall spacer 475/gate dielectric 425 interface 485.

In FIG. 5E, a fluorine ion implantation is performed to produce fluorine rich oxide regions 490 in BOX 405. The fluorine implantation is performed at an energy to place the implantation profile peak within BOX 405 and of sufficient dosage to lower the dielectric constant of BOX 405 by about 5 to 25% after the anneal step illustrated in FIG. 3E and described below. In one example, fluorine is implanted at a dose of about 1×10^{14} to 1×10^{17} atm/cm2 and energies of about 2 to 40 Kev.

In FIG. 5F, in order to activate the fluorine, an anneal of between 600 to 1100 °C under nitrogen or other inert gas is performed. Activation of the fluorine drives the fluorine into the silicon oxide lattice to produce fluorinated BOX 495. Fluorinated BOX 495 does not extend under body 470 any significant amount. In one example, BOX 405 has a dielectric constant of 3.9 and fluorinated BOX 495 has a dielectric constant of about 3.7 to 2.9. Referring to FIG. 2 and FIG. 5F, since T_{ox} for BOX 405 and fluorinated BOX 495 is the same but ϵ_{ox} of BOX 405 is higher than ϵ_{ox} of fluorinated BOX 495 it follows that the capacitance of the area junction capacitors formed from source/drains 465, fluorinated BOX 495 and substrate 400 is lower than the capacitance of the back-gate capacitor formed from body 470, BOX 405 and substrate 400.

FIG. 6 is a partial cross-sectional view illustrating a double BOX SOI FET fabricated according to the second embodiment of the present invention and is similar to FIG 5E except for the addition of a second silicon layer 500 under BOX 405 and fluorinated BOX 495 and a second BOX 505 between the second silicon layer and substrate 400. In addition, STI 420 extends through fluorinated BOX 495, through second silicon layer 500 to second BOX 505.

FIG. 7 is a partial cross-sectional view illustrating the fabrication of an SOI FET according to a third embodiment of the present invention. FIG. 7 is intended to replace the processes illustrated in FIG. 3D and described above. In addition, the steps for forming hard mask 335 are eliminated. In FIG. 7 a second photoresist layer 510 is formed on gate 330 and top surface 515 of gate dielectric 325. Photoresist 510 is

patterned with a slightly larger FET gate pattern than was illustrated in FIG. 3A and is aligned such that sidewalls 520 align over source/drains 365 between spacer 345 and STI 320. This embodiment is particularly well suited for large FET devices with long gate lengths.

Sidewalls 520 of second photoresist 510 limit the extension of fluorine rich oxide regions 375 under gate 330. The fluorine implantation is performed at an energy to place the implantation profile peak within BOX 305 and of sufficient dosage to lower the dielectric constant of BOX 305 by about 5 to 25% after the anneal step illustrated in FIG. 3E. In one example, fluorine is implanted at a dose of about 1 X 10^{14} to 1 X 10^{17} atm/cm2 and energies of about 2 to 40 Kev.

The description of the embodiments of the present invention is given above for the understanding of the present invention. It will be understood that the invention is not to the particular embodiments described herein, but is capable of various modifications, rearrangements and substitutions will now become apparent to those skilled in the art without departing from the scope of the invention. For example, the invention is applicable to raised source/drain FETs, wherein the fluorine implantation and anneal steps may be performed either before or after the formation of the raised source drain. In addition, the fluorine implant and anneal steps may be performed before source/drains are formed by replacing the gate after the fluorine implant and anneal and then performing source/drain spacer, implantation and anneal steps.

CLAIMS

1. A silicon-on-insulator (SOI) field effect transistor (FEI) comprising:

a silicon (300) substrate having a silicon layer (310) on top of a buried oxide layer (305) having doped regions (380) and an undoped region (305), said undoped region having a dielectric constant different from a dielectric constant of said doped regions;

source/drains (365) in said silicon layer and separated by a body (370) in said silicon layer, said source/drains aligned over said doped regions and said body aligned over said undoped region; and

a gate dielectric (325) on top of said body and a gate (330) on top of said gate dielectric.

2. The SOI FET of claim 1, wherein said dielectric constant of said doped regions is less than said dielectric constant of said undoped region.

3. The SOI FET of claim 2, wherein the said dielectric constant of said doped regions is 5 to 25 % less than said dielectric constant of said undoped region.

4. The SOI FET of any preceding claim, where said doped region is doped with fluorine.

5. The SOI FET of any preceding claim, wherein said buried oxide layer is a first buried oxide layer and further comprising a second silicon layer on top of a second buried oxide layer, said second silicon and said second buried oxide layer between said first buried oxide layer and said substrate.

6. The SOI FET of any of claims 1 to 5, wherein said silicon layer is 50 to 500 Å in thickness and said buried oxide layer is 50 to 500 Å in thickness.

7. A method of fabricating a silicon-on insulator (SOI) field effect transistor (FEI) comprising:

providing a silicon substrate (300) having silicon layer (310) on top of a buried oxide layer (305);

forming a gate dielectric (325) on top of the silicon layer;

forming a gate conductor (330) on top of said gate dielectric;

forming source/drains (365) in said silicon layer, said source drains being separated by a body (370) in said silicon layer, said body being aligned under said gate; and

forming doped regions (380) in said buried oxide layer, said doped regions being aligned under said source /drains and having a dielectric constant different from a dielectric constant of non-doped regions (305) of said buried oxide layer.

8. The method of claim 7, wherein said doped regions are fluorinated by implanting fluorine into said doped region.

9. The method of claim 8, wherein the implanting of fluorine is performed at an implant energy sufficient to place the peak of the fluorine implant distribution within said buried oxide layer.

10. The method of claim 8 or claim 9, further comprising annealing said SOI FET in the temperature range of 600 to 1100°C.

11. The method of any of claims 7 to 10, wherein said dielectric constant of said doped regions is 5 to 25% less than said dielectric constant of non-doped buried oxide.

12. The method of any of claims 8 to 10, further comprising forming a first spacer on sidewalls of said gate to limit extension of said source/drains and said fluorine implant under said gate.

13. The method of claim 12, further comprising forming a second spacer on sides of said first spacers to limit extension of said fluorine implant under said gate.

14. The method of claim 7, further comprising forming a hard mask on top of said gate.

15. The method of any of claims 8 to 10, further comprising forming a patterned photoresist layer on top of said gate, said photoresist layer having an edge extending and aligned over said source/drains to limit extension of said fluorine implant under said gate.

16. The method of any of claims 7 to 15, wherein said silicon layer is 50 to 500 Å in thickness and said buried oxide layer is 50 to 500 Å in thickness.

17. The method of claim 7, wherein said buried oxide layer is a first buried oxide layer and further comprising a second silicon layer on top of a second buried oxide layer, said second silicon and said second buried oxide layer between said first buried oxide layer and said substrate.

18. The method of any of claims 8 to 10, wherein said flourine is implanted a dose of 1 X 10^{14} to 1 X 10^{17} atm/cm2 and at energies of 2 to 40 Kev.