

PATENT SPECIFICATION

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NO DRAWINGS.

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COMPLETE SPECIFICATION.

Semiconductor Device Fabrication.

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—
This invention relates to semiconductor device fabrication.

Oxide layers, such as silicon oxide layers, have been successfully used for masking semiconductor bodies against diffusion of such conductivity determining impurities as boron, arsenic and phosphorus. However, zinc and cadmium vapours can penetrate these masking oxide layers rendering them ineffectual. Thus it is desired to provide in a method of fabricating a semiconductor device, for making oxide layers function as a masking layer against zinc and cadmium diffusion.

Accordingly, the present invention provides a method of fabricating a semiconductor device comprising the steps of: masking a portion of a semiconductor body with an oxide layer which includes another substance which inhibits the diffusion of zinc or cadmium conductivity modifier through said layer; and, treating said body in the vapours of zinc or cadmium to diffuse said modifier into the unmasked portion only of said body.

Since zinc and cadmium are usually the doping impurities for Group III—V semiconductors the semiconductor wafer used herein generally is a Group III—V compound, that is, a member of the Group consisting of the nitrides, phosphides, arsenides, and antimonides of boron, aluminium, gal-

lium and indium. However, the semiconductor itself plays no essential role in the method and so, any semiconductor, such as silicon or germanium, could be used if desired.

The oxide coating referred to herein is generally a silicon oxide, such as silicon monoxide or silicon dioxide, although magnesium oxide, titanium oxide, and aluminium oxide may be utilized for this purpose. Any method available in the art may be used for preparing this coating. A convenient method of depositing a silicon oxide coating on the semiconductor is to heat the semiconductor in the vapours of an organic siloxane compound at a temperature below the melting point of the semiconductor but above the temperature at which the siloxane compound decomposes. An inert adherent coating of silicon oxides is formed on the wafer surface. The silicon oxide coating provided herein includes a substance which inhibits the diffusion of zinc or cadmium conductivity modifier through said coating. Generally that substance is phosphorus. It is provided in the gas stream together with the siloxane in vapour form so that both materials deposit together in the coating.

To illustrate the present invention an example will now be described. A wafer of N-type gallium arsenide is placed in a furnace at 750°C. A gas stream of nitrogen as a carrier gas, ethyl orthosilicate as the siloxane compound, and a diffusion inhibitor substance, for example, trimethyl phosphate is introduced into the furnace and passed over the gallium arsenide. The gas stream is formed by passing the carrier gas through a liquid mixture of the siloxane and the diffusion inhibitor substance. The proportions of the inhibitor and of the siloxane compound may be varied to obtain different concentra-

[Price 4s. 6d.]



oxide
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2 tions of the inhibitor in the silicon concentra-
mask subsequently formed. Eight volumes
ethyl orthosilicate and two volumes tri-
methyl phosphate is a practical mixture.

5 At the furnace temperature the siloxane
compound and the phosphorus compounds
are decomposed. Thus a phosphorus-con-
taining silicon oxide coating is deposited on
the exposed face of the semiconductor
10 wafer.

A selected portion of the coating thus
produced is now removed by any convenient
technique. A simple method is to grind it
off. A selected portion of the wafer face is
15 thus exposed. The rest of the wafer face
is covered by a masking layer which is the
phosphorus containing silicon oxide coating.

A diffusion step is now performed by
heating the wafer in vapours of zinc.
20 The exact time and temperature utilized
depends on the depth at which diffusion is
desired. Suitably, the wafer is heated in
zinc vapours at a temperature of 700°C to
900°C for one to three hours. Zinc is thus
25 diffused into the wafer portion which is
immediately adjacent to the exposed por-
tion of the wafer face. Practically no zinc
diffuses through the phosphorus containing
silicon oxide layer. The part of the semi-
30 conductor into which zinc has diffused is
converted to P-type conductivity, and a
rectifying barrier of P-N junction is formed
at the interface between the P-type zinc
diffused wafer region and the N-type bulk of
35 the semiconductor wafer.

The masking coating is now removed by
any convenient technique such as by lap-
ping, or by treating the wafer in a hydro-
fluoric acid solution. An electrical lead
40 wire may be bonded to the zinc diffused P-
type region, and another electrical lead wire
bonded to wafer face coaxially opposite
to the first lead. The device thus fabricated
is a diffused gallium arsenide diode.

45 While the exact mechanism which in-
hibits the diffusion of zinc through the
masking layer is not presently certain, it is

theorized that the zinc atoms diffusing
through the masking layer react with the
diffusion inhibitor (phosphorus atoms in this
example) to form a compound (probably
zinc phosphide in this example), and are
thus immobilized and bound to the masking
layer. However, it will be understood that
the practice of the invention is not depen-
55 dent on whatever theory is selected to ex-
plain the improved results obtained.

WHAT WE CLAIM IS:—

1. A method of fabricating a semicon-
ductor device comprising the steps of: 60
masking a portion of a semiconductor body
with an oxide layer which includes another
substance which inhibits the diffusion of
zinc or cadmium conductivity modifier
through said layer; and, treating said body 65
in the vapours of zinc or cadmium to
diffuse said modifier into the unmasked
portion only of said body.

2. A method according to Claim 1
wherein said oxide layer is silicon oxide. 70

3. A method according to Claim 1
wherein said inhibitor substance is phos-
phorous.

4. A method according to Claim 1
wherein said semiconductor is a Group 75
III—V compound.

5. A method according to any one of
the preceding claims in which the masking
oxide layer is removed after the zinc or
cadmium has diffused into the unmasked 80
portion.

6. A method according to Claim 1 sub-
stantially as hereinbefore described.

7. A semiconductor device when pro-
duced by a method according to any one 85
of the preceding claims.

A. M. & Wm. CLARK,
Chartered Patent Agents,
5, Stone Buildings
Lincoln's Inn,
London, W.C.2.



oxide
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tions of the inhibitor in the silicon concentra- mask subsequently formed. Eight volumes ethyl orthosilicate and two volumes trimethyl phosphate is a practical mixture.

5 At the furnace temperature the siloxane compound and the phosphorus compounds are decomposed. Thus a phosphorus-containing silicon oxide coating is deposited on the exposed face of the semiconductor wafer.

10 A selected portion of the coating thus produced is now removed by any convenient technique. A simple method is to grind it off. A selected portion of the wafer face is thus exposed. The rest of the wafer face is covered by a masking layer which is the phosphorus containing silicon oxide coating.

A diffusion step is now performed by heating the wafer in vapours of zinc. 20 The exact time and temperature utilized depends on the depth at which diffusion is desired. Suitably, the wafer is heated in zinc vapours at a temperature of 700°C to 900°C for one to three hours. Zinc is thus 25 diffused into the wafer portion which is immediately adjacent to the exposed portion of the wafer face. Practically no zinc diffuses through the phosphorus containing silicon oxide layer. The part of the semiconductor into which zinc has diffused is 30 converted to P-type conductivity, and a rectifying barrier of P-N junction is formed at the interface between the P-type zinc diffused wafer region and the N-type bulk of the semiconductor wafer.

35 The masking coating is now removed by any convenient technique such as by lapping, or by treating the wafer in a hydrofluoric acid solution. An electrical lead 40 wire may be bonded to the zinc diffused P-type region, and another electrical lead wire bonded to wafer face coaxially opposite to the first lead. The device thus fabricated is a diffused gallium arsenide diode.

45 While the exact mechanism which inhibits the diffusion of zinc through the masking layer is not presently certain, it is

theorized that the zinc atoms diffusing through the masking layer react with the diffusion inhibitor (phosphorus atoms in this example) to form a compound (probably zinc phosphide in this example), and are thus immobilized and bound to the masking layer. However, it will be understood that the practice of the invention is not dependent on whatever theory is selected to explain the improved results obtained. 50 55

WHAT WE CLAIM IS:—

1. A method of fabricating a semiconductor device comprising the steps of: 60 masking a portion of a semiconductor body with an oxide layer which includes another substance which inhibits the diffusion of zinc or cadmium conductivity modifier through said layer; and, treating said body 65 in the vapours of zinc or cadmium to diffuse said modifier into the unmasked portion only of said body.

2. A method according to Claim 1 wherein said oxide layer is silicon oxide. 70

3. A method according to Claim 1 wherein said inhibitor substance is phosphorous.

4. A method according to Claim 1 wherein said semiconductor is a Group 75 III—V compound.

5. A method according to any one of the preceding claims in which the masking oxide layer is removed after the zinc or cadmium has diffused into the unmasked 80 portion.

6. A method according to Claim 1 substantially as hereinbefore described.

7. A semiconductor device when produced by a method according to any one 85 of the preceding claims.

A. M. & Wm. CLARK,
Chartered Patent Agents,
5, Stone Buildings
Lincoln's Inn,
London, W.C.2.