

## ABSTRACT

A memory device includes a first control circuit that is adjacent to a data input and output circuit and that generates an output enable signal driven to a first internal voltage based on an output control pulse generated after the start of a data output operation, generates output data from internal data loaded onto a global line through a repeater by receiving a delay output enable signal driven to a second internal voltage, and outputs the output data to the data input and output circuit, a data storage circuit that is adjacent to the first control circuit and that outputs the internal data to the global line after the start of the data output operation, and a second control circuit that is adjacent to the data storage circuit and that generates the delay output enable signal based on the output enable signal after the start of the data output operation.

FIG. 1