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TITLE OF THE INVENTION

LIQUID CRYSTAL DISPLAY

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor element and a liquid crystal display, and in particular, it relates to a semiconductor element suitable for use as a thin film semiconductor element and an active matrix addressing type liquid crystal display using the same.

As display devices for displaying image information and characters for use in the field of office automation equipment and the like, active matrix addressing liquid crystal displays using thin film transistors (hereinafter referred to as TFT) have been known. For this type of conventional liquid crystal displays, further improvements in resolution and high quality of display as well as cost reduction in manufacture are necessary. In order to solve these problems, it is most important to improve the performance of the thin film transistor which is a key device to the active matrix addressing liquid crystal displays. In this regard, it was proposed in the Conference Record of International Display Research Conference 1985, page 9, a concept of forming advanced high performance TFTs on a glass substrate, in which peripheral drive circuits for driving a TFT active matrix are fabricated using TFTs and integrated with its display unit on the same substrate so as to reduce the cost of manufacture. With provision of the advanced high performance peripheral drive

circuits integrated on the glass substrate, since other circuits to be mounted externally and their mounting process can be simplified, a substantial reduction in the packaging cost can be expected. However, in order to provide the high performance circuits, development of a more improved, sophisticated high performance TFT is required. In particular, TFTs which are formed on polycrystalline silicon (hereinafter referred to as poly-Si) and are expected as the most promising TFTs suitable for use in display equipment having integrated peripheral drive circuits, but have further technical problems yet to be solved, which include improvement of the carrier mobility and lowering of the threshold voltage Vth.

A method of operation at a lower voltage by lowering the threshold voltage Vth of transistors formed on an insulator is proposed as described in the Technical Digest of International Electron Device Meeting 1994, page 809- , in which a so-called dynamic threshold voltage MOSFET (hereinafter referred to as DTMOS) which has a fourth contact, separate from the source and drain, on a semiconductor film acting as a bipolar active layer, and is in contact with the gate electrode, is proposed as a submicron silicon-on-insulator (SOI) device.

In the above-mentioned prior art, the threshold voltage of transistors is substantially reduced further to lower the operating voltage of the circuits thereof, thereby lowering the power supply voltage, and thus

minimizing the power consumption in the drive circuits. This feature of decreased power consumption achieved by this drive circuit of the prior art is desirable for a drive circuit and device for the liquid crystal display as well. It should be noted, however, that the above-mentioned prior art is directed to the provision of logic devices or memory devices that can be operated at a low voltage and a high speed, and that they cannot be applied, as they are, to the drive devices for driving the liquid crystal display.

Namely, the semiconductor device according to the above-mentioned prior art, as described in the aforementioned literature, pages 809-, is designed to operate effectively with a gate voltage at 0.6 V or less, thereby the semiconductor device of the prior art cannot be applied as it is to the liquid crystal display in which a lower limit of gate drive voltage is determined by a liquid crystal drive voltage. More particularly, at least ± 3 V in peak amplitudes is required for driving normal liquid crystal materials, thereby a higher voltage than this minimum peak voltage is required as the gate voltage for driving pixel drive transistors in the liquid crystal device. Thus, the prior art semiconductor device described above which operates at the gate voltage less than 1 V cannot be applied to the liquid crystal display.

Summary of the Invention

An object of the invention is to provide an active matrix address type liquid crystal display of which the power

consumption can be substantially reduced.

Another object of the invention is to provide a small power consumption liquid crystal display having a built-in drive circuit.

Still another object of the invention is to provide a drive circuit for use in a small power consumption liquid crystal display.

According to the invention, a semiconductor element for use as a switching element to be formed in a display area of the liquid crystal display or for use as a drive element to be formed in the area of a drive circuit for driving the display area is comprised of: a first electrode, a second electrode, a third electrode and a fourth electrode; a pair of first conducting type semiconductor layers formed separated from each other and connected to the second and the third electrodes, respectively; an intrinsic semiconductor layer connected to the pair of the first conducting type semiconductor layers; and a second conducting type semiconductor layer formed on the intrinsic semiconductor layer; wherein the first electrode is formed on the intrinsic semiconductor layer via an insulating film; and the fourth electrode is formed on the second conducting type semiconductor layer which is formed on the intrinsic semiconductor layer.

Preferably, the pair of the first conducting type semiconductor layers and the second conducting type semiconductor layer are separated from each other by the

intrinsic semiconductor layer. Further, according to another aspect of the invention, the intrinsic semiconductor layer extends in lateral directions further than the insulating layer at least towards the pair of the first conducting type semiconductor layers on the substrate.

The first electrode and the fourth electrode are electrically connected via a resistance advantageously for wiring the liquid crystal display.

The intrinsic semiconductor layer, the first conducting type semiconductor layers and the second conducting type semiconductor layer are preferably a thin film semiconductor made either of silicon, silicon germanium and silicon carbide. Further, they may be made of polycrystalline silicon films as well. In particular, it is preferable to use polycrystalline silicon films in a drive circuit built-in type liquid crystal display.

The semiconductor element of the invention can be designed to have a structure either of a planar type, an inverted staggered type or a positive staggered type. In the case of the inverted staggered type, a first electrode is formed on one of a pair of substrates, an insulating layer is formed on the first electrode, and an intrinsic semiconductor layer is formed on this insulating layer, then a pair of first conducting type semiconductor layers are formed on the intrinsic semiconductor layer. Further, in the case of the planar type, the second, the third and the fourth electrodes are formed on one of the pair of substrates.

In both cases of the positive staggered and the inverted staggered types, it is also possible for either one of the pair of the first conducting type semiconductor layers or the second conducting type semiconductor layer to be formed by self-alignment utilizing a counterpart's pattern as its own masking pattern.

The semiconductor element of the invention can be used as complementary N-type and P-type semiconductor elements which can be formed in the drive circuit region in the liquid crystal display. More particularly, since a vertical scanning circuit and a picture signal drive circuit are provided in the drive circuit region, the complementary semiconductor element of the invention can be applied to a shift register within these circuits. More specifically, when the semiconductor element of the invention is used in the drive circuit region in a peripheral circuit built-in type liquid crystal display, the power consumption thereof can be reduced effectively and substantially.

According to the invention, an intrinsic semiconductor layer is formed as an i semiconductor layer between the first, the second and the third electrodes. Into this intrinsic semiconductor layer, a current carrier is injected which has a different polarity from a polarity of a current carrier in the impurity semiconductor layers of the first conducting type which are connected to the second and the third electrodes, respectively. According to

this arrangement, when the impurity semiconductor layers connected to the second and the third electrodes respectively are formed of an n-type semiconductor layer, there is formed a p-i-n junction between a current carrier injection layer or the fourth electrode and the second electrode.

Further, when a voltage applied across the current carrier injection layer, i.e., the fourth electrode and the second electrode is Vb, the voltage Vb is divided between an i-n junction and the i layer of the p-i-n junction, thereby preventing an excess current (base current) from flowing. Thereby, operation at a low power can be ensured until the gate voltage (to be applied to the first electrode) increases substantially. Namely, if a P-type or N-type semiconductor layer is used in place of the intrinsic semiconductor of the invention, a full voltage of Vb is applied to the source junction, and if Vb exceeds a built-in voltage (approximately 0.6 V) of the source junction, an excess current is caused to flow, thereby rapidly increasing power consumption. In contrast, if an active semiconductor layer is comprised of an intrinsic semiconductor, excess base current will not flow until a substantially higher gate voltage is applied, thereby ensuring operation at a low power. In this case, due to adoption of the p-i-n junction, the degree of drop in the threshold voltage becomes mild, but it is still substantial compared to the conventional elements. Due to this drop in

the threshold voltage, it becomes possible to operate the liquid crystal driving elements and associated peripheral circuits at lower voltages, thereby substantially reducing power consumption in the active matrix type displays.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features and advantages of the present invention will be understood more clearly from the following detailed description with reference to the accompanying drawings, wherein:

Fig. 1 is a cross-sectional view of a semiconductor element according to one embodiment of the invention;

Fig. 2 is a schematic diagram in cross-section of the semiconductor element of Fig. 1 indicative of the principles of operation thereof;

Fig. 3 is a schematic diagram of energy bands indicative of the principles of operation of the semiconductor element of Fig. 1;

Fig. 4 is a diagram indicative of transfer characteristics of the semiconductor element of Fig. 1;

Fig. 5 is a cross-section of a semiconductor element according to a second embodiment of the invention;

Fig. 6 is a cross-section of a semiconductor element according to a third embodiment of the invention;

Fig. 7 is an equivalent circuit of a semiconductor element according to a fourth embodiment of the invention;

Fig. 8 is a plan view of a semiconductor element according to a fifth embodiment of the invention;

Fig. 9 is a cross-section of a TFT taken along X-X' line in Fig. 8;

Fig. 10 is a plan view of a semiconductor element according to a sixth embodiment of the invention;

Fig. 11 is a cross-section of a TFT taken along X-A line in Fig. 10;

Fig. 12 is a circuit diagram of a complementary type inverter according to a seventh embodiment of the invention;

Fig. 13 is a plan view of the complementary type inverter of Fig. 12;

Fig. 14 is a cross-section of a complementary type inverter according to an eighth embodiment of the invention;

Fig. 15 is a plan view of the complementary type inverter of Fig. 14, which is a planar type semiconductor element of the invention;

Fig. 16 is a plan view of a unit picture element in a liquid crystal display according to a ninth embodiment of the invention, and taken along X-X' in Fig. 15;

Fig. 17 is a cross-section of the liquid crystal display taken along Y-Y' in Fig. 18;

Fig. 18 is an equivalent circuit indicative of a schematic configuration of the liquid crystal display;

Fig. 19 is a plan view and a cross-section of a semiconductor element according to a tenth embodiment of the invention;

Fig. 20 is a plan view and a cross-section of a unit picture element of a liquid crystal display constructed using

the semiconductor element of Fig. 19;

Fig. 21 is an equivalent circuit of a drive circuit built-in type liquid crystal display constructed using the semiconductor elements of Fig. 19;

Fig. 22 is a circuit configuration including shift register and buffer used in the drive circuit built-in type liquid crystal display of Fig. 21;

Fig. 23 is a cross-sectional view of a semiconductor element indicative of a process of fabrication thereof according to an eleventh embodiment of the invention;

Fig. 24 is a cross-sectional view of a semiconductor element indicative of a process of fabrication thereof according to a twelfth embodiment of the invention;

Fig. 25 is a diagram indicative of current-voltage characteristics of the semiconductor element of Fig. 19;

Fig. 26 is a cross-section of a liquid crystal cell of a liquid crystal display according to a thirteenth embodiment of the invention; and

Fig. 27 is a cross-section of a liquid crystal cell of a liquid crystal display according to a fourteenth embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the invention will be described in details with reference to the accompanying drawings.

First Embodiment of The Invention:

With reference to Fig. 1, a first embodiment of the invention will be described in the following. Fig. 1 is a cross-sectional view of a semiconductor element according to the first embodiment, which has a gate electrode 10 as a first electrode made of chrome and formed on the surface of a glass substrate 1. Gate electrode 10 is overlaid by a gate insulating film 20 consisting of SiN film. An intrinsic a-Si layer 30 is formed on gate insulating film 20. On the surface of intrinsic a-Si layer 30, there are formed n-type a-Si layers 31, 32 which are doped with phosphor, and a p-type a-Si layer 33 which is doped with boron.

p-type a-Si layer 33 is formed between a pair of n-type a-Si layers 31 and 32 on the intrinsic a-Si layer 30 by self-alignment using the pattern of n-type a-Si layers 31 and 32 as its own masking pattern. Use of the pattern of n-type a-Si layers 31, 32 as its own mask pattern thereby to form p-type a-Si layer 32 will enable forming both of n-type a-Si layers 31, 32 and p-type a-Si layer 33 by a single photolithographic process, thereby simplifying the fabrication process thereof and thus decreasing production cost. Further, as the second and the third electrodes to be connected to the n-type a-Si layers 31 and 32 respectively, a source electrode 11 and a drain electrode 12 made of titanium are formed. Further, a base electrode 14 is formed in contact with p-type a-Si layer 33 as a hole injection electrode. Then, the entire portion of the element is overlaid by a passivation film 22 made of SiN film, thereby

providing for an n-type field effect transistor according to the invention.

Namely, according to this embodiment of the invention, the majority carrier is electron, and the minority carrier is hole. By applying a positive voltage which is positive relative to source electrode 11 to base electrode 14 which is in contact with p-type a-Si layer 33, the minority carrier of holes is caused to be injected into intrinsic silicon layer 30.

Now, with reference to Figs. 2 and 3, operation of the semiconductor element of Fig. 1 will be described specifically. In the n-type transistor, with reference to Fig. 2, a conduction state (ON-state) is realized by applying positive voltages Vg and Vd which are positive relative to source electrode 11 which is at ground potential, to gate electrode 10 and drain electrode 12, respectively. At this time, a positive voltage Vb is applied to the fourth electrode 14 (hereinafter referred to as base electrode) which is in contact with p+type layer 33 formed on the intrinsic semiconductor layer. By the positive voltage Vb applied, an n-i-p junction comprised of n+layer 31 in contact with source electrode 11, intrinsic semiconductor layer 30 and p+layer 33 is biased in the forward direction, thereby causing holes to be injected through p+layer 33 into the intrinsic semiconductor layer.

A flow of injected holes is depicted by ϕh. Then, the injected holes drift toward source electrode 11, but are

blocked by a potential barrier at an n+/i junction formed between n+ layer 31 and intrinsic semiconductor layer 30, thereby being accumulated in the vicinity of the n+/i junction. The accumulated holes in turn cause the potential barrier at the n+/i junction to be lowered. Thereby, a large amount of electrons are injected from n+ layer 31 into intrinsic semiconductor layer 30 toward a channel ch formed at a boundary between intrinsic semiconductor layer 30 and gate insulating film 20. A flow of injected electrons is depicted by ϕe. As a result, a substantial increase in the majority carrier current (electrons) can be realized by the injection of a small amount of minority carrier current (holes) according to the invention.

Status of carrier flows across energy bands at the source junction along X-X' of Fig. 2 is depicted in Fig. 3, where it is indicated that holes injected from base electrode 14 are blocked by the potential barrier at the n+/i junction so as to be accumulated in the vicinity of the n+/i junction. Thereby, the potential energy in the intrinsic semiconductor layer 30 changes from its initial status prior to the accumulation of the injected holes which is depicted by dotted lines to a status as depicted by solid lines, thereby lowering the potential barrier against a mass of electrons present in n+ layer 31, thereby allowing the mass of electrons to be injected toward the channel ch as depicted by ϕe.

On the other hand, in order to cut-off the

transistor, a negative voltage is applied to gate10 as well as to base electrode 14 such that the n-i-p junction is biased in the reverse direction. When the n-i-p junction is reversely biased, injection of holes from the base electrode 14 is stopped, thereby interrupting the current.

According to the feature of this embodiment of the invention, the effect of current amplification in the transistor is most significant in a subthreshold region in which electron current is restricted due to injection from source electrode 11, and thus transfer characteristics therein change such that a current rise becomes steep in the subthreshold region R with an increasing base current ib as indicated in Fig. 4, thereby advantageously allowing threshold voltage Vth to decrease.

According to this feature of this embodiment of the invention as described above, since intrinsic semiconductor layer 30 is used as its semiconductor layer, when a voltage Vb is applied between the base and the source, the voltage Vb is subdivided between the i-layer and the i/n junction of the p-i-n junction, thereby preventing an excess base current from flowing until a substantially higher voltage is applied across the base and the source, thereby ensuring operation at a higher gate voltage, for example, exceeding ±5V and at a reduced power consumption. Thereby, when a semiconductor device of which the threshold voltage can be lowered is utilized as a liquid crystal driving element or as a peripheral circuit device thereof, it becomes possible

to lower the voltage to drive the liquid crystal display, thereby minimizing the power consumption in the active matrix addressing type display.

Second Embodiment:

Figure 5 is a cross-sectional view of a semiconductor device according to a second embodiment of the invention.

The semiconductor device according to the second embodiment of the invention has a structure of a positive stagger type TFT, in which a source electrode 11, a drain electrode 12 and a base electrode 14 each made of chromium are formed on the surface of a glass substrate separate from each other. On the surfaces of the source electrode 11 and the drain electrode 12 are formed n-type a-Si layers 31 and 32, respectively, and on the surface of the base electrode 14 is formed a p-type a-Si layer 33. An intrinsic semiconductor layer (intrinsic a-Si layer) 30 is formed between the source and base electrodes, between the base and drain electrodes, and on the surfaces of n-type a-Si layers 31 and 32 as well as on the p-type a-Si layer 33. A gate insulating film 20 made of a silicon nitride (SiN) film is formed on the surface of the intrinsic semiconductor layer 30, and further a gate electrode 10 made of aluminum is formed on the gate insulating film 20. Then, the whole structure of the device described above is encapsulated in a passivation film 22 made of a silicon nitride (SiN) film.

In the semiconductor device according to the second

embodiment of the invention, the majority carriers are electrons and the minority carriers are holes likewise the first embodiment of the invention.

According to this arrangement of the second embodiment of the invention, a positive voltage which is positive relative to a voltage at the source electrode 11 is applied to the base electrode 14 which is in contact with p-type a-Si layer 33, thereby causing the minority carrier of holes to be injected into the intrinsic semiconductor layer 30. Thereby, under the same principle as described in the first embodiment of the invention, it becomes possible to lower its threshold voltage and in consequence to improve its current drivability substantially.

In this second embodiment of the invention, intrinsic semiconductor layer (intrinsic a-Si layer) 30 is utilized as its active layer in the same manner as in the first embodiment of the invention, however, it is not limited thereto, and other semiconducting materials such as, for example, polycrystalline silicon (poly-Si) or silicon germanium (SiGe) films can be utilized as well to the same effect.

Third Embodiment:

Figure 6 is a cross-sectional view of a semiconductor device according to a third embodiment of the invention.

The semiconductor device according to the third embodiment of the invention has a structure of a planar-type

TFT, in which a base electrode 14 made of chromium is formed on a glass substrate 1 in the center portion thereof, and n-type poly-Si layers 311 and 321 are formed on the glass substrate separated by base electrode 14 interposed therebetween. A p-type poly-Si layer 331 is formed on the surface of base electrode 14. Further, an intrinsic semiconductor layer (intrinsic poly-Si layer) 301 is formed surrounding both the base electrode 14 and p-type poly-Si layer 331. A gate insulating film 201 made of SiO_2 is formed on a part of the intrinsic semiconductor layer 301, then, a gate electrode 10 made of aluminum is formed on the gate insulating film 201. The n-type poly-Si layers 311 and 321 formed in contact in part with intrinsic semiconductor layer 301 are further connected with a source electrode 11 and a drain electrode 12 both made of chromium, respectively. Then, source electrode 11, drain electrode 12 and gate electrode 10 are surrounded by a protective insulating film 21, and the entire structure of the device is encapsulated in a passivation film 22. Also in this third embodiment of the invention, the majority carriers are electrons and the minority carriers are holes as in the first embodiment of the invention.

According to this device arrangement of the third embodiment of the invention, when a positive voltage which is positive relative to a voltage at source electrode 11 is applied to the base electrode 14 which is in contact with p-type poly-Si layer 331, the minority carriers of holes are

caused to be injected into intrinsic semiconductor layer 301. Thereby, under the same principle of operation of the semiconductor device as indicated in Fig. 1, it becomes possible to lower the threshold voltage, thereby substantially improving the current drivability.

Further, according to this embodiment of the invention, n-type poly-Si layers 311 and 321 are formed by means of self-alignment with respect to the pattern of the gate insulating film 201 and gate electrode 10. Namely, the pattern of gate insulating film 201 and gate electrode 10 is utilized as a mask to form n-type poly-Si layers 311 and 321. Thereby, a single step of photolithographic processing allows provision of both patterns of n-type poly-Si layers 311 and 321 as well as gate electrode 10, thereby simplifying the process of fabrication, and reducing the cost of manufacture. Still further, there is another advantage that parasitic capacitances between gate electrode 10 and source electrode 11 as well as between gate electrode 10 and drain electrode 12 can be minimized since width of overlapping of gate electrode 10 with n-type poly-Si layers 311, 312 is minimized due to the self-alignment processing of the invention, thereby realizing a faster operation of the device.

Fourth Embodiment of the Invention:

When a semiconductor device is formed having four terminals of a gate electrode, a source electrode, a drain electrode and a base electrode, this semiconductor device

having four terminals cannot be applied as it is to a transistor for use in a liquid crystal display or in its associated drive circuit which principally requires three-terminal transistors. Therefore, in order to apply this four-terminal transistor, an additional wiring must be provided for supplying a base current, which substantially complicates its circuit configuration and increases the area for circuits.

Thereby, with reference to Fig. 7, by taking into consideration the fact that an npn type bipolar transistor comprising n-type a-Si layer 32, p-type a-Si layer 33 and n-type a-Si layer 31 is formed between source electrode 11 and channel ch in this field effect transistor (FET) of the fourth embodiment of the invention, it is contemplated that a base current can be supplied from the gate by connecting between base electrode 14 and gate electrode 10 via resistance rb having an appropriate value.

When the gate and base are connected via resistance rb, the additional wiring conventionally would have been required for supplying a base current to the base electrode can be eliminated, thereby simplifying the wiring substantially and improving the density of circuit integration, thereby allowing a finer resolution of display to be realized.

Fifth Embodiment of the Invention:

Fig. 8 is a plan view of a planar type TFT of the fifth embodiment of the invention, and Fig. 9 is a cross-

sectional view of the planar type TFT taken along X-X' in Fig. 8.

According to this embodiment of the invention, an intrinsic semiconductor layer 301 having a convex planar pattern and a pattern of a gate electrode 10 disposed in the center thereof are formed, and on the both sides thereof are formed n+layers 311 and 321 as the source and drain, respectively. By way of example, n+layers 311 and 321 are formed on a glass substrate likewise the planar type transistor of Fig. 6. In the upper protruding portion of intrinsic semiconductor layer 310 there is formed p+layer 331which serves as the base. Source electrode 11 and drain electrode 12 are formed in contact with n+layer 311 acting as source and n+layer 321 acting as drain, respectively. A portion extending below the gate electrode from intrinsic semiconductor layer 301 (channel) to p+layer 331 is not doped with any impurities of P-type or N-type and forms a high resistance layer rb. The source and drain of n+layers 311, 321 as well as the base of p+layer 331 are separated by intrinsic semiconductor layer 301 from each other.

Also, in this embodiment of the invention, likewise the first embodiment, the majority carrier is electron, and the minority carrier is hole. By applying a positive voltage which is positive relative to source electrode 11 to base electrode 14 which is in contact with p-type poly-Si layer 331, the minority carrier of holes is caused to be injected into intrinsic poly-Si layer 301. Thereby,

according to the same principle of operation as in the semiconductor element of Fig. 1, its threshold voltage can be decreased, and thereby improving its current drive capability.

Further, by electrically connecting between base electrode 14 and gate electrode 10 according to this embodiment of the invention, the operation available with the three terminal structure as indicated in Fig. 7 becomes possible. In this instance, since the high resistance layer rb acts to limit the base current, injection of an excessive base current is prevented, thereby allowing operation at a low power until the gate voltage increases to exceed, for example, ±5 V.

Current-voltage characteristics of TFTs according to this embodiment of the invention, such as drain current to gate voltage characteristics as well as drain current to drain voltage characteristics, are compared to those of conventional TFTs in Figs. 25 (a) and (b).
It is clearly indicated that TFTs of the invention have an improved current drive capability substantially greater than the conventional TFTs.

Sixth Embodiment of the Invention:

With reference to Fig. 10, a plan view of a planar type TFT according to a sixth embodiment of the invention is illustrated. Fig. 11 is a cross-sectional view taken along X-A in Fig. 10.

According to this embodiment of the invention,

likewise the fifth embodiment, an intrinsic semiconductor layer 301 is formed to have a convex planar pattern, with a pattern of a gate electrode 10 disposed in the center thereof. On both sides of intrinsic semiconductor layer 301 there are formed n+layer 311 as the source and n+layer 321 as the drain, respectively. Further, p+layer 331 is formed as the base in a protruding portion of the convex patterned intrinsic semiconductor layer 301. Further, in a portion below the gate electrode extending from intrinsic semiconductor layer 301 (channel) to p+layer 331, there is formed a high electrical resistance layer rb which is not doped with any impurities of P-type or N-type. These features are the same as those in the fifth embodiment of the invention. Another feature of this embodiment is characterized by comprising an off-set layer roff made of intrinsic semiconductor layer 301 between n+layer 311 as the source and n+layer 321 as the drain, and intrinsic semiconductor layer 301 (channel) directly below gate electrode 10. That is, n+layers 311 as the source, 321 as the drain, and p+layer 331 as the base have arrangements which are separated by intrinsic semiconductor layer 301 from each other. In order to realize such arrangements, a pattern of gate insulating film 20 is arranged to have a larger size than that of gate electrode 10, and by utilizing the pattern of this gate insulating film 20 as a mask pattern for masking other counterparts, n+layers 311, 321 as the source and drain or p+layer 331 as the base are formed

advantageously.

According to this embodiment of the invention, likewise the case of the first embodiment, the majority carrier is electron, and the minority carrier is hole. In this arrangement, a positive voltage which is positive relative to source electrode 11 is applied to base electrode 14 which is in contact with p-type poly-Si layer 331, thereby causing the minority carrier of holes to be injected into intrinsic poly-Si layer 301. Thereby, according to the same principle of operation as the semiconductor element of Fig. 1, the threshold voltage is successfully decreased, thereby improving the current drive capability substantially. Further, by electrically connecting between base electrode 14 and gate electrode 10 according to this embodiment of the invention, operation of the semiconductor element having a three-terminal configuration as indicated in Fig. 7 can be realized. In this configuration, since the off-set layer roff as well as the high resistance layer rb acts to limit the base current, an excess base current injection is more effectively prevented, thereby ensuring operation at a low electric power until the gate voltage is increased substantially greater. Further, since the off-set layer acts to mitigate electrical field present between source electrode 11 and drain electrode 12, occurrence of hot carriers is suppressed, thereby improving reliability of components substantially.

Seventh Embodiment of the Invention:

Fig. 12 is a schematic diagram of a circuit configuration of a complementary (CMOS) inverter using the semiconductor elements of Figs. 8 and 9, and Fig. 13 is a pattern configuration of the inverter circuit of Fig. 12. This type of inverters are used, in particular, in the drive circuit in a liquid crystal display. The complementary inverter according to this embodiment of the invention is comprised of a P-type transistor PMOS and an N-type transistor NMOS, wherein each gate and base in each transistor are electrically connected via base resistance rb. A first wiring electrode 105 coupling gate electrode 10 of TFT with input terminal Vin is provided extending to a protrusion of a TFT having a convex pattern, and is electrically connected via a second wiring electrode 106 to the base electrode formed in the protrusion.

Further, electrodes for supplying reference voltage Vss and power supply voltage Vdd to the circuit, as well as output terminal Vout are provided by the second wiring electrode 106. In order to realize a fast circuit operation, intrinsic poly-Si film 301 which has a greater carrier mobility is used as an active layer. Further, in order to prevent degradation of characteristics during operation due to hot carriers, N-type transistors in which hot carriers tend to occur are fabricated to have off-set layer roff as indicated in Fig. 10.

Transistors constituting the inverter circuit

according to this embodiment are enabled to operate at a lower threshold voltage by the action described above. Thereby, operation at a lower supply voltage is enabled, thereby advantageously decreasing power consumption in the circuit. Further, since the high resistance rb is inserted between the input terminal and base electrode 14 of TFT, an input current flowing from the input terminal to the source electrode via base electrode 14 is suppressed, thereby decreasing power consumption.

Eighth Embodiment of the Invention:

Fig. 14 is a cross-sectional view of a complementary (CMOS) inverter circuit comprised of inverted staggered TFTs indicated in Fig. 1, and Fig. 15 is a pattern configuration of the inverter circuit of Fig. 14. The structure of an N-type transistor indicated to the left side in Fig. 14 is the same as in Fig. 1. However, in order to realize a faster circuit operation, intrinsic poly-Si film 301 having a greater carrier mobility is used as its active layer. The structure of a P-type transistor indicated to the right side in Fig. 14 has a complementary structure with respect to that of the above-mentioned N-type transistor. Namely, n-type poly-Si layers 311, 321 are formed selectively and partially on the surface of intrinsic poly-Si film 301, and further, P-type poly-Si layers 331 are formed on the other areas of the surface of intrinsic poly-Si film 301 where n-type poly-Si layers 311, 321 are not formed. In the above P-type transistor, the minority carrier which is electrons

is injected from base electrode 14 and via the n-type poly-Si layer 311, whereby its threshold voltage is decreased by the same action as in the N-type transistor.

Therefore, it becomes possible for the inverter comprised of semiconductor elements according to the invention to be switched at a low input voltage Vin, thereby effectively reducing power consumption in the circuit. Further, it is the same as in the embodiment of Fig. 13 that the bases of the P-type transistor and N-type transistor are connected to their gate electrodes via base resistance rb. Thereby, since an input current flowing from the input terminal to the source electrode through base electrode 14 is suppressed, power consumption can be substantially reduced.

Ninth Embodiment:

Fig. 16 is a plan view of a unit picture element of a TFT active matrix constructed using semiconductor elements of Fig. 1. A cross-section of structure taken along X-X' in Fig. 16 is the same as that of Fig. 1. The active matrix is comprised of: a scanning electrode 100 formed on a glass substrate; a signal electrode 120 formed intercrossing with the scanning electrode; a TFT formed in the vicinity of the intercrossing of these electrode, comprising an intrinsic a-Si film 30, a source electrode 11 and a base electrode 14 formed on the intrinsic a-Si film 30; a pattern of an intrinsic a-Si film 30 formed separate from the intrinsic a-Si film 30 of the TFT and an n-type a-

Si film 31; and a picture element electrode 13 connected to the source electrode 11 of the TFT.

As seen from Figs. 1 and 17, base electrode 14 is arranged to electrically contact p-type a-Si layer 33 which is formed on the surface of intrinsic a-Si film 30 which constitutes the TFT with a pattern of n-type a-Si film 31 which is formed on the surface of an intrinsic a-Si film 30 formed separate from the p-type a-Si layer 33. A contact electrode 15 is formed separate from the base electrode 14 and in contact at its one end with the n-type a-Si film 31 on the intrinsic a-Si film 30, and the other end of the contact electrode 15 is connected with scanning electrode 100 via a throughhole TH provided in a gate insulating film 20.

In this arrangement, the pattern of n-type a-Si film 31 formed on the intrinsic a-Si film 30 which is in contact both with the base electrode 14 and the contact electrode 15 provides for a base resistance corresponding to the base resistance rb in the equivalent circuit of Fig. 7. A value of resistance rb can be controlled by adjusting a gap between the base electrode 14 and the contact electrode 15. Scanning electrode 100 can feed a base current since it is connected to base electrode 14 via the resistance, thereby eliminating necessity of providing additional feeder wiring, thereby preventing the aperture ratio of picture elements from decreasing. Further, since the base resistance is formed utilizing one of the

semiconductor films which constitute the TFT, an additional process for forming the resistance is eliminated, thereby simplifying the process of fabrication.

Fig. 18 is a schematic diagram representing an equivalent circuit of a display constructed using the unit picture elements of Fig. 16. In the drawing of Fig. 16, XiG, Xi+1G,... represent picture signal electrodes each connected to a picture element for forming a green filter G. Likewise, XiB, Xi+B,..., represent picture signal electrodes each connected to a picture element for forming a blue filter, and XiR, Xi+R,..., represent picture signal electrodes each connected to a picture element for forming a red filter. Yi, Yi+1,..., are scanning electrodes 100 for selecting picture element columns X1, X2,..., and these scanning electrodes 100 are connected to a vertical scanning circuit V. The picture signal electrodes are connected to a picture signal drive circuit H. A block of SUP includes a power circuit for obtaining a plurality of stabilized power supplies by dividing a single power supply, and a converter circuit for converting information suitable for display on a cathode ray tube supplied from a host computer to information suitable for display on a liquid crystal display.
Each of a plurality of display regions surrounded by a plurality of scanning electrodes and a plurality of picture signal electrodes on the display area formed on the insulated substrate is comprised of a switching element connected to its associated scanning electrode and picture signal

electrode, a picture element electrode connected to the switching element, a counterposed electrode disposed opposite to the picture element electrode, and a liquid crystal layer interposed between the picture element electrode and the counterposed electrode.

As this switching element provided in each display region, the semiconductor element of the invention is used. By use of the semiconductor element of the invention as the switching element in each display region, an output voltage from vertical scanning circuit V can be decreased, thereby substantially reducing the power consumption in the liquid crystal display.

Tenth Embodiment:

Fig. 19 is a plan view of a planar type TFT according to a tenth embodiment of the invention. Figs. 19(a) and 19(b) depict N-type and P-type TFTs, respectively. Further, Fig. 19(c) is a cross-sectional view taken along Y-Y' in Fig. 19(a), and Fig. (d) is a cross-sectional view taken along X-X' in Fig. 19(a). Other cross-sections along A-A', B-B' and Z-Z' of Figs. 19 (a) and (b) will be shown in Fig. 24 to be described later.

According to this embodiment of the invention, in the same manner as in the fifth embodiment of the invention, an intrinsic semiconductor layer 301 having a convex planar pattern is provided, and a pattern of a gate electrode 10 is disposed in the center thereof, and n+layers 311 and 321 are formed as the source and drain on both sides of the intrinsic

semiconductor layer, respectively. Further, p+layer 331 is formed as the base in the upper protrusion of the convex intrinsic semiconductor layer 301. Further, it is the same as in the fifth embodiment of the invention that in a portion extending from the intrinsic semiconductor layer 301 (channel) under the gate electrode to p+layer 331, there is formed a high resistance layer rb which is not doped with any impurities of P-type or N-type. According to this embodiment, an off-set layer roff made of intrinsic semiconductor layer 301 is formed between n+layers 311, 321 as the source and drain, and the intrinsic semiconductor layer (channel) immediately below the gate electrode 10. Namely, the structures of n+layers 311, 321 as the source and drain and of p+layer 331 as the base are separated by intrinsic semiconductor layer 301. In order to provide for such structures according to this embodiment, a pattern of gate insulating film 20 is formed in a larger size than that of gate electrode 10, then this pattern of gate insulating film 20 is utilized as a mask for forming n+layers 311, 321 as the source and drain, or for p+layer 331 as the base.

Further, as another feature according to this embodiment of the invention, as depicted in Figs. 19(c) and (d), gate electrode 10 has a structure that it extends to the upper protruding portion of the convex type intrinsic semiconductor layer 301, and that it has a planar pattern having devoid portions above p+layer 331 provided as the base and above the high resistance layer rb, and further that

p+layer 331 as the base and gate electrode 10 extending to the protruding portion are electrically connected by base electrode 14. By connecting between p+layer 331 and gate electrode 10, the semiconductor device of this embodiment can be used as a three-terminal semiconductor element. By adoption of this planar circuit pattern of this embodiment of the invention, gate electrode 10 and base electrode 14 can be advantageously connected while minimizing an increase in area to be occupied by the semiconductor device. Further, by removing a part of gate electrode 10 disposed on the high resistance layer rb, changes of values of the high resistance layer rb due to a gate voltage can be eliminated, thereby providing a stabilized base current limiting function. Still further, since off-set layer roff in addition to the high resistance layer rb acts to limit the base current, an excess base current injection can be more effectively prevented, thereby ensuring operation at a low power until the gate voltage is increased substantially. Furthermore, since the off-set layer acts to mitigate electrical field present between source electrode 11 and drain electrode 12, generation of hot carriers is suppressed, thereby substantially improving reliability of the semiconductor device.

Fig. 20(a) is a plan view of a unit picture element of a TFT active matrix constructed using the semiconductor device of Fig. 19(a), and Fig. 20(b) is a cross-sectional view taken along X-X' in Fig. 20(a).

This active matrix is comprised of: a scanning electrode 100 formed on the surface of a glass substrate; a signal electrode 120 formed intercrossing with the scanning electrode; a TFT formed in the vicinity of the intercrossing of these electrodes, including an intrinsic poly-Si film 301, a source electrode 11 and a base electrode 14 each connected to the intrinsic poly-Si film 301 via a throughhole; and a picture element electrode 14 connected to source electrode 11 of the TFT. As can be seen from Fig. 20(b) and as indicated in Fig. 19, base electrode 14 connects n+layer 331 and gate electrode 10. By connecting base electrode 14 and scanning electrode 100 in this manner according to the invention, scanning electrode 100 is also adapted to feed a base current, hence eliminating necessity of providing additional feeder wiring, thereby preventing the aperture ratio of the picture element from being reduced. Still further, since the base resistance can be formed using a part of the semiconductor film which constitutes the TFT, additional process for forming the resistance is eliminated, thereby simplifying the process of manufacture of the semiconductor device.

Fig. 21 indicates an equivalent circuit of a display which is provided by integrating on a same substrate the drive circuits constructed using the CMOS inverter of Figs. 12 and 13, and the TFT active matrix of Fig. 20. This display is comprised of: a TFT active matrix 50 according to the invention; a vertical scanning circuit 51 for

driving the matrix; a horizontal scanning circuit 53 for dividing a video signal per scan into a plurality of blocks and supplying them by time-sharing; data signal lines Vdr1, Vdg1, Vdb1, ..., for supplying video signal data; and a switch matrix circuit 52 for supplying video signals divided into plurality of blocks to the active matrix. Vertical scanning circuit 51 and horizontal scanning circuit 53 are constructed using a shift register and a buffer (to be described later with reference to Fig. 22), and are driven by clock signals CL1, CL2, and CKV. Fig. 22 depicts a scanning circuit corresponding to one scanning line. In the drawing of Fig. 22, numeral 70 depicts a P-type transistor and 71 depicts an N-type transistor. Each of these transistors has a structure in which its base and gate are connected via resistance rb. The shift register takes timing using two phase clocks (Vcp1, Vcp2) and its reversed clocks (Vcp1, Vcp2), reverses an input voltage and shifts it then to be transferred to the buffer. At the same time, this signal to be transferred to the buffer is also input as an input voltage to a shift register corresponding to the subsequent scanning line. The buffer outputs a pulse voltage of a maximum voltage of Vdd2, which becomes a scanning voltage for the active matrix display.

The shift register of a complementary type TFT using the semiconductor device according to the invention is confirmed to be able to operate at a half of the power consumption normally required with the conventional shift

registers using conventional TFTs. Further, since TFTs for constituting the active matrix are constructed using the semiconductor device according to the invention, the output level or Vdd2 of the scanning circuit has been halved compared to the conventional level. Thereby, a total power consumption of the whole active matrix substrate has been reduced to one third of the conventional.

Although the planar type TFT was used in the above-mentioned embodiment of the invention, it is not limited thereto, and the inverted staggered type or staggered type TFTs as indicated in Figs 1 or 2 may be used as well. It should be noted, however, that since the planar type semiconductor device in which parasitic capacitance between the gate and source or drain can be reduced, it ensures a faster operation to be attained.

Eleventh Embodiment:

Figs. 23(a)-(d) illustrate respective fabrication steps in cross-sectional view of the semiconductor device of the invention depicted in Fig. 1. A Cr film is accumulated by sputtering on the surface of a glass substrate 1 to a thickness of 100 nm, and is patterned into a predetermined planar shape using the known photolighography so as to provide a gate electrode 10. Then, over the entire area of the substrate including the surface of the gate electrode 10, there are formed a silicon nitride (SiN) film 20, an intrinsic amorphous silicon (a-Si) film 30, and an n-type a-Si film 31,

sequentially by the plasma CVD method. Respective film thicknesses are 350 nm for the SiN film, 200 nm for the intrinsic a-Si film and 40 nm for the n-type a-Si film (see Fig. 23(a)).

After having patterned the intrinsic a-Si film and n-type a-Si film into predetermined planar shapes, a photoresist PR having a predetermined planar shape is formed on n-type a-Si film 31 such that by using the photoresist as its mask, n-type a-Si film 31 is patterned into a predetermined shape by plasma etching, that is, the n-type a-Si film 31 is separated into two parts of n-type a-Si film 31 and n-type a-Si film 32 (see Fig. 23(b).

Subsequently, an ion beam IB which contains boron is irradiated over the entire area on the substrate with the photoresist still remaining, thereby forming a p-type a-Si film 33 in an area on the surface of the intrinsic a-Si film 30 from which the n-type a-Si film 31 was removed partially (refer to Fig. 23(c)).

Then, after having removed photoresist PR, Cr and Al are sputtered to a thickness of 40 nm and 400 nm, respectively, and which are patterned into each predetermined shape so as to provide for a source electrode 11, drain electrode 12 and base electrode 14, respectively. Finally, a SiN film is formed by the plasma CVD method to a thickness of 400 nm as a passivation film 22, thus completing the fabrication of the semiconductor element of the invention (refer to Fig. 23 (d)).

According to this embodiment of the invention, p-type a-Si layer 33 is formed by self-aligning with respect to the patterns of n-type a-Si layers 31 and 32. That is, p-type a-Si layer 33 is formed utilizing the patterns of n-type a-Si layers 31, 31 as its own mask. Thereby, both the n-type a-Si layers 31, 32 and p-type a-Si layer 33 can be formed advantageously by one photolithographic process according to the invention, thereby simplifying the process of fabrication and reducing the cost of manufacture.

Twelfth Embodiment:

With reference to Figs 24(a)-(f), fabrication processes of fabricating the complementary (CMOS) semiconductor device indicated in Fig. 19 according to the invention are illustrated in respective cross-sectional views. In the drawings of Fig. 24, sections indicated by A-A', Y-Y', B-B', Z-Z' correspond respectively to cross-sections indicated by A-A7, Y-Y', B-B', Z-Z' in Figs. 19.

After forming an intrinsic a-Si film 30 on a glass substrate to a thickness 50 nm by the LPCVD method, a high intensity XeCl excimer laser beam LASER is irradiated at an energy density of 330 mJ/cm^2 from the above such that the intrinsic a-Si film 30 is caused to melt and recrystallize to obtain an intrinsic polycrystalline silicon (poly-Si) film 301 (refer to Fig. 24(a)).

After patterning the poly-Si film 301 into a predetermined planar pattern, SiO_2 film is formed to a thickness 100 nm by the plasma CVD, and Al film is formed

to a thickness 100 nm by the sputtering method, and they are patterned into respective planar patterns so as to provide a gate insulating film 20 and a gate electrode 10 (refer to Fig. 24(b)).

After forming a photoresist pattern PR1 having a predetermined shape, and by using patterns of the photoresist PR1 and gate electrode 10 as its mask, an ion beam IP which contains phosphor is irradiated to form an n-type poly-Si layer 311 (refer to Fig. 24(c)).

After having removed the photoresist pattern PR1, another photoresist pattern PR2 is formed, and by using patterns of the photoresist PR2 and gate electrode 10 as its mask, an ion bean which contains boron is irradiated thereover, thereby forming p-type poly-Si layers 331. After having removed the photoresist pattern PR2, an XeCl excimer laser beam is irradiated once again thereover at an energy density of 200 mJ/cm^2 so as to activate injected phosphor and boron, thereby decreasing electrical resistance of n-type poly-Si layer 311 and p-type poly-Si layer 321 (refer to Fig. 24(d)).

Then, an SiO_2 film is formed by the plasma CVD method to a thickness of 300 nm as a passivation film 22, which is then patterned into a predetermined pattern as depicted in Fig. 24(e).

Finally, Cr and Al are deposited to thicknesses of 40 nm and 400 nm, respectively by sputtering, then they are patterned into respective patterns to provide for a source

electrode 11, drain electrode 12 and base electrode 14, thereby completing the process of fabrication of the semiconductor element of the invention as indicated in Fig. 24(f).

Thirteenth Embodiment:

Fig. 26 is a schematic block diagram in cross-section of a liquid crystal display according to the invention. On a glass substrate 1 disposed below a liquid crystal layer 506 disposed in the center portion in Fig. 26, there are formed a scanning signal electrode 10 and a picture signal electrode 120 both intercrossing in matrix, a TFT which is formed in the vicinity of the intercrossing, and a picture element electrode 13 made of ITO which is driven via the TFT. On a counterposed glass substrate 508 disposed opposite to glass substrate 1 with respect to the liquid crystal layer 506 which is interposed therebetween, there are formed a counterposed electrode 510 made of ITO, color filter 507, color filter protection film 511 and a shading film 512 which forms a shading black matrix pattern. The center portion of Fig. 26 represents a cross-section of one picture element portion, the left side portion of the drawing represents the left side end portion in cross-section of a pair of glass substrates 1 and 508 wherein an external lead terminal is provided, and the right side portion of the drawing represents the right side end portion in cross-section of the pair of glass substrates 1 and 508 wherein no external lead terminal is provided.

Seal material SL provided on both sides of the left end portion and the right end portion is formed so as to seal liquid crystal layer 506, and is formed along the whole portion of periphery of the pair of glass substrates 1 and 508 except for a liquid crystal injection port (not shown). The seal material may be made of epoxy resin, for example. Counterposed electrode 510 provided on the counterposed glass substrate 508 is connected at least at a part thereof to the external lead wiring on glass substrate 1 via silver paste SIL. This external connection wiring is formed in the same fabrication process as each of those for scanning signal wiring 10, source electrode 11, picture signal wiring 120 and base electrode 14. Respective layers of orientation film ORI1, ORI2, picture element electrode 13, protection film 22, gate SiN film 20 are formed inside the seal material SL. Polarization plate 505 is formed on each outer surface of the pair of glass substrates 1 and 508.

Liquid crystal layer 506 is interposed between the upper orientation film ORI1 and the bottom orientation film ORI2 which set orientation of liquid crystal molecules, and is sealed by the seal material SL. The bottom orientation film ORI1 is formed in the upper portion of protection film 20 on the glass substrate 1. On the internal surface of counterposed glass substrate 508, there are formed sequentially by lamination shading film 512, color filter 507, color filter protection film 511, counterposed electrode 510 and the upper orientation film ORI2. This

liquid crystal display is constructed by the steps of: separately forming the layers on the glass substrate 1 and the layers on the counterposed glass substrate 508; laminating the glass substrate 1 and the counterposed glass substrate 508; and sealing liquid crystal 506 in a space therebetween. Then, a TFT driven color liquid crystal display is provided by enabling adjustment of transparency of light from a backlight BL by picture element electrode 13.

Since the semiconductor device according to the invention described above is used as TFT to drive the picture element electrode 13 at a reduced voltage, liquid crystal displays capable of operating at a reduced power consumption have been realized.

Fourteenth Embodiment:

Fig. 27 is a schematic block diagram in cross-section of a reflection type liquid crystal display according to the invention. Only a cross-section of a picture element portion is indicated. On a glass substrate 1 provided below a liquid crystal layer 506 which is in the center portion in Fig. 27, there are formed scanning signal electrode 10 and picture signal electrode 120 intersecting each other in a matrix, and a TFT which is formed in the vicinity of the intersection for driving a picture element electrode 130 provided thereon. According to this embodiment of the invention, picture element electrode 130 is made of Al. On the internal surface of counterposed glass substrate 508 disposed opposite to the glass substrate 1 via liquid

crystal layer 506, there are formed counterposed electrode 510, color filter 507, color filter protection film 511, and a shading film 512 which forms a shading black matrix pattern. Further, phase plate 530 for shifting phase of light and polarization plate 505 are formed on the outer surface of counterposed glass substrate 1, 508. Respective layers of orientation films ORI1and ORI2, picture element electrode 13, protection film 22, and gate SiN film 20 are formed inside a seal material (not shown). Liquid crystal layer 506 is inserted between the upper and the bottom orientation films ORI1and ORI2 which set orientation of liquid crystal molecules, and is sealed by the seal material. The bottom orientation film ORI1 is formed in the upper portion of protection film 22 on the glass substrate 1. On the internal surface of counterposed glass substrate 508, there are formed in lamination sequentially a shading film 512, color filter 507, color filter protection film 511, counterposed electrode 510 and the upper orientation film ORI2. This liquid crystal display of the invention is fabricated by the steps of: separately forming layers on the glass substrate 1 and on the counterposed substrate 508; then, laminating both the glass substrate 1 and the counterposed substrate 508; and sealing liquid crystal 506 in a space therebetween.

Since this embodiment of the invention is of a reflection type display, incident light comes from a light source provided outside counterposed glass substrate 508, and

this incident light is reflected from a mirror-finished surface of picture element electrode 130. A TFT driven reflection type color liquid crystal display according to the invention is thus provided in which intensity of reflected light is adjusted in the portion of liquid crystal layer 506. In this type of reflection type display, since the backlight which consumes considerable electric power is eliminated, a low power consuming liquid crystal display can be realized. Further, if the above-mentioned semiconductor device of the invention is utilized as TFTs for driving picture element electrode 130 and/or TFTs for constituting associated peripheral drive circuits, since the electric power consumed in the active matrix substrate components can be reduced, there can be realized a very low power consuming liquid crystal display. This type of liquid crystal display of the invention is most preferable for use as an image display device in a portable information terminal which is driven by dry cells.

As described heretofore, there is such an advantage according to the invention that the field effect semiconductor device of the invention can reduce its threshold voltage substantially, thereby decreasing its operating voltage of its circuit or active matrix, and thereby reducing the power consumption in the display.

This Sheet Has Been Replaced



THIS SHEET HAS BEEN REPLACED

WHAT IS CLAIMED IS

1. A liquid crystal display having a pair of substrates at least one of which is transparent and a liquid crystal layer held between said pair of substrates, wherein

on one of said pair of substrates there are formed a plurality of semiconductor elements disposed in a matrix; wherein

each of said plurality of semiconductor elements comprises: a first, a second, a third and a fourth electrodes; a pair of a first conducting type semiconductor layers separate from each other and connected to said second and said third electrodes, respectively; an intrinsic semiconductor layer provided in contact with both the pair of the first conducting type semiconductor layers; and a second conducting type semiconductor layer formed on the intrinsic semiconductor layer, and wherein

said first electrode is formed on said intrinsic semiconductor layer via an insulating film, and

said fourth electrode is formed on the second conducting semiconductor layer which is formed on said intrinsic semiconductor layer.

2. A liquid crystal display according to claim 1, wherein said pair of the first conducting type semiconductor layers and said second conducting type semiconductor layer are separated from each other by said



intrinsic semiconductor layer.

3. A liquid crystal display according to claim 2, wherein the intrinsic semiconductor layer has a region extending greater than a region of the insulating layer toward said pair of the first conducting type semiconductor layers on said substrate.

4. A liquid crystal display according to claim 1, wherein said first electrode and said fourth electrode are electrically connected via a resistance.

5. A liquid crystal display according to claim 1, wherein said intrinsic semiconductor layer, said first conducting type semiconductor layers, and said second conducting type semiconductor layer are comprised of a semiconductor film made of either one of silicon, silicon germanium and silicon carbide.

6. A liquid crystal display according to claim 1 wherein said intrinsic semiconductor layer, said pair of the first conducting type semiconductor layers, and the second conducting type semiconductor layer are made of a polycrystalline silicon film, respectively.

7. A liquid crystal display according to claim 1, wherein said plurality of the first conducting type layers

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and said second conducting type semiconductor layer are an N-type semiconductor and a P-type semiconductor, respectively.

8. A liquid crystal display according to claim 1, wherein said intrinsic semiconductor layer is injected with a current carrier from the fourth electrode via the second conducting type semiconductor layer.

9. A liquid crystal display according to claim 1, wherein said first, said second, said third and said fourth electrodes correspond to a gate, a source, a drain and a base electrodes, respectively.

10. A liquid crystal display according to claim 1, wherein each of said plurality of semiconductor elements has a structure either of a planar type, an inverted staggered type or a normal staggered type.

11. A liquid crystal display according to claim 10 wherein said first electrode is formed on one of said pair of substrates, said insulating layer is formed on said first electrode, said intrinsic semiconductor layer is formed on said insulating layer, and said pair of the first conducting type semiconductor layers are formed on said intrinsic semiconductor layer.

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12. A liquid crystal display according to claim 10 wherein said second electrode, said third electrode and said fourth electrode are formed on one of said pair of substrates.

13. A liquid crystal display having a pair of substrates at least one of which is transparent, and a liquid crystal layer which is held between said pair of substrates, wherein

one of said pair of substrates has a display region and a drive circuit region for driving said display region disposed on the surface thereof, wherein

in said drive circuit region, there are formed a plurality of complementary N-type and P-type semiconductor elements which constitute a shift register, wherein

each one of said N-type semiconductor elements formed in said drive circuit region comprises: a first, a second, a third and a fourth electrodes; a pair of N-type conducting semiconductor layers separated from each other and connected to said second and the third electrodes, respectively; an intrinsic semiconductor layer connected to said pair of N-type conducting semiconductor layers; and a P-type conducting semiconductor layer which is formed partially on said intrinsic semiconductor layer, wherein said first electrode is formed on said intrinsic semiconductor layer via an insulating film, and said fourth electrode is formed on the P-type conducting semiconductor layer which is formed



partially on said intrinsic semiconductor layer, and

each of said plurality of P-type conducting semiconductor layers formed in said drive circuit region comprises: a first, a second, a third and a fourth electrodes; a pair of P-type conducting semiconductor layers which are formed separate from each other and connected to said second and said third electrodes, respectively; an intrinsic semiconductor layer connected to said pair of P-type conducting semiconductor layers; and an N-type conducting semiconductor layer formed on the intrinsic semiconductor layer, and wherein said first electrode is formed on said intrinsic semiconductor layer via an insulating film, and said fourth electrode is formed on the N-type conducting semiconductor layer which is formed on said intrinsic semiconductor layer.

14. A liquid crystal display according to claim 13, wherein said semiconductor element formed in said display region is an N-type semiconductor element.

15. A liquid crystal display according to claim 14, wherein said N-type semiconductor element formed in said display region comprises: a first, a second, a third and a fourth electrodes; a pair of N-type conducting semiconductor elements formed separate from each other and connected to said second and said third electrodes, respectively; an intrinsic semiconductor layer connected to

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said pair of N-type conducting semiconductor layers; and a P-type conducting semiconductor layer formed on the intrinsic semiconductor layer, wherein said first electrode is formed on said intrinsic semiconductor layer via an insulating film, and said fourth electrode is formed on the P-type conducting semiconductor layer which is formed said intrinsic semiconductor layer.

16. A liquid crystal display according to claim 13, wherein the semiconductor elements formed in said display region and said drive circuit region are either of a planar type, inverted staggered type and normally staggered type.

17. A liquid crystal display according to claim 13, wherein the intrinsic semiconductor layer, N-type conducting semiconductor layer and P-type conducting semiconductor layer are made of a polycrystalline silicon film, respectively.

18. A liquid crystal display according to claim 13, wherein said pair of N-type conducting semiconductor layers and said P-type conducting semiconductor layer are separated from each other by said intrinsic semiconductor layer.

19. A liquid crystal display according to claim 18, wherein a region of said intrinsic semiconductor layer in a vertical direction of said substrate extends more than a

region of said insulating layer at least toward said pair of N-type conducting semiconductor layers.

20. A liquid crystal display according to claim 13, wherein said first and said fourth electrodes are electrically connected via an electric resistance.

21. A liquid crystal display having a pair of substrates at least one of which is transparent, and a liquid crystal layer which is held between said pair of substrates, wherein

one of said pair of substrates has a display region and a drive circuit region for driving said display region disposed on the surface thereof, wherein

said display region has: a plurality of scanning signal electrodes and a plurality of picture signal electrodes intercrossing with said plurality of scanning electrodes in a matrix; a plurality of N-type semiconductor elements formed at crosspoints corresponding to intersections between said plurality of scanning signal electrodes and said plurality of picture signal electrodes; and a plurality of picture element electrodes connected to said semiconductor elements respectively, and

said drive circuit region has a plurality of complementary N-type and P-type semiconductor elements formed thereon, which constitute a vertical scanning circuit and a picture signal drive circuit, wherein,



said N-type semiconductor element formed in said display region or in said drive circuit region comprises: a first, a second, a third and a fourth electrodes; N-type conducting semiconductor layers connected to said second and said third electrodes, respectively; an intrinsic semiconductor layer connected to these N-type conducting semiconductor layers; and a P-type conducting semiconductor layer formed on the intrinsic semiconductor layer, wherein said first electrode is formed on the intrinsic semiconductor layer via an insulating film, and said fourth electrode is formed on the surface of the P-type semiconductor layer which is formed on said intrinsic semiconductor layer, and

said P-type semiconductor element formed in said drive circuit region comprises: a first, a second, a third and a fourth electrodes; P-type conducting semiconductor layers connected to said second and said third electrodes, respectively; an intrinsic semiconductor element connected to these P-type conducting semiconductor layers; and an N-type semiconductor element formed on the intrinsic semiconductor layer, wherein said first electrode is formed on the intrinsic semiconductor element via an insulating film, and said fourth electrode is formed on the N-type conducting semiconductor layer which is formed on the intrinsic semiconductor element, and wherein

said first electrode is connected to said scanning signal electrode, said second electrode is connected to said picture signal electrode, and said fourth electrode is



connected to said first electrode via an electric resistance.

22. A liquid crystal display according to claim 21, wherein said pair of N-type conducting semiconductor elements and said P-type conducting semiconductor element are separated from each other by said intrinsic semiconductor layer.

23. A liquid crystal display according to claim 22, wherein said intrinsic semiconductor layer has a region extending further than a region of said insulating layer toward said pair of N-type conducting semiconductor layers on said substrate.

