

PLASMA CONFINEMENT RING ASSEMBLIES HAVING REDUCED POLYMER DEPOSITION CHARACTERISTICS

BACKGROUND

5 [0001] Plasma processing chambers can include an upper electrode and a lower electrode. The upper electrode typically faces a substrate support adapted to support a semiconductor substrate during plasma processing. During the plasma processing, power is supplied to one or both electrodes to activate the process gas and produce the plasma to process the substrate.

10 [0002] Plasma etching can be performed in plasma processing chambers to etch selected materials provided as layers on a semiconductor substrate. The processing conditions are chosen so that the plasma etches desired features in selected portions of the layers.

SUMMARY

15 [0003] A preferred embodiment of a plasma confinement ring assembly for a plasma processing chamber comprises a plurality of plasma confinement rings. Each of the plasma confinement rings includes an inner portion having a plasma-exposed inner diametric surface, an outer portion disposed radially outwardly from the inner portion, and at least one thermal choke. The thermal choke is adapted to reduce heat conduction from the inner
20 portion to the outer portion when the inner diametric surface is exposed to plasma in the plasma processing chamber. As a result, the inner diametric surface reaches a sufficiently high temperature to substantially prevent polymer deposition thereon.

25 [0004] Another preferred embodiment of a plasma confinement ring assembly for a plasma processing chamber comprises a mounting ring and a plurality of plasma confinement rings adapted to be suspended below the mounting ring. The plasma confinement rings comprise an upper plasma confinement ring and a plurality of lower plasma confinement rings. The upper plasma confinement ring includes a top surface facing the mounting
30 ring and a plasma-exposed bottom surface disposed radially inward from the

second plasma confinement rings. At least a portion of the top surface of the upper plasma confinement ring is opaque to IR radiation so as to enhance heating of the upper plasma confinement ring. As a result, the bottom surface reaches a sufficiently high temperature to substantially prevent polymer deposition thereon when the bottom surface is exposed to the plasma.

[0005] A preferred embodiment of a method of processing a semiconductor substrate in a plasma processing chamber comprises supplying a process gas into a plasma processing chamber comprising a plurality of plasma confinement rings, which each include a plasma-exposed surface; and producing a plasma from the process gas and etching a semiconductor substrate in the plasma processing chamber. During the etching, the plasma-exposed surfaces of the plasma confinement rings reach a sufficiently high temperature to substantially prevent polymer deposition thereon.

BRIEF DESCRIPTION OF THE DRAWING FIGURES

[0006] FIG. 1 illustrates a portion of a preferred embodiment of a plasma confinement ring assembly.

[0007] FIG. 2 illustrates a top plan view of a portion of a preferred embodiment of a plasma confinement ring of the plasma confinement ring assembly, wherein the ring includes a thermal choke.

[0008] FIG. 3 is an enlarged partial top view of the plasma confinement ring shown in FIG. 2.

[0009] FIG. 4 illustrates a side view of another preferred embodiment of a plasma confinement ring of the plasma confinement ring assembly, which has a two-piece construction.

[0010] FIG. 5 illustrates a plasma processing chamber including a preferred embodiment of the plasma confinement ring assembly.

[0011] FIG. 6 depicts an embodiment of the plasma confinement ring assembly without thermal chokes that was used in Examples 1 and 2.

[0012] FIG. 7 depicts an embodiment of the plasma confinement ring assembly including thermal chokes that was used in Example 3.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

5 [0013] Parallel-plate plasma processing chambers, such as capacitively-coupled chambers, include an upper electrode, such as a showerhead electrode, and a lower electrode. The upper electrode typically faces a semiconductor substrate to be processed. During the plasma processing, power is supplied to one or both electrodes to activate the process gas and produce the plasma to process the substrate.

10 [0014] Interior surfaces of such plasma processing chambers can be powered surfaces (e.g., "RF hot surfaces"), grounded surfaces, or floating surfaces (comprised of insulating materials). Different energy is supplied to, or impinges, on these different types of surfaces during plasma processing. Particularly, heating of a chamber part in a parallel-plate plasma processing chamber depends upon the ion energy and the ion flux supplied to the part's
15 exposed surfaces, and on the infrared (IR) energy absorption characteristics of the part. Grounded (return path) surfaces and powered surfaces receive significant ion energy from plasma, which causes these surfaces to be heated more than floating parts or surfaces, and also to reach significantly
20 different temperatures.

[0015] Highly-polymerizing process gas chemistries, such as process gases containing fluorocarbons, hydrofluorocarbons, or precursors of such gases, can be used to etch dielectric materials, such as silicon oxide. During such plasma etch processes, polymer tends to deposit on some internal
25 surfaces of the plasma processing chamber. The polymer deposits are undesirable because they can flake off of the surfaces and contaminate processed substrates (e.g., processed wafers), as well as the chamber. However, as device features continue to shrink, it becomes increasingly desirable to maintain plasma-exposed chamber surfaces clean from wafer-to-wafer to achieve repeatable process results. Accordingly, it is desirable to
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reduce, and preferably to avoid, such polymer deposits on internal surfaces of chamber parts.

[0016] Generally, polymer deposits are more likely to form on cooler plasma-exposed surfaces of the plasma processing chamber during plasma processing operations. Floating surfaces tend to be cooler surfaces and consequently are generally more prone to develop polymer buildup on them as compared to powered or grounded surfaces. The temperature increase, ΔT , of a plasma-exposed part or surface during plasma processing depends on the amount of heat, Q , added to the part or surface, and the mass, m , and the specific heat, c , of the part; according to the following relationship: $Q = mc\Delta T$. Accordingly, for a given amount of heat added to a part, increasing the part mass decreases the increase in temperature of the part. Consequently, a part having a high mass may not reach a sufficiently high temperature during plasma processing to avoid polymer deposition on plasma exposed surfaces of the part. Increasing the heat capacity of a part also decreases the temperature reached by the part for a given amount of heat added to the part.

[0017] In addition, during plasma processing, heat can be transferred to and/or from a part to other chamber surfaces by thermal conduction (when the part is in physical contact with another surface), radiation (when electromagnetic waves carry heat to and/or from the part) and convection (when heat is carried by a moving fluid in the chamber). Convective heat losses from parts increase with increasing chamber pressure.

[0018] The problem of polymer deposition on plasma-exposed surfaces of some parts in plasma processing chambers can be addressed by actively heating the part(s). For example, chamber walls can be heated to keep their plasma-exposed interior surface(s) at a sufficiently high temperature to avoid polymer deposition on the surface(s). Active temperature control of showerhead electrode assemblies and electrostatic chucks can also be used. However, as such surfaces are powered or grounded and consequently subject to high ion energy, polymer deposition on these

surfaces is less likely to occur than on a floating surface even without active heating of the surfaces.

[0019] Alternatively, the polymer deposition problem can be addressed by removing as-formed polymer deposits from surfaces. For example, polymer deposits can be removed by employing aggressive plasma chemistries. Alternatively, the plasma chamber can be opened and a wet cleaning technique can be used to remove polymer deposits from chamber surfaces. However, such cleaning techniques reduce process throughput.

[0020] In order to achieve desirable process efficiency and etch uniformity, plasma can be confined within a plasma confinement zone defined between the upper and lower electrodes of a parallel-plate plasma processing chamber. Plasma confinement ring assemblies can be used to provide such plasma confinement. Exemplary plasma confinement ring assemblies are disclosed in commonly-owned U.S. Patent Nos. 5,534,751; 5,998,932; 6,019,060; 6,178,919 and 6,527,911, each of which is incorporated herein by reference in its entirety. As described in U.S. Patent No. 5,534,751, a plasma confinement ring assembly can include a plurality of plasma confinement rings, which are arranged in a stack to define a plurality of gas passages extending radially through the rings from an inner to an outer surface. Charged particles in the plasma are neutralized as the particles pass through the passages, thereby minimizing the tendency for a discharge outside the plasma confinement zone (i.e., "unconfinement" of the plasma).

[0021] As also described in U.S. Patent No. 5,534,751, plasma confinement ring assemblies may confine polymer deposition during plasma etch processes to only the plasma confinement rings themselves. However, it is desirable to avoid such polymer deposition on the confinement rings in order to avoid potential chamber and substrate contamination problems, as well as to avoid additional chamber cleaning steps to remove as-formed polymer deposits from the plasma confinement rings.

[0022] In light of the above-described polymer deposition problem, it has been determined that plasma confinement ring assemblies can be provided

that include confinement rings adapted to reach sufficiently high temperatures on plasma-exposed surfaces of the rings to avoid polymer deposition on those surfaces, without employing active heating of the surfaces. More particularly, the plasma confinement rings are adapted to
5 localize heating at selected portions of the rings that include the plasma exposed surfaces. Heating is localized at these selected portions by providing one or more thermal chokes in each of the rings at selected locations to thereby reduce heat conduction from those portions to other portions of the rings that otherwise act as heat sinks in confinement rings
10 without the thermal chokes.

[0023] FIG. 1 depicts a preferred embodiment of a plasma confinement ring assembly 10. The plasma confinement ring assembly 10 comprises, in a concentric arrangement, a mounting ring 12 and plasma confinement rings 14, 16, 18 and 20 suspended from the mounting ring 12. The mounting ring
15 12 and plasma confinement rings 14, 16, 18 and 20 are vertically-movable to provide adjustment. The number of plasma confinement rings of the assembly is not limited to four rings, as shown; alternatively, there can be less than four rings, e.g., three rings, or more than four rings, e.g., five, six or more rings.

[0024] The mounting ring 12 and the plasma confinement rings 14, 16, 18 and 20 are floating parts comprised of a suitable electrically insulating material (dielectric). The insulating material can be, for example, quartz, fused silica, silicon nitride, alumina, or a plastic material. High-purity quartz is a preferred material for use in etch processes for dielectric materials. In
25 the embodiment, the mounting ring 12 and each of the plasma confinement rings 14, 16, 18 and 20 are of a single piece of the insulating material.

[0025] As shown in FIG. 1, the plasma confinement rings 14, 16, 18 and 20 are connected to the mounting ring 12 by a hanger 22 configured to extend through holes 24 in each of the plasma confinement rings 14, 16, 18
30 and 20. An insert 26 is preferably provided in each hole 24 to prevent direct contact between the hanger 22 and the plasma confinement rings 14, 16, 18 and 20. A spring 28 is preferably provided on an inner shaft 30 of the

hanger 22 to resiliently bias the hanger 22 with respect to a fitting 32 on the hanger 22.

[0026] For etching round semiconductor substrates, such as wafers, the plasma confinement rings 14, 16, 18 and 20 include an inner diametric surface 34, 36, 38 and 40, respectively, and an outer diametric surface 42, 44, 46 and 48, respectively. The inner diametric surfaces 34, 36, 38 and 40 are plasma-exposed surfaces. As shown in FIG. 1, the uppermost plasma confinement ring 14 has a greater width in the radial direction than the plasma confinement rings 16, 18 and 20. As also shown, the inner diametric surfaces 36, 38 and 40 of the respective plasma confinement rings 16, 18 and 20 are preferably vertically aligned.

[0027] The inner diametric surface 34 of the plasma confinement ring 14 is preferably vertically aligned with the inner diametric surface 50 of the mounting ring 12. By this arrangement, the plasma confinement ring 14 overlies the bottom surface 52 of the mounting ring 12. It has been determined that due to the relatively large thermal mass of the mounting ring 12, without the plasma confinement ring 14, the bottom surface 52 of the mounting ring 12 does not reach a sufficiently high temperature to prevent polymer deposition on the bottom surface 52 during plasma processing. By incorporating the plasma confinement ring 14 separated from the bottom surface 52, the bottom surface 52 is protected from exposure to plasma and polymer deposition on the bottom surface 52 is preferably minimized.

[0028] In the embodiment, the plasma confinement rings 14, 16, 18 and 20 include thermal chokes 54, 56, 58 and 60, respectively. Heat is supplied to the plasma confinement rings 14, 16, 18 and 20 by plasma and other heating effects during plasma etching processes. The thermal chokes 54, 56, 58 and 60 reduce heat conduction in the radial outward direction from the locations of the thermal chokes 54, 56, 58 and 60, to thereby enhance heating of the inner portion of the respective plasma confinement rings 14, 16, 18 and 20 defined between the thermal chokes 54, 56, 58 and 60 and the inner diametric surfaces 34, 36, 38 and 40, respectively. Consequently, each of the inner diametric surfaces 34, 36, 38 and 40 preferably reaches a

sufficiently high temperature to substantially prevent polymer deposition on these surfaces during plasma processing.

[0029] FIGs. 2 and 3 depict a portion of a preferred embodiment of a plasma confinement ring 120 including a thermal choke 160. In the embodiment, the mounting ring and/or one or more of the other plasma confinement rings of the plasma confinement ring assembly can also include a thermal choke configured as shown in FIGs. 2 and 3.

[0030] The illustrated thermal choke 160 comprises a plurality of inner slots 161 arranged in a discontinuous first circular pattern, and a plurality of outer slots 163 spaced outwardly from the inner slots and arranged in a concentric discontinuous second circular pattern. Adjacent inner slots 161 are separated by inner regions 165, and adjacent outer slots 163 are separated by outer regions 167. As shown in FIG. 2, the inner regions 165 and outer regions 167 are offset from each other around the plasma confinement ring 120. The inner slots 161 and the outer slots 163 preferably extend completely through the thickness of the plasma confinement ring 120. This construction and placement of the thermal choke 160 reduces radial heat transfer to the outer portion 169 of the plasma confinement ring 120, such that the inner diametric surface 140 reaches a sufficiently high temperature to substantially prevent polymer deposition on this surface during plasma processing.

[0031] The inner slots 161 and outer slots 163 preferably have a width of from about 0.005 inch to about 0.020 inch. In a preferred embodiment, the inner slots 161 and 163 are formed by a laser ablation technique.

[0032] In another preferred embodiment, one or more of the plasma confinement rings of the plasma confinement ring assembly 10 has a multi-piece construction. For example, the embodiment of the plasma confinement ring 220 shown in FIG. 4 has a two-piece construction and comprises an inner ring portion 221 and an outer ring portion 223. The inner ring portion 221 includes a plasma-exposed inner diametric surface 240. The inner ring portion 221 and the outer portion 223 are preferably comprised of the same insulating material.

[0033] In the plasma confinement ring 220, the inner ring portion 221 and outer ring portion 223 are configured to minimize contact between surfaces of the inner ring portion 221 and the outer ring portion 223 at the region 227 (which contact occurs due to gravity). At least one gap is defined between
5 opposed surfaces of the inner ring portion 221 and outer ring portion 223. In the embodiment, the gaps 225 act as thermal chokes. By this construction of the plasma confinement ring 220, heat conduction from the inner ring portion 221 to the outer ring portion 223 occurs only at the region 227 where there is surface contact when the inner diametric surface 240 of inner ring
10 portion 221 is exposed to plasma. Consequently, the inner diametric surface 240 can reach a sufficiently high temperature to substantially prevent polymer deposition on the surface.

[0034] In a preferred embodiment, at least one surface of one or more of the plasma confinement rings of the plasma confinement ring assembly can
15 be roughened and/or coated with a material that is opaque to IR (infrared) radiation and can block transmission of the IR radiation. In the embodiment, IR radiation incident on the confinement ring is transmitted through the body of the confinement ring, but is blocked by the roughened and/or coated surface. For example, the confinement ring can be comprised of quartz, or
20 another IR transparent insulating material. By blocking the IR radiation, heating of a selected portion of the confinement ring partially defined by the roughened and/or coated surface is enhanced.

[0035] Selected surfaces of the plasma confinement rings can be roughened by a suitable technique, such as shot peening or by machining
25 the surface using a diamond tool that produces a pitted surface. The surfaces can be coated with a suitable IR opaque material. Surfaces that are not exposed to plasma can be coated with alumina.

[0036] For example, as shown in FIG. 1, the upper surface 62 of the plasma confinement ring 14 can be roughened and/or coated with an IR
30 opaque material in the region between the inner diametric surface 34 and the thermal choke 54. Consequently, IR radiation incident on the lower surface 64 and/or inner diametric surface 34 of the plasma confinement ring

14 is blocked by the roughened and/or coated upper surface 62, which thereby enhances heating of the portion of the plasma confinement ring 14 between the inner diametric surface 34 and the thermal choke 54. As the surface 64 is not directly exposed to plasma, the IR opaque material can be of a material, such as alumina, that is not preferred for use on plasma-confining surfaces.

[0037] In another preferred embodiment, selected surfaces that define the slots formed in the plasma confinement rings can be roughened and/or coated with a material that is opaque to IR radiation. For example, in the embodiment of the plasma confinement ring 120 shown in FIGs. 2 and 3, at least one of the surfaces 169 and 171 can be roughened and/or coated with an IR opaque material to block transmission of IR radiation to affect further heating of the inner diametric surface 140.

[0038] FIG. 5 depicts an exemplary embodiment of a capacitively-coupled plasma processing chamber 300 in which the plasma confinement ring assembly 10 is mounted. The plasma processing chamber 300 includes an upper electrode 302 having a bottom surface 304. In the embodiment, the bottom surface 304 includes a step 306 adapted to control a localized density of the plasma formed adjacent the exposed surface of the upper electrode 302, as described in U.S. Patent No. 6,391,787, which is incorporated herein by reference in its entirety. In the embodiment, the upper electrode 302 is a showerhead electrode including gas passages 308 arranged for distributing process gas into the plasma processing chamber 300. The upper electrode 302 can be comprised of silicon (e.g., single crystal silicon or polycrystalline silicon) or silicon carbide.

[0039] In the embodiment, the upper electrode 302 is a single-piece electrode (e.g., for 200 mm wafer processing). The upper electrode 302 is preferably mounted (e.g., elastomer bonded) to a backing member 310 of a suitable material, such as graphite or silicon carbide. The backing member includes gas passages 312 in fluid communication with corresponding gas passages 308 in the upper electrode 302.

[0040] In another embodiment, the upper electrode can have a two-piece construction (e.g., for 300 mm wafer processing) and include a single-piece inner electrode member and an outer electrode member surrounding the inner electrode member, such as described in commonly-owned U.S. Patent Application No. 10/743,062, which is incorporated herein by reference in its entirety. In the embodiment, the backing member preferably includes a backing plate co-extensive with the inner electrode member and a backing ring co-extensive with the outer electrode member, as described in U.S. Patent Application No. 10/743,062.

[0041] In the embodiment of the plasma processing chamber 300 shown in FIG. 5, a thermal control plate 314 is preferably provided on the backing member 310. The thermal control plate 314 preferably includes one or more heaters adapted to control the temperature of the upper electrode 302, as described in U.S. Patent Application No. 10/743,062.

[0042] The plasma processing chamber 300 includes a gas source (not shown) for supplying process gas to the upper electrode 302. The process gas is distributed in the chamber by the gas passages 308 in the upper electrode 302. The upper electrode 302 can be powered by an RF power source 316 via a matching network. In another embodiment, the upper electrode 302 can be electrically grounded to provide a return path for power supplied by a bottom electrode of the substrate support 320 of the plasma processing chamber 300.

[0043] In the embodiment, process gas is supplied into the plasma processing chamber 300 at the plasma generation region in the space between the upper electrode 302 and a semiconductor substrate 322, e.g., a semiconductor wafer, supported on a substrate support 320. The substrate support 320 preferably includes an electrostatic chuck 324 that secures the semiconductor substrate 322 on the substrate support by an electrostatic clamping force. The electrostatic chuck 324 acts as a bottom electrode and is preferably biased by at least one of the RF power sources 326, 327 (typically via a matching network).

[0044] During plasma processing of the semiconductor substrate 322, the plasma confinement ring assembly 10 confines plasma in a plasma confinement zone between the upper electrode 302 and the semiconductor substrate 322. Edge rings 326, 328 are preferably arranged in surrounding relationship to the semiconductor substrate 322 to focus the plasma so as to improve etch uniformity.

[0045] A vacuum pump (not shown) is adapted to maintain a desired vacuum pressure inside the plasma processing chamber 300.

[0046] An exemplary parallel-plate plasma reactor that can be used is a dual-frequency plasma etch reactor (see, e.g., commonly-owned U.S. Patent No. 6,090,304, which is hereby incorporated by reference in its entirety). In such reactors, etching gas can be supplied to a showerhead electrode from a gas supply and plasma can be generated in the reactor by supplying RF energy at different frequencies from two RF sources to the showerhead electrode and/or a bottom electrode. Alternatively, the showerhead electrode can be electrically grounded and RF energy at two different frequencies can be supplied to the bottom electrode.

[0047] **Example 1**

[0048] In Example 1, a plasma confinement ring assembly 400 as shown in FIG. 6 was used in a parallel-plate, capacitively-coupled plasma processing chamber. As shown, the plasma confinement ring assembly 400 generally has the same construction as the assembly 10 shown in FIG. 1; however, the plasma confinement rings 414, 416, 418 and 420 do not include thermal chokes. The plasma confinement rings were of quartz.

[0049] In Example 1, the following dielectric etch process conditions were used to process 85 wafers: 45 mT chamber pressure/1100 W power at a frequency of 2 MHz applied to bottom electrode/800 W power at a frequency of 60 MHz applied to bottom electrode/300 sccm argon/15 sccm C₄F₈/10 sccm O₂/upper electrode temperature of 140°C/bottom electrode temperature of 20°C. An oxygen cleaning step was performed after etching each wafer using the following process conditions: 500 mT chamber pressure/200 W power at a frequency of 27 MHz applied to bottom

electrode/300 W power at a frequency of 60 MHz applied to bottom electrode/2000 sccm O₂/40 seconds.

[0050] As shown in FIG. 6, temperatures were measured using thermocouples attached at location A on the bottom surface 452 of the mounting ring 412, location B on the top surface of the confinement ring 414, location C at the top surface of the confinement ring 416, and location D at the top surface of the confinement ring 420.

[0051] The following temperatures were measured at these locations during the plasma processing: location A – about 66°C/location B – about 110°C to about 116°C/location C – about 82°C/location D – about 82°C to about 104°C. Following etching of the wafers, the plasma processing chamber was opened and the confinement ring assembly 400 was visibly examined for the presence of polymer deposition. No polymer deposition was observed on the plasma confinement ring 414. However, polymer deposition was observed on the plasma-exposed, inner diametric surfaces 436, 438 and 440 of the plasma confinement rings 416, 418 and 420, indicating that these surfaces did not reach a sufficiently high temperature to prevent polymer deposition.

[0052] Example 2

[0053] Example 2 used the plasma confinement ring assembly 400 shown in FIG. 6 in a parallel-plate, capacitively-coupled plasma processing chamber to etch 100 wafers using the following dielectric etch process conditions: 45 mT chamber pressure/1100 W power at a frequency of 2 MHz applied to bottom electrode/800 W power at a frequency of 60 MHz applied to bottom electrode/300 sccm argon/28 sccm C₄F₈/13 sccm O₂/upper electrode temperature of 140°C/bottom electrode temperature of 20°C. An oxygen cleaning step was performed after etching each wafer using the following process conditions: 500 mT chamber pressure/250 W power at a frequency of 27 MHz applied to bottom electrode/125 W power at a frequency of 60 MHz applied to bottom electrode/2000 sccm O₂/40 seconds.

[0054] Following etching of the wafers, the plasma processing chamber was opened and the confinement ring assembly 400 was visibly examined for the presence of polymer deposition. No polymer deposition was observed on the plasma confinement ring 414. However, polymer deposition was observed on the plasma-exposed, inner diametric surfaces 436, 438 and 440 of the plasma confinement rings 416, 418 and 420, indicating that these surfaces did not reach a sufficiently high temperature to prevent polymer deposition.

[0055] **Example 3**

10 [0056] In Example 3, a plasma confinement ring assembly 500 as shown in FIG. 7 was used in a parallel-plate, capacitively-coupled plasma processing chamber. As shown, the plasma confinement ring assembly 500 has the same construction as the assembly 10 shown in FIG. 1, and includes thermal chokes 554, 556, 558 and 560 on the respective plasma
15 confinement rings 514, 516, 518 and 520. The thermal chokes 554, 556, 558 and 560 were slots formed in a concentric, discontinuous circular arrangement, such as shown in FIG. 2. The slots had a width of from about 0.010 inch to about 0.015 inch and extended through the thickness of the plasma confinement rings 514, 516, 518 and 520.

20 [0057] In Example 3, the same etch process conditions that were used in Example 2 were used to process 100 wafers.

[0058] As shown in FIG. 7, temperatures were measured using thermocouples attached at location A on the bottom surface 552 of the mounting ring 512; location B on the top surface of the confinement ring 514, inwardly from the thermal choke 554; location C at the top surface of the
25 confinement ring 514, outwardly from the thermal choke 554; location D at the top surface of the confinement ring 516, inwardly of the thermal choke 556; and location E at the top surface of the confinement ring 516, outwardly from the thermal choke 556. The following temperatures were measured at
30 these locations: location A – about 71°C to about 77°C /location B – about 127°C to about 132°C/location C – about 71°C to about 77°C /location D – about 116°C to about 143°C/location E - about 77°C to about 82°C.

[0059] Following etching of the wafers, the plasma processing chamber was opened and the confinement ring assembly 500 was visibly examined for the presence of polymer deposition. No polymer deposition was observed on the plasma confinement ring 514 or on the plasma-exposed, inner diametric surfaces 536, 538 and 540 of the plasma confinement rings 516, 518 and 520, indicating that these surfaces reached a sufficiently high temperature to prevent polymer deposition.

[0060] Referring to FIG. 1, the above-described test results demonstrate that by incorporating the uppermost extended plasma confinement ring 14 in the plasma confinement ring assembly, polymer deposition on the thick mounting ring 12 can preferably be prevented. In addition, by providing one or more thermal chokes in the plasma confinement rings 14, 16, 18 and 20, polymer deposition on plasma exposed surfaces of the rings can preferably be prevented.

[0061] The foregoing has described the principles, preferred embodiments and modes of operation of the present invention. However, the invention should not be construed as being limited to the particular embodiments discussed. Thus, the above-described embodiments should be regarded as illustrative rather than restrictive, and it should be appreciated that variations may be made in those embodiments by workers skilled in the art without departing from the scope of the present invention as defined by the following claims.

WHAT IS CLAIMED IS:

1. A plasma confinement ring assembly for a plasma processing chamber, comprising a plurality of plasma confinement rings each including
5 an inner portion having a plasma-exposed inner diametric surface, an outer portion disposed radially outwardly from the inner portion, and at least one thermal choke adapted to reduce heat conduction from the inner portion to the outer portion when the inner diametric surface is exposed to plasma in the plasma processing chamber, such that the inner diametric surface
10 reaches a sufficiently high temperature to substantially prevent polymer deposition thereon.
2. The plasma confinement ring assembly of Claim 1, wherein one or more of the plasma confinement rings has a one-piece construction.
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3. The plasma confinement ring assembly of Claim 1, wherein one or more of the plasma confinement rings comprises inner and outer portions which are separate pieces.
- 20 4. The plasma confinement ring assembly of Claim 3, wherein the inner portion is an inner ring including the inner diametric surface, the outer portion is an outer ring, and at least one gap is defined between the inner ring and outer ring.
- 25 5. The plasma confinement ring assembly of Claim 3, wherein the inner portion and the outer portion are comprised of the same dielectric material.
- 30 6. The plasma confinement ring assembly of Claim 1, wherein the inner portion of one or more of the plasma confinement rings has at least one surface that is roughened and/or coated with a material that blocks IR radiation.

7. The plasma confinement ring assembly of Claim 1, wherein the thermal choke of at least one of the plasma confinement rings comprises a plurality of slots.

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8. The plasma confinement ring assembly of Claim 7, wherein at least one of the slots is partially defined by a surface that is roughened and/or coated with a material that blocks IR radiation.

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9. The plasma confinement ring assembly of Claim 7, wherein the slots comprise a plurality of first slots which extend around a discontinuous first circle and a plurality of second slots which extend around a concentric discontinuous second circle surrounding the first circle.

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10. The plasma confinement ring assembly of Claim 7, wherein the slots each extend completely through the thickness of the plasma confinement ring.

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11. A plasma processing apparatus, comprising:
an upper electrode;
a substrate support including a lower electrode; and
a plasma confinement ring assembly according to Claim 1 arranged to enhance confinement of a plasma in a space between the upper electrode and the substrate support.

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12. A plasma confinement ring assembly for a plasma processing chamber, comprising:

a mounting ring; and
a plurality of plasma confinement rings suspended below the mounting ring, the plasma confinement rings comprise an upper plasma confinement ring and a plurality of lower plasma confinement rings, the upper plasma confinement ring includes a top surface facing the mounting

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ring and a plasma-exposed bottom surface disposed radially inward from the lower plasma confinement rings, at least a portion of the top surface of the upper plasma confinement ring is adapted to block IR radiation to thereby enhance heating of the upper plasma confinement ring such that the bottom
5 surface reaches a sufficiently high temperature to substantially prevent polymer deposition thereon when the bottom surface is exposed to the plasma.

13. The plasma confinement ring assembly of Claim 12, wherein
10 the top surface of the upper plasma confinement ring is roughened and/or coated with a material that blocks IR radiation.

14. The plasma confinement ring assembly of Claim 12, wherein:
the upper plasma confinement ring comprises an inner portion, an
15 outer portion and at least one thermal choke which reduces heat conduction from the inner portion to the outer portion when the bottom surface is exposed to the plasma; and

the lower plasma confinement rings each comprise an inner portion including a plasma-exposed surface, an outer portion, and at least one
20 thermal choke adapted to reduce heat conduction from the inner portion to the outer portion thereof when the plasma-exposed surface is exposed to the plasma.

15. The plasma confinement ring assembly of Claim 14, wherein
25 the thermal chokes are adapted to cause the bottom surface of the upper plasma confinement ring and the plasma-exposed surface of each of the lower plasma confinement rings to reach a sufficiently high temperature to substantially prevent polymer deposition on the bottom surface and on each of the plasma-exposed surfaces when the bottom surface and the plasma-
30 exposed surfaces are exposed to the plasma.

16. The plasma confinement ring assembly of Claim 14, wherein the thermal chokes each comprise a plurality of slots.

17. The plasma confinement ring assembly of Claim 16, wherein
5 the slots comprise a plurality of first slots which extend around a discontinuous first circle and a plurality of second slots which extend around a concentric discontinuous second circle surrounding the first circle.

18. The plasma confinement ring assembly of Claim 16, wherein
10 the slots each extend completely through the thickness of the upper plasma confinement ring and/or completely through the thickness of the lower plasma confinement rings and the slots have a width of from about 0.005 inch and 0.020 inch.

19. The plasma confinement ring assembly of Claim 16, wherein at
15 least some of the slots are defined in part by a surface that is roughened and/or coated with a material that blocks IR radiation.

20. The plasma confinement ring assembly of Claim 12, wherein
20 the plasma confinement rings each have a one-piece construction.

21. The plasma confinement ring assembly of Claim 12, wherein
the plasma confinement rings each include an inner portion and a separate
outer portion.

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22. The plasma confinement ring assembly of Claim 21, wherein
the inner portion is an inner ring, the outer portion is an outer ring, at least
one gap is defined between the inner ring and the outer ring.

23. The plasma confinement ring assembly of Claim 21, wherein
30 the inner portion and the outer portion are comprised of the same dielectric material.

24. A plasma processing chamber, comprising:
an upper electrode;
a substrate support including a lower electrode; and
5 a plasma confinement ring assembly according to Claim 12
arranged to enhance confinement of a plasma in a space between the upper
electrode and the substrate support.

25. A method of processing a semiconductor substrate in a plasma
10 processing chamber, comprising:
supplying process gas into a plasma processing chamber
comprising a plurality of plasma confinement rings each including a plasma-
exposed surface; and
producing a plasma from the process gas and etching a
15 semiconductor substrate in the plasma processing chamber;
during the etching, the plasma-exposed surface of each of the
plasma confinement rings reaches a sufficiently high temperature to
substantially prevent polymer deposition thereon.

20 26. The method of Claim 25, wherein the semiconductor substrate
comprises a dielectric material which is etched by the plasma, and the
process gas contains at least one constituent selected from the group
consisting of fluorocarbons, hydrofluorocarbons, fluorocarbon precursors
and hydrofluorocarbon precursors.

25 27. The method of Claim 25, wherein the plasma processing
chamber comprises a grounded upper electrode, and a lower electrode to
which power is applied at two different frequencies.

30 28. The method of Claim 27, wherein the upper electrode is a
showerhead electrode.

29. The method of Claim 25, wherein the plasma confinement rings each include at least one thermal choke which reduces heat conduction through the plasma confinement rings when exposed to plasma in the plasma processing chamber, such that plasma exposed surfaces of the plasma confinement rings reach a sufficiently high temperature to substantially prevent polymer deposition thereon.

30. The method of Claim 29, wherein the thermal chokes are slots.

31. The method of Claim 29, wherein one or more of the plasma confinement rings comprises separate pieces defining at least one gap therebetween.

32. The method of Claim 29, wherein one or more of the plasma confinement rings has at least one surface that is roughened and/or coated with a material that blocks IR radiation.