~~What is claimed is:~~

CLAIMS

1. A method for fabricating a semiconductor device comprising:

forming a gate stack comprising a gate dielectric and gate electrode over a substrate;

forming stressor regions within the substrate on opposed sides of the gate stack, the stressor regions comprising stressor material incorporated into substitutional sites of the substrate;

forming a first stressor layer over the substrate after forming the stressor regions, the first stressor layer having a first stress value; and

annealing to memorize at least a portion of the first stress value in the semiconductor device, wherein the anneal is conducted at a low temperature.

2. The method of claim 1, wherein the annealing step to memorize at least a portion of the first stress value is conducted at a temperature of 700°C or less.

3. The method of claim 1, wherein the annealing step to memorize at least a portion of the first stress value comprises annealing at a temperature of approximately between 600 to 700 °C.

4. The method of claim 1, wherein the annealing step to memorize at least a portion of the first stress value comprises annealing in a furnace environment.

5. The method of claim 1, further comprising removing the first stressor layer after the annealing to memorize at least a portion of the first stress value.

6. The method of claim 1, further comprising:

forming first diffusion regions within the substrate on opposed sides of the gate stack; and

annealing the substrate with a laser anneal to activate dopants in the first diffusion regions.

7. The method of claim 6, comprising forming the stressor regions before forming the first diffusion regions and performing the activation laser anneal.

8. The method of claim 6, wherein the activation laser anneal step comprises performing a laser anneal for a time duration of 1 millisecond or less.

9. The method of claim 6, wherein the first diffusion regions are source/drain regions and the semiconductor device is a MOS transistor.

10. The method of claim 6, forming the first stressor layer after forming the first diffusion regions.

11. The method of claim 1, wherein forming the stressor regions comprises

implanting at least one stressor material into the substrate; and

annealing the substrate to incorporate the stressor material into substitutional sites of the substrate.

12. The method of claim 11, comprising incorporating the stressor material using laser annealing.

13. The method of claim 1, wherein the stressor material comprises carbon.

14. A method for fabricating a semiconductor device comprising:

forming a gate stack comprising a gate dielectric and gate electrode over a substrate;

forming stressor regions within the substrate on opposed sides of the gate stack, the stressor regions comprising implanted stressor material incorporated into substitutional sites of the substrate;

forming a first stressor layer over the substrate after forming the stressor regions, the first stressor layer having a first stress value;

annealing to memorize at least a portion of the first stress value in the semiconductor device, wherein the anneal is conducted at a temperature of 700°C or less;

forming first diffusion regions within the substrate on opposed sides of the gate stack; and

annealing the substrate with a laser anneal at a temperature to activate dopants in the first diffusion regions.

15. The method of claim 14 wherein the stressor regions are formed before forming the first diffusion regions.

16. The method of claim 14 wherein the first diffusion regions are source/drain regions and the semiconductor device is a MOS transistor.

17. The method of claim 14 wherein the atomic concentration of stressor material incorporated into substitutional sites is at least 1% post memorization anneal and activation anneal.

18. A method for fabricating a semiconductor device comprising:

forming a gate stack comprising a gate dielectric and gate electrode over a substrate;

forming a stressor regions within the substrate on opposed sides of the gate stack, the stressor regions comprising stressor material incorporated into substitutional sites of the substrate;

forming first spacers adjacent opposed sidewalls of the gate stack after forming the stressor regions; and

forming first diffusion regions on opposed sides of the gate stack within the substrate wherein the stressor regions are located closer to an edge of the gate stack compared to the first diffusion region.

19. A semiconductor device comprising:

a gate stack comprising a gate dielectric and gate electrode over a substrate;

a stressor region within the substrate on opposed sides of the gate stack, the stressor region comprising stressor material incorporated in substitutional sites of the substrate; and

first diffusion regions within the substrate on opposed sides of the gate stack, wherein the stressor regions are located closer to an edge of the gate stack compared to the first diffusion regions.

20. A semiconductor device comprising:

a gate stack comprising a gate dielectric and gate electrode over a substrate;

a stressor region within the substrate on opposed sides of the gate stack, the stressor region comprising stressor material incorporated in substitutional sites of the substrate; and

a first stressor layer having a first stress value comprising lateral portions adjacent to a surface of the substrate wherein the stressor regions are located closer to an edge of the gate stack compared to the lateral portions of the first stressor layer.

What is claimed is:

CLAIMS

1. A method for fabricating a semiconductor device comprising:

providing a substrate prepared with isolation regions;

forming a gate stack having first and second sidewalls over a substrate;

forming stressor diffusion extension regions within the substrate on opposed sides of the gate stack, wherein the stressor diffusion extension regions comprise a first concentration of stressor atoms incorporated into substitutional sites of diffusion extension regions;

forming source/drain (S/D) stressor diffusion regions on opposed sides of the gate stack within the substrate, wherein the S/D stressor diffusion regions comprise a depth which is deeper than the diffusion extension regions and comprise the first concentration of stressor atoms incorporated into substitutional sites of S/D diffusion regions;

forming a first stressor layer over the substrate after forming the stressor diffusion extension regions, the first stressor layer having a first stress value;

performing a first anneal to memorize at least a portion of the first stress value in the semiconductor device, wherein the first anneal is conducted at a low temperature; and

performing a second anneal with a laser based anneal to activate dopants in the S/D diffusion regions after the first anneal, wherein the first and second anneal prevent displacement of the stressor atoms having the first concentration from the substitutional sites and which are distributed throughout a width of diffusion extension and diffusion regions which extends from a sidewall of the gate to the isolation region.

2. The method of claim 1, wherein the first anneal to memorize at least a portion of the first stress value is conducted at a temperature of 700°C or less.

3. The method of claim 1, wherein the first anneal to memorize at least a portion of the first stress value comprises annealing in a furnace environment.

4. The method of claim 1, further comprising removing the first stressor layer after the first anneal to memorize at least a portion of the first stress value.

5. The method of claim 1 wherein forming the stressor diffusion extension regions comprises performing a laser anneal to incorporate the stressor atoms into the substitutional sites and to convert the stressor diffusion extension regions into crystalline stressor regions.

6. The method of claim 1, wherein the second anneal comprises performing a laser spike anneal.

7. The method of claim 1, wherein the diffusion extension regions are source/drain extension regions and the semiconductor device is a MOS transistor.

8. The method of claim 1, wherein the stressor atoms comprise carbon.

9. A method for fabricating a semiconductor device comprising:

providing a substrate prepared with isolation regions;

forming a gate stack having first and second sidewalls over a substrate;

forming stressor diffusion extension regions within the substrate on opposed sides of the gate stack, wherein the stressor diffusion extension regions are formed by implanting a first concentration of stressor atoms which are incorporated into substitutional sites of diffusion extension regions and distributed throughout a width of the diffusion extension regions; and

forming stressor diffusion regions by implanting the first concentration of stressor atoms which are incorporated into substitutional sites of diffusion regions and distributed throughout a width of the diffusion regions on opposed sides of the gate stack within the substrate, wherein the stressor diffusion regions comprise a depth which is deeper than a depth of the diffusion extension regions, and the stressor diffusion extension regions are located closer to an edge of the gate stack compared to the stressor diffusion regions, and wherein the first concentration of the stressor atoms are distributed throughout the width of diffusion extension and diffusion regions which extends from a sidewall of the gate to the isolation region.

10. A semiconductor device comprising:

a substrate having isolation regions;

a gate stack having first and second sidewalls disposed over a substrate;

stressor diffusion extension regions within the substrate on opposed sides of the gate stack, wherein the stressor diffusion extension regions comprise a first concentration of stressor atoms incorporated in substitutional sites of diffusion extension regions and which are distributed throughout a width of the diffusion extension regions; and

stressor diffusion regions having the first concentration of stressor

atoms which are incorporated into substitutional sites of diffusion regions and distributed throughout a width of the diffusion regions within the substrate on opposed sides of the gate stack, wherein the stressor diffusion regions comprise a depth which is deeper than a depth of the diffusion extension regions, and wherein the stressor diffusion extension regions are located closer to an edge of the gate stack compared to the stressor diffusion regions, and wherein the first concentration of the stressor atoms are distributed throughout a width of diffusion extension and diffusion regions which extends from a sidewall of the gate to the isolation region.

11. The method of claim 9, wherein forming the stressor diffusion extension regions comprises:

introducing first type dopants to form the diffusion extension regions; and

introducing the stressor atoms, wherein the stressor atoms are confined within the diffusion extension regions.

12. The method of claim 11, wherein introducing the stressor atoms is performed after introducing the first type dopants.

13. The method of claim 11, wherein:

introducing the stressor atoms comprises implanting the stressor atoms into the substrate; and comprises

annealing the substrate to incorporate the stressor atoms into the substitutional sites of the substrate.

14. The method of claim 13, wherein the implant of the stressor atoms is tuned such that the stressor atoms are substantially confined within an upper portion of the diffusion extension regions.

15. The method of claim 13, wherein the stressor atoms are incorporated into the substitutional sites of the substrate using laser annealing.

16. The method of claim 11, comprising:

forming first spacers along sidewalls of the gate stack, wherein the first spacers act as a mask during introduction of the first type dopants and stressor atoms such that edges of the stressor diffusion extension regions are aligned with outer edges of the first spacers.

17. The method of claim 16, wherein forming the stressor diffusion regions comprises:

forming second spacers along sidewalls of the first spacers;

introducing first type dopants to form the diffusion regions; and

introducing stressor atoms, wherein the stressor atoms are confined within the diffusion regions to form the stressor diffusion regions.

18. The method of claim 1 comprising:

forming first spacers along sidewalls of the gate stack, wherein the first spacers act as a mask during the formation of the stressor diffusion extension regions such that edges of the stressor diffusion extension regions are aligned with outer edges of the first spacers.

19. The method of claim 1 wherein the diffusion extension regions are source/drain extension regions and the semiconductor device is a MOS transistor.

20. The method of claim 1 wherein the atomic concentration of stressor atoms incorporated into the substitutional sites is at least 1% post first and second anneal.

21. A method for fabricating a semiconductor device comprising:

providing a substrate prepared with isolation regions;

forming a gate stack having first and second sidewalls over a substrate;

forming stressor diffusion extension regions within the substrate on opposed sides of the gate stack, wherein the stressor diffusion extension regions comprise stressor atoms incorporated into substitutional sites of diffusion extension regions;

forming source/drain (S/D) diffusion regions, wherein the S/D diffusion regions comprise a depth which is deeper than the diffusion extension regions;

forming a first stressor layer over the substrate after forming the stressor diffusion extension regions, the first stressor layer having a first stress value;

performing a first anneal to memorize at least a portion of the first stress value in the semiconductor device, wherein the first anneal is conducted at a low temperature; and

performing a second anneal with a laser based anneal to activate dopants in the S/D diffusion regions after the first anneal, wherein the first and second anneal prevent displacement of the stressor atoms from the substitutional sites and which are distributed throughout a width of diffusion extension regions which extends from a sidewall of the gate to the isolation region.