A Method To Fabricate Variable Work Function Gates For FUSI Devices

Abstract

An embodiment for forming variable work function gates in a FUSI device is described. The embodiment uses a work function doping implant to dope the polysilicon to achieve a desired work function. Selective epitaxy growth (SEG) preferably is used to form silicon over the source/drain regions. The doped poly-Si gate is fully silicided to form fully silicided gates that have a desired work function. We form a gate dielectric layer and a gate layer over the substrate. We implant impurities into the gate layer gate in the NMOS gate regions and the PMOS gate regions. We pattern the cap layer, the gate layer and the gate dielectric layer to form a NMOS gate and a PMOS gate. We form fully silicided NMOS gate and fully silicided PMOS gate.

FIGURE 8