Description

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a MOSFET transistor, comprising

- a semiconductor substrate having a first conductivity type;
- source and drain regions formed at a certain distance away from each other in a surface area of the substrate; and
- a gate electrode formed on a surface of the substrate through a gate insulating film formed thereon between the source and drain regions,
- a channel region located in the surface area of the substrate between the source and drain regions being composed of different concentration regions, and a threshold voltage of a high concentration channel region being lower than that of a low concentration channel region.

Description of the Background Art

A MOSFET transistor of this kind is known from DE-A-2 903 534.

In Fig. 1, there is shown a conventional N-channel MOS transistor which comprises a P-type semiconductor substrate 1, an N-type polycrystalline silicon gate electrode 3 formed on the surface of the substrate 1 via a gate insulating oxide film 5, and a drain 7 and a source 9 formed in the surface area of the substrate 1 in the right and left sides of the gate electrode 3.

In this case, in order to determine a threshold voltage to a relatively large value such as approximately 0.6 to 0.8 V, it is necessary to fairly raise the concentration of the P-type impurity in the substrate 1. That is, when polycrystalline silicon implanted with an N-type impurity is used for the gate electrode 3, since the work function difference between the substrate 1 and the gate electrode 3 become large, the impurity concentration in the substrate 1 is necessarily increased so as not to form an inversion layer in a channel region 11 in the surface area of the substrate 1 between the drain and source regions 7 and 9.

On the other hand, when the gate oxide film 3 is thinned as the device is miniaturized, the impurity concentration in the substrate 1 must be increased in order to obtain a large threshold voltage. That is, even when the device is miniaturized, the reduction of the threshold voltage causes the increase of the leakage current, and hence the threshold voltage cannot be reduced largely. Accordingly, as the device is miniaturized, the impurity concentration in the substrate is increased.

As described above, the impurity concentration increase in the substrate invites the fall-off of the carrier mobility. That is, when the impurity concentration in the substrate is increased, the electric field in the direction perpendicular to the substrate increases to cause the carrier dispersion in the surface area and the impurity dispersion due to the impurity concentration increase which affect the fall-off of the carrier mobility. Further, the impurity concentration increase in the substrate brings about the increase of the variation rate of the threshold voltage increase (back bias effect) while a reverse bias is applied between the source and substrate, thereby lowering the characteristics of the device. Further, it becomes difficult to operate the device in high speed, and the current driving ability thereof is reduced.

Meanwhile, when the gate electrode 3 is made of a metal having a high melting point, a silicide thereof or an undoped polycrystalline silicon, the work function difference between the substrate 1 and the gate electrode 3 becomes small, thereby enabling the reduction of the impurity concentration in the substrate even when the large threshold voltage is obtained.

However, in such a case, the depletion layer is liable to extend from both the drain and source regions 7 and 9 toward the channel region 11. Hence, when the depletion layers extending from the drain and source regions 7 and 9 are contacted with each other, a short-circuit is caused between them to cause the punch-through phenomenon. Also, even when such depletion layers do not contact with each other, the depletion layers extending in the channel region 11 bring about the short channel effect.

In order to prevent or minimize such punch-through phenomenon and short channel effect, p pocket regions are provided in the surface area of the substrate between the ends of the gate electrode and the drain and source regions, as diclosed in the documents "IEDM (" Tech Digest (1982), pp 718-721, Seiki Ogura et al.".

In Fig. 2, there is shown a conventional N-channel MOS transistor having p pocket regions 13 in the surface are of the substrate 1 between the ends of the gate electrode 3 and the drain and source regions 7 and 9. The p pocket regions 13 implanted with an N-type high concentration impurity are formed in a deep position under silicon oxide (SiO_2) side walls 15 on the gate electrode 3 between the drain and source regions 7 and 9 by using a technique for providing such side walls 15. The p pocket regions 13 function so as to restrain the extension of the depletion layers from the drain and source regions 7 and 9, thereby preventing the punch-through.

In such a case, since the p pocket regions 13 are formed of a p-type high concentration region and become highly resistant, when the p pocket regions 13 are formed right under the side walls 15, the driving force of the device is reduced, and a high electric field is produced in the channel region 11 to generate hot

electrons.

Therefore, the p pocket regions 13 should be formed in a deep position below the surface area of the channel region 11.

As described above, in any of the conventional MOS transistors, it is quite difficult to effectively improve the high speed operation of the device and the current driving ability and to effectively prevent the punch-through phenomenon and the short channel effect.

From PATENT ABSTRACTS OF JAPAN, vol 10, No. 213, and JP-A 61 53 773 a semiconductor device is known, providing a low concentration region of a second conductivity type between a low concentration region of a first conductivity type and a region of the second conductivity type under a gate electrode.

From PATENT ABSTRACTS OF JAPAN, vol. 9, No. 169 and JP-A-60 43 863 a semiconductor device is known having a gate electrode 26 of a poycrystalline silicon film containing a p type impurity and a non-doped second gate electrode provided only at the side wall of the gate electrode.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a MOSFET transistor, free from the aforementioned defects and disadvantages of the prior art, which is capable of performing a high speed operation of the transistor and a high current driving ability without causing a punch-through penomenon and a short channel effect.

In accordance with the present invention, there is provided a MOSFET transistor, comprising a semiconductor substrate having a first conductivity type, source and drain regions, formed at a certain distance away from each other in a surface area of the substrate, and a gate electrode formed on a surface of the substrate through a gate insulating film formed thereon between the source and drain regions, a channel region located in the surface area of the substrate between the source and drain regions being composed of different concentration regions, and a threshold voltage of a high concentration channel region being lower than that of a loow concentration channel region, characterized in that

- the gate electrode is composed of a central gate member formed in a central portion of the gate electrode and side gate members formed in both side end portions of the gate electrode,
- the central gate member locating above the low concentration channel region and the side gate members locating above the high concentration channel region adjacent to the source and drain regions,
- the central gate member comprising one of an undoped semiconductor film, a metal and a metallic silicide,
- the side gate members comprising a semiconductor film having a second conductivity type different from the first conductivity type.

BRIEF DESCRIPTION OF THE DRAWINGS.

The above and other objects, features and advantages of the present invention will more fully appear from the following description of the preferred embodiments with reference to the accompanying drawings, in which:

Fig. 1 is a longitudinal cross section of a convention MOSFET transistor;

Fig. 2 is a longitudinal cross section of another conventional MOSFET transistor having p packet regions;

Fig. 3 is a longitudinal cross section of a first embodiment of a MOSFET transistor according to the present invention;

Figs. 4a and 4d show a method for producing the MOSFET transistor shown in fig. 3;

Fig. 5 is a longitudinal cross section of a second embodiment of a MOSFET transistor according to the present invention;

Figs. 6a and 6d show a method for producing the MOSFET transistor shown in Fig. 5; and

Fig. 7 is a graphical representation showing characteristics of the transistor shown in Figs. 3 and 5.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings, wherein like reference characters designate like or corresponding components throughout the several views and thus the repeated description thereof may be omitted for the brevity, there is shown in Fig. 3 the first embodiment of an N-channel MOSFET transistor according to the present invention.

In the drawing, the N-channel MOSFET transistor is formed on a P-type single crystal silicon semiconductor substrate 21, i.e., a gate electrode 3 is formed on the surface of the substrate 21 via a gate insulating oxide film 25 between a drain 27 and a source 29 formed in the surface area of the substrate 21 in the right and left sides of the gate electrode 3.

The gate electrode 3 is integrally composed of a central gate member 23a of undoped polycrystalline silicon and a pair of side gate members 23b of N-type polycrystalline silicon doped with an N-type impurity such as As, and the central gate member 23a is arranged between the side gate members 23b.

A pair of P-type impurity regions 31 having a higher impurity concentration than that of the substrate 21 is formed to extend in the lower portions right under the drain and source regions 27 and 29 and the side portions on the drain and source regions

27 and 29 and under the side gate members 23b of the gate electrode 23. A field oxide film 37 as a device separation region covers the surface of the substrate 21 to separate the devices from one another. A silicon oxide (SiO_2) surface protecting film 33 as a passivation film is formed to cover the gate electrode 23 and the entire surface of the device. Aluminum wires 35 are connected to the drain and source regions 27 and 29 through the surface protecting film 33 and the gate insulating film 25.

A method for producing the MOSFET transistor described above will now be described in detail in connection with Figs. 4a to 4d.

In Fig. 4a, on a P-type single crystal silicon semiconductor substrate 21 having an impurity concentration of approximately $3x10^{16}cm^{-3}$ a field oxide film 37 of silicon nitride having a thickness of approximately 600 nm (6000 Å) for constituting a device separation region is formed so as to surround a transistor formation region. A gate insulating oxide film 25 having a thickness of approximately 10 nm (100 Å) is formed over the surface of the substrate 21 surrounded by the field oxide film 37, and then an undoped polycrystalline silicon film (not shown) having a thickness of approximately 200 nm (2000 Å) is deposited on the entire surface of the gate oxide film 25 by using the CVD (chemical vapor deposition) method. A photoresist material is applied on the undoped polycrystalline silicon film, and a patterning of the photoresist materials is carried out to obtain a photoresist masking pattern 41 on the undoped polycrystalline silicon film. Then, by using the photoresist masking pattern 41 an etching process of the undoped polycrystalline silicon film is performed by the RIE (reactive ion etching) method to obtain an undoped polycrystalline silicon gate electrode 23 on the gate oxide film 25.

In Fig. 4b, the photoresist masking pattern 41 is partially etched by the oxygen plasma treatment to expose both sides of the gate electrode 23. By using a partially etched photoresist masking pattern 43, As ions are implanted into the surface of the substrate 21 including the gate electrode 23 under the condition such as at acceleration energy of approximately 20 keV with a dose of approximately $5x10^{15}cm^{-2}$ to obtain side gate members 23b of an N-type polycrystalline silicon in the gate electrode 23 and also drain and source regions 27 and 29 of an N-type diffusion region in the surface area of the substrate 21 in the left and right sides of the gate electrode 3 at the same time.

In Fig. 4c, by using the masking pattern 43, B ions are implanted into the surface of the substrate 21 including the gate electrode 23 under the relatively high energy condition such as at acceleration energy of approximately 100 keV with dose of approximately $1x10^{12}cm^{-2}$, and then, after removing the masking pattern 43, the obtained substrate 21 with the gate electrode 23 is annealed at approximately 600 °C in a lamp annealing treatment. In this case, since the B ions are implanted at the relative high energy, the shooting range of the B ions is relatively deep such as approximately 300 nm (3000 Å) in depth, and hence P-type impurity regions 31 having a higher impurity concentration than that of the substrate 21 are formed under the side gate members 23b in a channel region in the surface of the substrate 21 between the drain and source regions 27 and 29, and also right under the drain and source regions 27 and 29.

In Fig. 4d, a silicon oxide (SiO_2) surface protecting film 33 as a passivation film is formed over the entire surface of the obtained substrate 21 with the gate electrode 23 thereon. Then, holes for wiring are opened in the surface protecting film 33 and the gate oxide film 25 by an etching or an appropriate manner so as to reach the drain and source regions 27 and 29, and aluminum wires 35 are formed in the holes to contact with the drain and source regions 27 and 28, thereby obtaining the N-channel MOSFET transistor shown in Fig. 3.

In Fig. 5, there is shown the second embodiment of an N-channel MOSFET transistor according to the present invention, having the same construction as that of the first embodiment shown in Fig. 3, except that a central gate member 59a of a gate electrode 59 is composed of molybdenum silicide. That is, a gate electrode 59 is composed of the central gate member 59a of molybdenum silicide and a pair of side gate members 59b of N-type polycrystalline silicon doped with an N-type impurity such as As, and the central gate member 59a is arranged between the side gate members 59b.

A method for producing the MOSFET transistor shown in Fig. 5 will now be described in detail in connection with Figs. 6a to 6d.

In Fig. 6a, a field oxide film 53 is formed on a P-type single crystal silicon semiconductor substrate 51, and a gate insulating oxide film 51 is formed over the surface of the substrate 51 in the same manner as the first embodiment described above. Then, a molybdenum silicide film (not shown) having a thickness of approximately 500 nm (5000 Å) and another silicon oxide film (not shown) are consecutively deposited on the entire surface of the gate oxide film 51. Then, by using a photoresist masking pattern (not shown) the silicon oxide film and the molybdenum silicide film are successively etched by the RIE method to obtain a molybdenum silicide central gate member 59a of a gate electrode 59 with a silicon oxide film 57 formed thereon. Then, by using the central gate member 59a with the silicon oxide film 57 formed thereon as a masking pattern, B ions are implanted into the surface of the substrate 21 under the energy condition such as at acceleration energy of approximately 80 keV with a dose of approximately $8x10^{11}cm^{-2}$ and are also implanted into the surface of the substrate 21 under the energy condition such as at acceleration

energy of approximately 30 keV with a dose of approximately $8x10^{11}cm^{-2}$, and then the obtained substrate 51 with the central gate member 59a is annealed at approximately 600 °C in a lump annealing treatment to obtain P-type impurity regions 61 having a higher impurity concentration than that of the substrate 51 in the surface area of the substrate 51 in the right and left sides of the central gate member 59a.

In Fig. 6b, an N-type polycrystalline silicon film (not shown) doped with an N-type impurity such as As is deposited on the entire surface of the substrate 51 and the central gate member 59a, and then the deposited N-type polycrystalline silicon film is partially etched back by the RIE method to obtain the N-type polycrystalline silicon side gate members 59b on the gate oxide film 55 in contact with both the sides of the central gate member 59a.

In Fig. 6c, by using the gate electrode 59 composed of the central gate member 59a and the side gate members 59b as a mask, As ions are implanted into the surface of the substrate 51 under the condition such as at acceleration energy of approximately 30 keV with a dose of approximately $5x10^{15}cm^{-2}$, and then the lump annealing treatment is carried out to obtain drain and source regions 63 and 65 of an N-type diffusion region in the surface areas of the left and right P-type impurity regions 61.

In Fig. 6d, a silicon oxide (SiO_2) surface protecting film 67 and aluminum wires 69 are formed in the same manner as the first embodiment described above, thereby obtaining the N-channel MOSFET transistor shown in Fig. 5.

In Fig. 7, there are shown curves for representing the relation between the threshold voltage and the impurity concentration of the channel region of the two preferred embodiments described above in the transistor according to the present invention. It is readily understood from Fig. 7 that the threshold voltage is changed by a certain amount corresponding to the work function difference depending on the fact whether or not the gate electrode contains the impurity. That is, the threshold voltage of the gate electrode containing the impurity is restricted to a fairly low value as compared with that of the containing no impurity.

In the preferred embodiments described above, the threshold voltages in the regions under the undoped polycrystalline silicon central gate member 23a or the molybdenum silicide central gate member 59a and under the N-type polycrystalline silicon side gate members 23b or 59b were approximately 0.7 V and 0.4 V, respectively. Hence, in the channel region in the surface area of the substrate between the drain and source regions, the side regions adjacent to the drain and source regions under the side gate members have a high impurity concentration than that of the substrate and a lower threshold voltage than that of the central region under the central gate member.

In the transistor according to the present invention, relating to the current driving ability, it is approximately equal to that of the conventional one shown in Fig. 2, and is approximately 20% higher than that of the conventional one shown in Fig. 1. It is considered that the increase of the current driving ability in the transistor of the present invention is obtained by the carrier mobility increase caused by the decrease of the electric field in the direction perpendicular to the substrate due to the drop of the impurity concentration in the substrate. Therefore, when the impurity concentration in the substrate must be increased as the miniaturization of the device is advanced, since the carrier mobility variation by the Coulomb scattering is to be added, the current driving ability difference will become more remarkable.

On the other hand, in the transistor according to the present invention, the short channel effect is improved as compared with the conventional one including the molybdenum silicide gate electrode, as shown in Fig. 2. The conventional transistor shown in Fig. 2 can normally operate until the channel length is up to 0.7μm, but the present transistors can normally operate until the channel length is up to 0.5μm. This means that, even when the miniaturization of the device is advanced, the punch-through phenomenon can be effectively reduced by increasing the impurity concentration in the P-type impurity regions 31 or 61 in the preferred embodiments shown in Figs. 3 and 5.

In the transistor of the present invention, the N-type polycrystalline silicon side gate members can be formed in a self-aligned manner with respect to the undoped polycrystalline silicon central gate member, and hence superior controllability and reproducibility of such a gate electrode structure can be obtained, with the result of the above described effects and advantages.

Further, the transistor of the present invention can be fabricated without increasing the number of the steps, as shown in Figs. 4 and 6, and the cost increase for fabricating such a transistor can be prevented.

Also, the present invention can be applied to a P-channel MOSFET transistor by reversing the polarity of the impurity to be doped into the substrate, the drain and source regions and the polycrystalline silicon and the polarity of the impurity regions formed in the channel region.

Although the central gate member is formed by the undoped polycrystalline silicon or the molybdenum silicide in the preferred embodiments, a material having a work function between N-type and P-type polycrystalline siliconscan be properly used with the same effects.

In the transistor shown in Fig. 4, in order to reduce the junction resistance between the undoped polycrystalline silicon central gate member 23a and the N-type polycrystalline silicon side gate members 23b

and a contact resistance between these gate members and a gate wiring, a silicide having a high melting point may be attached on the gate electrode. In such a case where another material is present on a gate electrode, since the work function of the gate electrode can be determined by a material in the gate oxide film side, the same effects and advantages as those described above can be obtained.

As described above, according to the present invention, the channel region is composed of the different impurity concentration regions, and the threshold voltage of the high impurity concentration region in the channel region is lower than that of the low impurity concentration region. Accordingly, the extension of the depletion layer can be effectively controlled by the high concentration region in the channel region, and the resistance in the high concentration region can be reduced. Further, by the low concentration region in the channel region, the drop of the carrier mobility and the increase of the back bias effect can be prevented, thereby preventing the cause of the punch-through phenomenon and the short channel effect. Therefore, according to the present invention, MOSFET transistors having quick operativity and high current driving ability can be obtained.

Claims

1. A MOSFET transistor, comprising:
   - a semiconductor substrate (21, 51) having a first conductivity type;
   - source and drain regions (27, 29, 63, 65) formed at a certain distance away from each other in a surface area of the substrate (21, 25); and
   - a gate electrode (23, 59a, 59b) formed on a surface of the substrate (21, 51) through a gate insulating film (25, 55) formed thereon between the source and drain regions (27, 29, 63, 65),
   - a channel region located in the surface area of the substrate between the source and drain regions being composed of different concentration regions, and a threshold voltage of a high concentration channel region (31, 61) being lower than that of a low concentration channel region;

   characterized in that
   - the gate electrode (23, 59a, 59b) is composed of a central gate member (23a, 59a) formed in a central portion of the gate electrode and side gate members (23b, 59b) formed in both side end portions of the gate electrode,
   - the central gate member (23a, 59a) locating above the low concentration channel region and the side gate members (23b, 59b) locating above the high concentration channel region (31, 61) adjacent to the source and drain regions,
   - the central gate member (23a, 59a) comprising one of an undoped semiconductor film, a metal and a metallic silicide,
   - the side gate members (23b, 59b) comprising a semiconductor film having a second conductivity type different from the first conductivity type.

2. The transistor of claim 1, wherein the high concentration channel regions (61, 31) extend in parts of the channel region, adjacent to the source and drain regions (27, 29, 63, 65) and right under the source and drain regions (27, 29, 63, 65).

Patentansprüche

1. MOSFET-Transistor mit
   - einem Halbleitersubstrat (21, 51) mit einem ersten Leitfähigkeitstyp;
   - Source- und Draingebieten (27, 29, 63, 65), die in einer bestimmten Entfernung voneinander beabstandet in einem Oberflächengebiet des Substrats (21, 25) gebildet sind; und
   - einer auf einer Oberfläche des Substrats (21, 51) durch einen darauf gebildeten Gateisolierfilm (25, 55) zwischen den Source- und Draingebieten (27, 29, 63, 65) gebildeten Gateelektrode (23, 59a, 59b);
   - einem in dem Oberflächengebiet des Substrats zwischen den Source- und Draingebieten angeordneten Kanalgebiet, welches aus Gebieten verschiedener Konzentration besteht, wobei eine Schwellenspannung eines Kanalgebietes (31, 61) hoher Konzentration niedriger ist als die eines Kanalgebietes niedriger Konzentration;

   dadurch **gekennzeichnet**, daß
   - die Gateelektrode (23, 59a, 59b) aus einem zentralen Gateteil (23a, 59a) besteht, das in einem zentralen Abschnitt der Gateelektrode gebildet ist, sowie Seitengateteilen (23b, 59b), die in beiden Seitenendabschnitten der Gateelektrode gebildet sind,
   - das zentrale Gateteil (23a, 59a) sich oberhalb des Kanalgebietes niedriger Konzentration befindet, und die Seitengateteile (23b, 59b) sich oberhalb des Kanalgebietes (31, 61) mit hoher Konzentration den Source- und Draingebieten benachbart befinden,
   - das zentrale Gateteil (23a, 59a) einen un-

and a contact resistance between these gate members and a gate wiring, a silicide having a high melting point may be attached on the gate electrode. In such a case where another material is present on a gate electrode, since the work function of the gate electrode can be determined by a material in the gate oxide film side, the same effects and advantages as those described above can be obtained.

As described above, according to the present invention, the channel region is composed of the different impurity concentration regions, and the threshold voltage of the high impurity concentration region in the channel region is lower than that of the low impurity concentration region. Accordingly, the extension of the depletion layer can be effectively controlled by the high concentration region in the channel region, and the resistance in the high concentration region can be reduced. Further, by the low concentration region in the channel region, the drop of the carrier mobility and the increase of the back bias effect can be prevented, thereby preventing the cause of the punch-through phenomenon and the short channel effect. Therefore, according to the present invention, MOSFET transistors having quick operativity and high current driving ability can be obtained.

Claims

1. A MOSFET transistor, comprising:
   - a semiconductor substrate (21, 51) having a first conductivity type;
   - source and drain regions (27, 29, 63, 65) formed at a certain distance away from each other in a surface area of the substrate (21, 25); and
   - a gate electrode (23, 59a, 59b) formed on a surface of the substrate (21, 51) through a gate insulating film (25, 55) formed thereon between the source and drain regions (27, 29, 63, 65),
   - a channel region located in the surface area of the substrate between the source and drain regions being composed of different concentration regions, and a threshold voltage of a high concentration channel region (31, 61) being lower than that of a low concentration channel region;

   characterized in that
   - the gate electrode (23, 59a, 59b) is composed of a central gate member (23a, 59a) formed in a central portion of the gate electrode and side gate members (23b, 59b) formed in both side end portions of the gate electrode,
   - the central gate member (23a, 59a) locating above the low concentration channel region and the side gate members (23b, 59b) locating above the high concentration channel region (31, 61) adjacent to the source and drain regions,
   - the central gate member (23a, 59a) comprising one of an undoped semiconductor film, a metal and a metallic silicide,
   - the side gate members (23b, 59b) comprising a semiconductor film having a second conductivity type different from the first conductivity type.

2. The transistor of claim 1, wherein the high concentration channel regions (61, 31) extend in parts of the channel region, adjacent to the source and drain regions (27, 29, 63, 65) and right under the source and drain regions (27, 29, 63, 65).

Patentansprüche

1. MOSFET-Transistor mit
   - einem Halbleitersubstrat (21, 51) mit einem ersten Leitfähigkeitstyp;
   - Source- und Draingebieten (27, 29, 63, 65), die in einer bestimmten Entfernung voneinander beabstandet in einem Oberflächengebiet des Substrats (21, 25) gebildet sind; und
   - einer auf einer Oberfläche des Substrats (21, 51) durch einen darauf gebildeten Gateisolierfilm (25, 55) zwischen den Source- und Draingebieten (27, 29, 63, 65) gebildeten Gateelektrode (23, 59a, 59b);
   - einem in dem Oberflächengebiet des Substrats zwischen den Source- und Draingebieten angeordneten Kanalgebiet, welches aus Gebieten verschiedener Konzentration besteht, wobei eine Schwellenspannung eines Kanalgebietes (31, 61) hoher Konzentration niedriger ist als die eines Kanalgebietes niedriger Konzentration;

   dadurch **gekennzeichnet**, daß
   - die Gateelektrode (23, 59a, 59b) aus einem zentralen Gateteil (23a, 59a) besteht, das in einem zentralen Abschnitt der Gateelektrode gebildet ist, sowie Seitengateteilen (23b, 59b), die in beiden Seitenendabschnitten der Gateelektrode gebildet sind,
   - das zentrale Gateteil (23a, 59a) sich oberhalb des Kanalgebietes niedriger Konzentration befindet, und die Seitengateteile (23b, 59b) sich oberhalb des Kanalgebietes (31, 61) mit hoher Konzentration den Source- und Draingebieten benachbart befinden,
   - das zentrale Gateteil (23a, 59a) einen un-

* C L M S *

dotierten Halbleiterfilm, ein Metall oder ein metallisches Silizid umfaßt,

- wobei die Seitengateteile (23b, 59b) einen Halbleiterfilm mit einem zweiten, von dem ersten Leitfähigkeitstyp verschiedenen Leitfähigkeitstyp umfassen.

2. Transistor nach Anspruch 1, dadurch gekennzeichnet, daß sich die Kanalgebiete (61, 31) hoher Konzentration in Teile des Kanalgebiets erstrecken, neben den Source- und Draingebieten (27, 29, 63, 65) und direkt unter den Source- und Draingebieten (27, 29, 63, 65).

Revendications

1. Transistor à effet de champ MOS, comprenant :
   - un substrat semi-conducteur (21, 51) présentant un premier type de conductivité,
   - des régions de source et de drain (27, 29, 63, 65) formées à une certaine distance l'une de l'autre dans une zone de surface du substrat (21, 25), et
   - une électrode de grille (23, 59a, 59b) formée sur une surface du substrat (21, 51) par l'intermédiaire d'un film isolant de grille (25, 55) formé sur celle-ci entre les régions de source et de drain (27, 29, 63, 65),
   - une région de canal située dans la zone de surface du substrat entre les régions de source et de drain qui est constituée de régions de concentration différente , et une tension de seuil de la région de canal à concentration élevée (31, 61) qui est inférieure à celle d'une région de canal à faible concentration,

   caractérisé en ce que
   - l'électrode de grille (23, 59a, 59b) est constituée d'un élément de grille central (23a, 59a) formé dans une partie centrale de l'électrode de grille et d'éléments de grille latéraux (23b, 59b) formés sur les deux parties d'extrémités latérales de l'électrode de grille,
   - l'élément de grille central (23a, 59a) se trouve au-dessus de la région de canal à faible concentration et les éléments de grille latéraux (23b, 59b) se trouvent au-dessus de la région de canal à concentration élevée (31, 61) contigue aux régions de source et de drain,
   - l'élément de grille central (23a, 59a) comprend soit un film semi-conducteur non dopé, soit un métal, soit un siliciure metallique,
   - les éléments de grille latéraux (23b, 59b) comprennent un film semi-conducteur ayant un second type de conductivité différent du premier type de conductivité.

2. Transistor selon la revendication 1, dans lequel les régions de canal à concentration élevée (61, 31) s'étendent dans des parties de la région de canal, contiguës aux régions de source et de drain (27, 29, 63, 65) et directement sous les régions de source et de drain (27, 29, 63, 65).

* C L M S *