

ABSTRACT

A fail detecting method of a memory system including a nonvolatile memory device and a memory controller, the fail detecting method including: counting, by the memory controller, the number of erases of a word line connected to a pass transistor; issuing a first erase command, by the memory controller, when the number of erases reaches a reference value; applying a first voltage, by the nonvolatile memory device, in response to the first erase command, that causes a gate-source potential difference of the pass transistor to have a first value; detecting, by the memory controller, a leakage current in a word line, after the applying of the first voltage; and determining, by the memory controller, the word line as a fail when a leakage voltage caused by the leakage current is greater than a first threshold value.

FIG. 4A