

ELECTRONIC SPEED-CONTROL CIRCUIT

This invention relates to electronic circuits, and more particularly to an electronic circuit for controlling or regulating the speed of rotation of a microgenerator, of the type having a first input and a second input which can
5 be connected to the microgenerator, an oscillator supplying a reference signal of a predetermined frequency, an energy-dissipation circuit for braking the microgenerator, energy-dissipation control means for controlling the energy dissipation of the energy-dissipation circuit as a function of the reference signal and of the signal between the mentioned inputs, a rectifier and voltage-
10 multiplying circuit for rectifying and multiplying the signal between the first and second inputs, the rectifier and voltage-multiplying circuit containing at least one capacitor which can be charged by the microgenerator via at least one switch, and at least one control circuit of the mentioned switch or switches.

The invention further relates to a watch movement containing a
15 circuit of the aforementioned type.

Numerous miniaturized electronic and electromechanical apparatus require an independent source of power. This source often consists of a battery pack or of solar cells. Batteries lead to various kinds of trouble, such as limited life, annoyingly frequent replacement, increased costs, and pollution of
20 the environment. Solar cells operate only when there is sufficient light and require an additional store of energy. Further, their disposal may likewise lead to environmental problems, and fitting them into miniaturized apparatus such as watches, for instance, is difficult and leads to significant design restrictions.

In order to avoid such trouble, it has been proposed, e.g., in
25 Japanese Laid-Open Application No. 50-006373, to replace the batteries of a watch movement by a generator and a spring driving the generator. The watch movement described contains a spring which, via gearing, drives a time display and a generator supplying an AC voltage. The generator feeds a rectifier, the rectifier feeds a capacitive component, and the capacitive component feeds an
30 electronic reference circuit having a stable quartz oscillator and an electronic control circuit. The electronic control circuit has a comparator logic element

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and an energy-dissipation circuit connected to the output of the comparator logic element and controllable in its power draw by the comparator logic element. One input of the comparator logic element is connected to the electronic reference circuit and another input of the comparator logic element is
5 connected to the generator. The comparator logic element is designed in such a way that it compares a clock signal coming from the electronic reference circuit with a clock signal coming from the generator, controls the magnitude of the power draw of the energy-dissipation circuit as a function of the result of this comparison, and in this way, via the control of the control-circuit power
10 draw, controls the running of the generator and thus the running of the time display. In such a watch, the advantages of a mechanical watch, i.e., the absence of batteries, are combined with the accuracy of a quartz watch.

Japanese Patent No. 62-255 889 and European Patent No. 679968 describe different electronic circuits for controlling the speed of a
15 microgenerator in which a monitoring circuit constantly monitors the angular position of the rotor and brakes it as soon as its angular position is in advance. Because of their sensitivity to errors and phase variations of the components, these circuits are difficult to manage.

International Patent Application No. PCT/EP96/02791, the
20 disclosure of which is incorporated in the present application by reference, describes an improved electronic control circuit which can be used in such a device. This application describes in particular a control circuit in which a voltage multiplying circuit rectifies and multiplies the signal between the terminals of the generator. The voltage multiplying circuit contains various
25 capacitors C1, C2, C3 fed by the microgenerator through active elements, e.g., through field-effect transistors instead of diodes. Diodes are used only for initializing the system. In this way, the energy efficiency of the circuit can be greatly improved in that the threshold voltage losses of the diodes are avoided. Thus, the circuit can operate with a lower generator voltage, allowing a
30 reduction in size of the generator and the spring and an increase in the power reserve of the watch movement. Furthermore, means are described for interrupting the braking of the microgenerator periodically so that optimum charging of the capacitors is ensured.

It is the object of this invention to propose an improved electronic control circuit which can be operated in a particularly favorable manner as regards power consumption.

To this end, in the electronic circuit according to the present invention for regulating the speed of rotation of a microgenerator, of the type
5 originally mentioned, the control circuit of the switch or switches contains at least one storage means which in a first phase with blocked switch stores at least one control signal to be applied to the switches, and in a second phase the switches are triggered by means of the control signal.

10 Preferred embodiments of the invention will now be described in detail with reference to the accompanying drawings, in which:

Figure 1 is a block circuit diagram of the inventive electronic circuit,

15 Figure 2 is a diagram of a rectifier and voltage-multiplicating circuit,

Figure 3 is a diagram of a first comparator used in the rectifier and voltage-multiplicating circuit,

Figure 4 is a diagram of a second comparator use in the rectifier and voltage-multiplicating circuit,

20 Figure 5a is a diagram of a logic circuit generating two signals, latch and meas,

Figure 5b is a wave diagram of the latch and meas signals,

Figure 6 is a diagram of a power source supplying various parts of the circuit with power,

Figure 7 is a frequency divider which divides the frequency generated by a quartz oscillator,

Figure 8 is a diagram of a circuit for starting up the system upon initialization,

5 Figure 9 is a diagram of a counter, the reading of which is dependent upon the frequency difference between the generator and a reference frequency,

Figure 10 is a diagram of a control circuit controlling the energy dissipation of the energy-dissipation circuit,

10 Figure 10a is a graph showing the development of the braking current across the resistors R_f , which are selected as a function of the counter reading, and

Figure 11 is a diagram of an energy-dissipation circuit.

Figure 1 is a block diagram of an inventive electronic circuit 11
15 for controlling or regulating the speed of a microgenerator 1. Circuit 11 is fed by microgenerator 1 whose speed it regulates via a capacitor C3 which temporarily stores the energy supplied by generator 1. Microgenerator 1, which generates an AC voltage, is driven by a spring (not shown) via gears (not shown). The gears further drive the hands (not shown). Circuit 11 controls the
20 power draw of an energy-dissipation circuit 9 (Figure 11) connected to microgenerator 1, so that the frequency of rotation of the rotor of microgenerator 1 is synchronized with the reference frequency at the output of a frequency divider 5, the input of which is fed by a quartz oscillator 3, 4.

The microgenerator used may, for example, be such as is
25 described in European Patent Application No. 96810901.7, the disclosure of which is specifically incorporated here by reference. The nominal frequency of the AC voltage of microgenerator 1 is preferably 2^n , n being a natural number other than zero. The mechanical portion of the watch movement forms part of

the prior art and is described, for example, in Japanese Laid-Open Application No. 50-006373.

Microgenerator 1 is connected to the two inputs G- and G+ of electronic circuit 11. Circuit 11 preferably takes the form of a single IC. Inputs G- and G+ are connected to a rectifier and voltage-transformer circuit 2, the function of which is described below with reference to Figures 2-5. Rectifier and voltage multiplying circuit 2 charges a storage capacitor 10 (C3), which temporarily stores the electrical energy generated by microgenerator 1 and supplies the energy to the IC in the form of a substantially continuous voltage. Rectifier and voltage multiplying circuit 2 also uses two further capacitors 16 (C1) and 15 (C2). Capacitors C1, C2, and C3 are preferably external, although they may possibly be integrated in IC 11.

In the embodiment illustrated, energy-dissipation circuit 9 is connected in parallel with microgenerator 1. However, energy-dissipation circuit 9 might instead be disposed on the other side from rectifier and voltage transformer 2, connected in parallel with capacitor C3. Energy-dissipation circuit 9 consists of an ohmic resistor, the resistance of which is controlled by energy-dissipation control means 30 (Figure 10). Energy-dissipation circuit 9 might also consist of an adjustable power source. The speed of rotation of the rotor of microgenerator 1 is controlled by varying the resistance.

A stabilized power source 32, described in detail with reference to Figure 6, produces different stabilized currents pp, pn, intended to feed rectifier and voltage transformer 2 and elements 3, 7, 31. Stabilized power source 32 procures its energy from capacitor C3 which feeds the entire IC. Oscillator 3, 4 supplies a reference signal having a predetermined frequency. Oscillator 3, 4 has a quartz 4 which is preferably mounted outside IC 11 and the oscillations of which define a reference frequency at the output of oscillator 3. By means of frequency divider 5, this reference frequency is divided by a predetermined factor described in detail with reference to Figures 7 and 8.

The IC further comprises a counter 6, which is described in detail with reference to Figure 9. A decrementing input (DOWN) of counter 6 is

connected to the output of frequency divider 5, while the incrementing input (UP) of counter 6 is connected to microgenerator 1 via a hysteresis comparator, which ascertains the zero transitions of the signal at the output of microgenerator 1, and via an anticoincidence circuit 8. Anticoincidence circuit 8 prevents UP and DOWN pulses from coming in simultaneously at both inputs of counter 6, which might otherwise behave unpredictably. For this purpose, circuit 8 synchronizes the UP and DOWN signals with signals of different phases coming from frequency divider 5. The IC further comprises an internal voltage doubler 31 making it possible to feed and trigger the energy-dissipation control means 30 and the energy-dissipation circuit 9 with a higher voltage $HV > V_{dd}$ and a lower voltage $LV < V_{ss}$.

Energy-dissipation control means 30 control the energy dissipation of energy-dissipation circuit 9 as a function of the reference signal generated by quartz oscillator 3, 4 and of the signal coming from microgenerator 1. When the rotor of microgenerator 1 turns too fast, the frequency of the signal between inputs G+ and G- is higher than the frequency of the reference signal at the output of frequency divider 5.

Therefore, during a given interval, counter 6 receives more pulses at its incrementing input UP than at its decrementing input DOWN; its count thus increases. As a function of this count, the energy-dissipation control means 30 control the resistance of energy-dissipation circuit 9 and, consequently, the energy dissipation, in such a way that microgenerator 1 is braked. In this way, the rotational frequency of microgenerator 1—and thus the running of the time display as well—is synchronized with the reference frequency coming from the quartz oscillator.

The regulating value B1:B31 supplied to energy-dissipation circuit 9 by energy-dissipation control means circuit 30 depends in this embodiment upon the reading of counter 6, i.e., upon the difference between the number of pulses of the signal UP coming from microgenerator 1 and the number of DOWN pulses coming from quartz oscillator 3, 4 since the watch started running. The type of control or regulation is therefore integral. Other types of control, e.g., a regulation proportional to the momentary frequency

difference or to the gradient of the frequency difference, or a proportional-integral derived (PID) control, may also be used. In the embodiment illustrated, the speed of rotation of the rotor is controlled by regulating the braking resistance in energy-dissipation circuit 9; however, an on-off control might be
 5 used instead.

As mentioned, energy-dissipation control means 30 comprises a hysteresis comparator 7 which compares the signals G+, G- at the two inputs connected to microgenerator 1. Thus the signal Gen at the output of comparator 7 is a rectangular signal which changes its state upon each change
 10 of polarity of the signal between the inputs G+, G-. The use of a hysteresis comparator allows disturbances of the signal between the inputs G+, G- to be filtered out. To avoid unwanted changes in value of the signal Gen which would lead to erroneous incrementations and thus to excessive braking of microgenerator 1, other filter means may be provided, e.g., a low-pass or band-
 15 pass filter, or a filter which changes its state only after a predefined period of time. Hysteresis comparator 7 is fed by power source 32.

Rectifier and voltage-multiplicating circuit 2 is shown in Figures 2-5.

In order to achieve the greatest possible efficiency, the diodes
 20 normally used are replaced in this circuit by switches 17, 18, 19 and comparators 20, 21 triggering these switches, as already proposed in the aforementioned International Patent Application No. PCT/EP96/02791. A first switch 19 is connected in series with microgenerator 1 and with the earlier mentioned storage capacitor C3.

25 First switch 19 preferably consists of a field-effect transistor which, immediately after starting of the watch movement, acts as a simple diode. At that moment, the voltage drop across switch 19 is equal to the diode threshold voltage, about 400 mV. As soon as the potential of capacitor 10 is high enough for the internal power source, and thus also the comparators, to
 30 function, the transistors acting as switches are triggered by the comparators. When the voltage supplied by the voltage-tripler circuit is higher than the

voltage of capacitor 10, the first field-effect transistor is enabled. However, the voltage drop across the channel of the field-effect transistor amounts to only about 10 mV. Hence when transistors and the comparators triggering the transistors are used instead of diodes, the voltage loss is considerably
 5 reduced, the energy reserve of the watch movement is used more economically, and the power reserve is increased.

Field-effect transistor 19 is not disabled again until the voltage C2 supplied by the voltage-tripler circuit again drops below the voltage Vdd of first capacitor 10.

10 First switch 19 is controlled by a signal /ser transmitted by a first comparator circuit 21 shown in Figure 4.

Comparator circuit 21 has a comparator 210 which compares the voltage on both sides of switch 19. When voltage C2 on the left-hand side of switch 19 is higher than the voltage Vdd on the right-hand side, the output of
 15 comparator 210 passes from 0 to 1.

Normal comparators always have a (positive or negative) offset voltage V_o . In order for the output of comparator 210 to pass to 1, the following condition must therefore be met:

$$C2 > Vdd + V_o$$

20 If, for instance, the offset voltage is +2 mV, the difference of potential across switch 19 must amount to 2 mV or more in order for the output of comparator 210 to pass to 1.

If, however, switch 19 were directly controlled by comparator 210, switch 19 would close as soon as the difference of potential was 2 mV or
 25 more. Yet because the internal resistance of this switch is low, the voltage drop across the closed switch can be smaller than the offset voltage. In this case, switch 19 would be immediately reopened. The difference of potential across switch 19 would then be present again, so that the output of the

comparator would again pass to 1, and switch 19 would close again: the system could oscillate.

In order to avoid this problem, the present invention provides for a time difference between measuring and switching. First, switch 19 is blocked
 5 by the meas signal, and the comparator is thereby able to detect the difference of potential across the switch. Thereafter, the value at the output of comparator 210 with transistor 19 disabled is stored in a storage element 211 by means of a latch signal. Not until after a certain interval do the meas and latch signals pass to 0, and switch 19 is triggered by means of the value ser stored in
 10 storage element 211. In this way, it is ensured that the system does not oscillate and that the current flows from C2 to Vdd.

The formation of the two delayed signals latch and meas, shown in Figure 5b, is described with reference to Figure 5a. A NAND gate 3081, which combines the 16kHz, 8kHz, 4kHz, 2kHz, and 1kHz signals supplied by
 15 frequency divider 5, transmits a signal p. Accordingly, pulsing signal p always has a value of 1 except once per 1kHz cycle during a 16kHz half cycle. This signal at the output of NAND gate 3081 is inverted by an inverter 3082 connected to an AND gate 3083. A power-on reset signal rud, the formation of which is explained below with reference to Figure 8, is supplied at the other
 20 input of gate 3083. When the circuit is started up, the rud signal is zero, thereafter always one. Thus, the meas signal supplied by gate 3083 is always zero except after starting-up, when the logical state of p is 1.

Signal p at the output of NAND gate 3081 is also transmitted to an OR gate 3084 which likewise receives a 32kHz signal coming from
 25 frequency divider 5. The signal r supplied by gate 3084 consequently always has a value of zero except when p and the 32kHz signal are simultaneously zero, i.e., once per 1kHz cycle during half a 32kHz cycle. This signal is validated by the rud signal and inverted by means of a NAND gate 3085. Thus, the latch signal supplied by gate 3085 equals only when r has assumed a value
 30 of 1 and when rud is not simultaneously zero. The latch signal is used in this way in order to store the state at the outputs of comparators 20 and 21, respectively, in storage elements 201, 211 in comparator circuits 20, 21.

The meas and latch signals can be formed only when the quartz oscillator and the divider chain are working. This is not the case, however, when the circuit starts up, so the circuit must be designed in such a way that when the system is started up, the switches are triggered directly by the comparators: when the system is set running, the meas and latch signals are kept at zero and one, respectively, by the rud signal. Switch 19 is thereby triggered directly by comparators 20, 21. As soon as the rud signal passes to one, meaning that the quartz oscillator and the divider chain are working, switch 19 is triggered by means of the value stored in storage means 211.

Voltage tripler 15, 16, 17, 18 comprises a second capacitor 15 (C2) and a third capacitor 16 (C1) connected in series with microgenerator 1 at inputs G+ and G-. A second switch 17 is connected between input G- and the grounded end of third capacitor 16 opposite microgenerator 1. A third switch 18 is connected between input G+ and the end of second capacitor 15 opposite microgenerator 1 which is connected to first switch 19. Switches 17 and 18 are controlled by a second comparator circuit 20 (Figure 3) which compares the electric potential of input G-, connected to second capacitor 15, with the potential of the ground.

Switches 17 and 18 likewise consist of field-effect transistors acting in the disabled state as diodes. When the watch movement starts running, capacitors 15 and 16 are charged by the diode structures of transistors 17 and 18. As soon as the comparators are working and the voltage of the generator at junction G- is lower than V_{ss} , second comparator circuit 20 flips with the next edge of the meas signal, and with the edge of the latch signal the state of the comparator is stored in storage element 201 and the switches are triggered by means of the stored values. Transistors 17 and 18 are then conducting. Capacitors 15 and 16 are consequently charged solely over the channels of transistors 17 and 18, which proves to be favorable energy-wise. It should be noted that input G-, connected to microgenerator 1, is grounded over the channel of transistor 17 as soon as the latter becomes conducting.

Other voltage multiplying circuits are described in the earlier mentioned International Application No. PCT/EP96/02791 and in European Patent No. 695,978, for example.

Comparators 200 and 210 (Figures 3 and 4) are fed by voltage V_{dd} stored in capacitor C3. They further require current feeds pp and pn, respectively, which is managed through power source 32 explained in Figure 6. The comparators do not work as long as the respective currents pp and pn are not high enough; in that case, their outputs remain in zero state so that the controlled switches 17, 18, 19 remain blocked.

Power source 32 consists of a conventional current mirror. It comprises a resistor 321 having a high value, e.g., 300 Ω , connected between the ground and the source of an n-channel field-effect transistor 322. The drain of transistor 322 is connected in series with the drain of field-effect transistor 323a and with the gates of three p-channel transistors 323a, 323b, and 323c, the source of the latter being fed by the voltage generated by voltage transformer 2. The drain of transistor 322 is further connected to the gates of the three p-channel field-effect transistors 323a, 323b, and 323c as a mirror circuit. The pp current flowing through the channel of transistor 322 and resistor 321 feeds comparator 200 illustrated in Figure 3.

The drain of transistor 323a is connected to the drain of n-channel transistor 322 and in series with the gates of n-channel transistors 322a', 322b', 322c', and 322d' and as a mirror concerning transistor 322. The source of transistor 322a' is grounded. The pn current flowing through transistors 323a', 323b', and 323c' feeds comparator 210 illustrated in Figure 4.

The mode of operation of this type of power source with current mirror is known per se and is consequently described only briefly. When the pp current increases, the current drop across resistor 322 likewise increases, and the voltage at the drain of transistor 322 accordingly increases as well. The voltage applied to transistors 322a', 323b', and 323c' is consequently increased, which leads to their disabling, so that the voltage at the drain of p-channel transistor 323a' decreases. This voltage is applied to the gate of p-

channel transistor 322, which becomes less conducting since its gate voltage is reduced. Accordingly, transistor 322 has the tendency to become disabled and to limit the pp current.

Conversely, a lessening of pp leads to a reduction of the voltage
 5 drop across resistor 323 and hence to a voltage reduction which is applied to the gates of p-channel transistors 323a', 323b', and 323c'. These consequently become more conducting, leading to an increase of the voltage at the drain of transistor 323a' applied to the gate of transistor 322. The latter therefore becomes more conducting and allows an increase of the pp current flowing
 10 through. The pp current is stabilized and thus depends only slightly upon the load applied. It is easily shown that the pn current flowing through transistors 323a', 323b', and 323c' is stabilized in the same manner.

The magnitude of the current can therefore be determined by
 adapting the characteristics of the elements in the power source, particularly
 15 the number of transistors and the size of their channels. It is thus possible to determine the currents pp and pn freely through the two branches of the mirror.

Such a current mirror has two stable states. The first one has been described and is achieved when the pp and pn currents have reached the desired intensities. The second state corresponds to the pp and pn currents
 20 equal to zero. This second state is achieved when all transistors are disabled. It exists particularly when voltage is applied to the system, after which the pp and pn currents are thus zero. An n-channel initializing transistor 320 is provided in order to force a current through current mirror 32 in the starting-up phase so that it reaches its first stable state. The gate of transistor 320 is
 25 grounded, while its source is connected to input G- of microgenerator 1. The drain of initializing transistor 320 is connected to the gates of the p-channel transistors. During the starting-up phase of the watch movement, microgenerator 1 is floating with respect to ground. Signal G- at the input of microgenerator 1 consequently oscillates in an approximately sinusoidal
 30 manner in relation to ground. When input signal G- is negative, i.e., is below ground voltage, transistor 320 becomes conducting, and the negative voltage of G- is applied to the gates of p-channel transistors 323a', 323b', and 323c'.

Hence these transistors suddenly become conducting so that only a pn current circulates, the voltage at the gate of transistor 322 rises, and this transistor also conducts a pp current. As explained above, this current is applied to comparator 20 (Figure 3) in the rectifier and voltage multiplying circuit 2,
 5 which begins to operate. The output signal of comparator circuit 20 changes its state, as indicated in Figure 2, when the voltage at the junction G- is lower than Vss, and enables transistors 17 and 18, thus grounding input G- of microgenerator 1 and connecting input G+ of microgenerator 1 to C2. As soon as input G- is grounded, transistor 320 is disabled and thereafter ceases to
 10 consume current. Power source 2 is henceforth initialized, and the pp and pn currents quickly attain the desired values.

The power source may easily be completed, e.g., by means of other n-channel transistors, the gates of which are connected to the drain of transistor 323a' and the sources grounded. Thus, the current through these
 15 transistors can easily be controlled for feeding other components, e.g., components of quartz oscillator 3, 4.

Figure 7 illustrates a preferred embodiment of the invention comprising a frequency divider 50 consisting of ten D-flipflops connected in series. The frequency of the signal is divided by 2 at each flipflop. When the
 20 reference signal supplied by oscillator 3, 4 at the input of frequency divider 50 oscillates at 32 kHz, the frequency of the signal at the output of divider 50 is 2^{-10} 32 kHz, i.e., 32 Hz. This signal is combined by a circuit 500 with the 4 kHz signal in order to generate a DOWN signal which assumes the logic state 1 just once per cycle of 32 Hz and during a half cycle of 4 kHz.

Figure 8 illustrates a circuit 51 which delivers a power-on reset signal rud. This signal is intended, among other things, to reset counter 6 to a predetermined value upon initialization and to cut out energy-dissipation circuit 9. Circuit 51 comprises three p-channel field-effect transistors 510, 511, and 512 disposed in series with a p-channel transistor between ground and the
 30 feed. The gates of the three p-channel transistors receive the pp signal coming from power source 32. During initialization, the three transistors 510, 511, and 512 remain disabled as long as power source 32 does not supply sufficient

current. Hence the voltage at point 516 is zero. An inverter 550 converts this voltage into a signal POR1 which is combined by means of an OR gate 528 with a signal POR2. The signal at the output of gate 528 is relayed to a flipflop consisting of two NOR gates 517 and 518 and having two inputs. The other
 5 input of flipflop 517, 518 is connected to the output of a frequency divider 520 composed of five flipflops 521-526. The 32 Hz output signal supplied by frequency divider 50 is connected to the input of the first flipflop 521. The /reset inputs for resetting flipflops 521-526 are connected via an inverter 527 to the output of inverter 515.

10 Upon initialization, signal POR1 is binary one as long as the power source does not supply sufficient power. Similarly, signal POR2 is binary one as long as the frequency from frequency divider 5 does not reach a predetermined value. Consequently, the signal at the output of gate 528 is not zero until the quartz oscillator and the power source are both working.

15 Upon initialization, this signal is still at 1, so that flipflops 521-526 are all set to zero. The input of flipflop 517, 518 connected to flipflop 526 thus receives the logic state zero, whereas the input connected to inverter 515 receives the logic state 1. The signal is inverted by inverter 519 into a signal called rud (reset up-down counter) and having a logic value of zero.

20 As soon as the power source is supplying enough power, the three transistors 510 to 512 become conducting. The signal at point 516 is therefore Vdd, so that inverter 515 supplies a signal POR1 having a logic value of zero. When the quartz oscillator is also working, a logic value of zero is supplied through gate 528 to flipflop 517, 518 having two inputs, while the /reset inputs
 25 of flipflops 521-526 receive the logic value 1. Frequency divider 520 starts to divide the 32 Hz frequency supplied. After one second, the signal at the output of flipflop 560 passes to 1. Since the two inputs of flipflop 517, 518 receive the logic value 1, its output passes to zero, so that signal rud reaches the logic value 1. This value is then maintained as long as the current pp is sufficient
 30 and the quartz oscillator is also working.

When the generator is stopped, e.g., when the watch movement is being set, capacitor 10 (C3) is no longer fed by the generator. However, the IC continues to consume power, so voltage Vdd at C3 drops more and more. When the voltage has dropped so far that the quartz oscillator no longer functions, the meas and latch signals are no longer formed.

However, since it is not ensured that capacitor 514 is discharged quickly enough, it may happen that, although the circuit no longer has sufficient voltage, signal POR1 does not pass to binary one. The second power-on reset signal POR2 passes to binary one, however, as soon as the frequency from the frequency divider drops below a certain value. Thus, after a brief interval, signal rud appears again, so that switches 17, 18, 19 of the voltage transformer are triggered directly by comparators 200, 210 in this case, too.

In an embodiment which is not illustrated, the start-up of the IC is ensured only by means of signal POR2 from the frequency divider. Signal POR2 remains at zero. Figure 9 illustrates a preferred design of counter circuit 6. In this design, circuit 6 comprises a 6-bit counter 60 which is formed, for example, by six resettable D-flipflops connected in series. The binary number formed by outputs Q1 to Q6 increases by one unit with each leading edge supplied to input 601. The counter is reset when a signal rud is supplied to reset-input 603.

A maximum detector 63 consisting of the two NAND gates 61, 62 and the OR gate blocks, by means of a NAND gate 64, the introduction of new UP pulses at incrementation input 601 when the maximum output state $Q1=Q2=...=Q6=1$ is reached. In the same way, a minimum detector 65, 66, 67, 68 prevents all counting down below the minimum output state $/Q1=/Q2=...=/Q6=1$. False counts outside the counting limits of counter 60 are thus prevented owing to the two state detectors.

Signals Q1-Q6, supplied by counter 6, allow the coding of 64 different braking values. There is minimum braking when $Q1=Q2=...=Q6=0$ (level 0) and maximum braking when $Q1=Q2=...=Q6=1$ (level 63). According to

the present invention, however, braking of the microgenerator does not increase linearly between these minimum and maximum values. The energy dissipation across braking resistor R_f of energy-dissipation circuit 9 preferably develops in such a way as plotted in the graph of Figure 10A. Between 0 and 31, the frequency difference integrated by counter 6 between microgenerator 1 and oscillator 3, 4 is slight: no braking is caused. This allows fast acceleration of the microgenerator when the watch is set running, so the nominal speed is very quickly reached. Between 32 and 61, the energy dissipation increases linearly with a moderate rise. From level 62 on, the energy dissipation increases with a much sharper rise and reaches its maximum at level 63, so that the rotor of the microgenerator is braked hard if it starts spinning.

Figure 10 illustrates energy-dissipation control means 30. They convert signals Q1:Q6 from the counter into signals B1:B63, which directly activate energy-dissipation circuit 9 shown in Figure 11. As already explained in connection with Figure 1, energy-dissipation circuit 9 is connected directly between inputs G+, G- of the microgenerator. It consists of a plurality of resistors 910 to 916 integrated in the IC. Switches 900 to 906, controlled by signals B1 to B5 and B62, 63 coming from energy-dissipation control means 30, permit modification of the number of parallel-disposed resistors. According to Figure 10A, the resistances of resistors 910 to 916 are inversely proportional to the strength of control signals B1-B63: signals B62 and B63 thus control more effective braking than, e.g., signal B1.

Switches 900 to 906 are n-channel field-effect transistors. When the potential at the gate of the transistor is 0, the transistor is disabled, hence no current flows through the transistor. However, as soon as the potential at the source of the respective transistor is below V_{ss} , the transistor becomes conducting. This means that the generator is braked because now a current is flowing since the resistors are connected between the terminals (G+ and G-) of the generator.

Depending upon which circuit is used, however, it is indispensable that the generator attain a substantially higher speed of rotation than the rated speed of rotation, and thus the highest possible output voltage,

in order for the circuit to be able to start up at all. In this connection, however, it is possible for the voltage at G+ and G- to be less than Vss, so that the generator is then braked because the switching transistor for the brake becomes conducting. Yet if the high speed of rotation and thus the high output
 5 voltage are not attained, the circuit cannot start up because of the voltage drop across the diodes.

Now, in order that the generator may not be braked by energy-dissipation circuit 9 upon starting of the system, it is necessary to connect at least one p-channel field-effect transistor and at least one n-channel field-effect
 10 transistor in series if they are to serve as switches for connecting braking resistors between G+ and G-. According to the present invention, this is solved by means of a p-channel field-effect transistor 920. Transistor 920 can conduct only if the potential at the gate is lower than one threshold value below the source potential. That is certainly not the case when the system starts up, so
 15 that the generator is not braked, and it is possible to start the system.

N-channel and p-channel transistors can be used as good switches only in the vicinity of Vss and Vdd. If the potential at drain and source is somewhere between Vdd and Vss, it no longer suffices to trigger the gate with Vdd or Vss in order for the transistors to become conducting.

20 This is precisely the case with energy-dissipation circuit 9 and with switch 19 of the voltage doubler:

In order that the transistors may be used as switches under these conditions, the gate of the n-channel transistor must now be triggered with a voltage higher than Vdd in order for the transistor to conduct well. The
 25 same applies to the p-channel transistor, the gate of which must be activated with a voltage which is at least one threshold value lower than Vss in order for the transistor to become properly conducting.

Hence transistor 920 is not activated by means of Vss but rather by means of an LV signal which in active state has a substantially lower voltage
 30 than Vss. The formation of LV in circuit 30 is described in more detail below.

In the same way, n-channel transistors 900:906 cannot be triggered directly by means of signals Q1:Q6 from the counter because these signals cannot be higher than Vdd. These transistors are therefore activated by means of signals B1:B63, the logic states of which correspond to those of Q1:Q6, but the voltages of which are doubled. For this purpose, signals Q1-Q5
 5 are converted into output signals B1-B5 in energy-dissipation control means 30 by means of level shifters 301-305.

In another embodiment of the invention (not shown), for similar reasons, switch 18 of voltage multiplying circuit 2 is triggered by means of a
 10 signal having the same logic state as the signal par but a higher voltage. It would be equally possible to double the voltages of the signals par and ser which trigger switches 17 and 19.

Level shifters 301-305 in Figure 10 are fed by a voltage HV obtained by doubling the voltage Vdd at capacitor C3 by means of a voltage
 15 doubler 31 (not shown). In order for the circuit to start up reliably, the voltage doubler must be so constructed that it supplies a voltage at least equal to Vdd even at the time of initialization. For this purpose, voltage doubler 31 may, for example, be triggered by signal rud already described, so that at the time of initialization, it supplies a voltage Vdd, and doubled voltage HV only after
 20 signal rud has changed its state when the quartz oscillator and the power source are both working.

The logic state "62" is indicated by an AND gate 306 when signals B2, B3, B4, and B5 are all at binary 1 (decimal 62 corresponds to binary 111110). Gate 306 multiplies signals B2 to B5 and supplies a signal
 25 B62 having the logic state 1 only when the count reaches levels 30 or 31. A second AND gate multiplies B62 by B1 in such a way that the logic state "63" is indicated by means of a signal B63. Signals B62 and B63 directly control transistors 905 and 906, respectively.

As already mentioned, circuit 30 supplies an LV signal intended
 30 to trigger p-channel transistor 920 in energy-dissipation circuit 9. The LV signal is generated by a level shifter 300. As already mentioned, in order for

transistor 920 to be properly conducting, the voltage of the LV signal in the active state must be at least one threshold value lower than V_{ss} . For this purpose, the output of level shifter 300 is connected to a capacitor 3005. A transistor 3006, functioning as a diode, is connected between the other side of capacitor 3005 and the point /rud. Transistor 3006 has a threshold value of U_e , e.g., 400mV. When level shifter 300 supplies a voltage HV, the voltage charged in capacitor 3005 is ΔU_{HV-U_e} . If the voltage at the output of level shifter 300 suddenly drops to V_{ss} , the voltage of the LV signal drops to $V_{ss} - (HV - U_e)$, which permits transistor 920 to be made conducting.

When the system is initialized, signal /rud is at binary one, so that LV also remains at binary one, and transistor 920 is disabled. Transistor 920 cannot conduct until signal /rud is at binary zero.

Level shifter 300 is controlled by a signal /b in such a way that energy-dissipation circuit 9 brakes when signal /b is at binary zero. Signal /b is transmitted by a NAND gate 3080 which logically combines signals Q6 and p. Signal /b is at 1 when at least one of those two signals is zero. For example, if Q6 is zero, i.e., if counter 6 has not reached at least level 16, signal /b is 1, so that energy-dissipation circuit 9 can brake only from level 16 of the counter on, according to the graph in Figure 10A. The formation of pulsing signal p by circuit 308 has already been explained with reference to Figure 5a. Consequently, pulsing signal p always has a value of 1 except once per 1kHz cycle during a 16kHz half cycle. This serves the purpose of recharging the capacitor which produced the LV. Here braking is interrupted by pulsing signal p once per millisecond (pulsed braking). However, solutions are also conceivable using LV1 and LV2, hence two p-channel transistors, so that braking need not be interrupted.

In order for the system to be stable, the charging of capacitors C1, C2, and C3 must be separate from the braking, i.e., the moment of braking must not be dependent upon charging. In the circuit shown in Figure 10, braking takes place during the entire period. The voltage drop is consequently relatively small; moreover, this voltage drop exists only when hard braking takes place. This is tantamount to a high driving moment and thus to greater

certainty that after an impact, the generator can be rapidly accelerated again and the system again supplied with power. It would also be possible, however, to separate braking and charging altogether. For example, during one positive and negative half-wave first only braking would take place, and during the next
5 positive and negative half-wave only the capacitors would be charged. Thus the voltage drop caused by braking is omitted, and the capacitors are charged to the maximum.

**CLAIMS**

1. An electronic circuit for regulating the speed of rotation of a microgenerator (1), comprising:

5 a first input (G+) and a second input (G-) which can be connected to the microgenerator (1),

 an oscillator (3, 4) supplying a reference signal of a predetermined frequency,

 an energy-dissipation circuit for braking the microgenerator (1),

10 energy-dissipation control means (5, 6, 7, 8, 30, 31) for controlling the energy dissipation of the energy-dissipation circuit (9) as a function of the reference signal and of the signal between said inputs (G-, G+),

 a rectifier and voltage-multiplicating circuit (2) for rectifying and multiplying the signal between said first and second inputs, the rectifier and
15 voltage-multiplicating circuit comprising at least one capacitor (C1; C2; C3) which can be charged by said microgenerator via at least one switch (17, 18, 19), and

 at least one control circuit (20; 21) of said switch or switches (17, 18, 19),

20 characterized in that said control circuit (20; 21) comprises at least one storage means (201; 211) which in a first phase with blocked switch stores at least one control signal to be applied to said switches (17, 18, 19), and that in a second phase said switches (17, 18, 19) are triggered by means of said control signal (ser/par).



2. An electronic circuit according to the preceding claim, characterized in that said control circuit (20, 21) comprises a comparator (200, 210).

3. An electronic circuit according to claim 1, characterized in
5 that braking is blocked during every second cycle of the signal from the microgenerator.

4. An electronic circuit according to claim 1, characterized in that said energy-dissipation circuit (9) is connected between said inputs (G-, G+) intended for connection to the microgenerator.

10 5. An electronic circuit according to claim 1, characterized in that said energy-dissipation circuit (9) is connected between the inputs intended for connection to said capacitor (10) charged by the microgenerator.

6. An electronic circuit according to claim 1, characterized in that said energy-dissipation control means (5, 6, 7, 30, 31) have a counter (6),
15 the count of which depends upon the frequency difference between the microgenerator (1) and the oscillator (3, 4), the energy dissipation of the energy-dissipation circuit being a function of said count.

7. An electronic circuit according to the preceding claim, characterized in that the count of the counter (6) increases with each pulse of
20 an incrementation signal (UP) coming from the signal between the two inputs (G-, G+) and decreases with each pulse of a decrementation signal (DOWN) coming from said oscillator (3, 4).

8. An electronic circuit according to the preceding claim, characterized in that it comprises means (51, rud) for resetting said counter (6)
25 to a predetermined value when a voltage is applied to the circuit.

9. An electronic circuit according to claim 1, characterized in that it comprises initialization means (51) which transmit a signal (POR1) of a specific value as long as the current supplied by said stabilized power source



(32) does not reach a given value, and a signal of the opposite value is transmitted as soon as the current supplied by said stabilized power source (32) exceeds said predetermined value.

10. An electronic circuit according to claim 1, characterized in
5 that it comprises initialization means which transmit a signal (POR2) of a specific value as long as the quartz oscillator is not working, and a signal of the opposite value is transmitted as soon as the quartz oscillator is working.

11. An electronic circuit according to claim 1, characterized in that it comprises initialization means (51) which transmit the following signals:

10 a first power-on reset signal (POR1) having a specific value as long as the current supplied by said stabilized power source (32) does not reach a given value, and having the opposite value as soon as the current supplied by said stabilized power source (32) exceeds said predetermined value,

15 a second power-on reset signal (POR2) having a specific value as long as the quartz oscillator is not working, and having the opposite value as soon as the quartz oscillator is working,

and that the initialization means further comprises means (528) which combine the two power-on reset signals (POR1, POR2).

20 12. An electronic circuit according to one of the claims 9 to 11, characterized in that said initialization means (51) comprise delay means (510).

13. An electronic circuit according to claim 6, characterized in that the energy dissipation of said energy-dissipation circuit (9) can assume at least three specific values.

25 14. An electronic circuit according to claim 1, characterized by means (51) for minimizing the energy dissipation of said energy-dissipation circuit (9) when a voltage is applied to the electronic circuit.



15. An electronic circuit according to claim 1, characterized in that said oscillator (3, 4) is connected to a frequency divider (50).

16. An electronic circuit according to claim 1, characterized in that said energy-dissipation control means (5, 6, 7, 30, 31) comprise the
5 following components;

a hysteresis comparator (7) which compares the signal between said first and second inputs (G-, G+), and

an anticoincidence circuit (8) which is connected to the output of said hysteresis comparator (7) and transmits said incrementation signal (UP).

10 17. An electronic circuit according to claim 1, characterized in that said rectifier and voltage-multiplicating circuit (2) comprises at least one capacitor (10, 15, 16) which is charged via one or more passive elements when a voltage is applied to the electronic circuit, said passive element or elements being replaced by active elements (17, 18, 19) as soon as the voltage charged
15 in the capacitor or capacitors (10, 15, 16) suffices to activate the active element or elements.

18. An electronic circuit for regulating the speed of rotation of a microgenerator (1), comprising:

a first input (G+) and a second input (G-) which can be
20 connected to the microgenerator (1),

an oscillator (3, 4) supplying a reference signal of a predetermined frequency,

an energy-dissipation circuit for braking the microgenerator (1),

energy-dissipation control means (5, 6, 7, 8, 30, 31) for
25 controlling the energy dissipation of the energy-dissipation circuit (9) as a function of the reference signal and of the signal between said inputs (G-, G+),



said energy-dissipation circuit (9) having a network of elements connected in parallel, each element comprising a resistor (910 to 916) in series with a switch (900:906), the total resistance of the energy-dissipation circuit being controllable by connecting in a predetermined combination of switches
5 (900:906), and

a rectifier and voltage-multiplicating circuit (2) for rectifying and multiplying the signal between said first and second inputs,

characterized in that said switches (900 to 906) in series with said resistors (910:916) are n-channel field-effect transistors,

10 that said energy-dissipation circuit further comprises at least one p-channel field-effect transistor (920) connected to said network of elements (900:916) connected in parallel, and

that said electronic circuit further includes means (3080, 300) for controlling said p-channel field-effect transistor (920) in order to disable said p-
15 channel field-effect transistor when the electronic circuit is put into operation, so that braking of the microgenerator is blocked.

19. An electronic circuit according to the preceding claim, characterized in that said n-channel transistors are triggered by means of a voltage higher than V_{dd} , and that said p-channel field-effect transistor is
20 triggered by means of a voltage which is at least one threshold value lower than V_{ss} .

20. An electronic circuit according to claim 18, characterized in that said control circuit (20, 21) comprises a comparator (200, 210).

21. An electronic circuit according to claim 18, characterized
25 in that braking is blocked during every second cycle of the signal from the microgenerator.



22. An electronic circuit according to claim 18, characterized in that said energy-dissipation circuit (9) is connected between said inputs (G-, G+) intended for connection to the microgenerator.

23. An electronic circuit according to claim 18, characterized
5 in that said energy-dissipation circuit (9) is connected between the inputs intended for connection to said capacitor (10) charged by the microgenerator.

24. An electronic circuit according to claim 18, characterized in that said energy-dissipation control means (5, 6, 7, 30, 31) include a counter (6), the count of which is a function of the frequency difference between the
10 generator (1) and the oscillator (3, 4), the energy dissipation of the energy-dissipation circuit being a function of said count.

25. An electronic circuit according to the preceding claim, characterized in that the count of the counter (6) increases with each pulse of an incrementation signal (UP) coming from the signal between the two inputs
15 (G-, G+) and decreases with each pulse of a decrementation signal (DOWN) coming from said oscillator (3, 4).

26. An electronic circuit according to the preceding claim, characterized in that it comprises means (51, rud) for resetting said counter (6) to a predetermined value when a voltage is applied to the circuit.

27. An electronic circuit according to claim 18, characterized
20 in that it comprises initialization means (51) which transmit a signal (POR1) of a specific value as long as the current supplied by said stabilized power source (32) does not reach a given value, and a signal of the opposite value is transmitted as soon as the current supplied by said stabilized power source
25 (32) exceeds said predetermined value.

28. An electronic circuit according to claim 18, characterized in that it comprises initialization means which transmit a signal (POR2) of a specific value as long as the quartz oscillator is not working, and a signal of the opposite value is transmitted as soon as the quartz oscillator is working.



29. An electronic circuit according to claim 18, characterized in that it comprises initialization means (51) which transmit the following signals:

5 a first power-on reset signal (POR1) having a specific value as long as the current supplied by said stabilized power source (32) does not reach a given value, and having the opposite value as soon as the current supplied by said stabilized power source (32) exceeds said predetermined value,

10 a second power-on reset signal (POR2) having a specific value as long as the quartz oscillator is not working, and having the opposite value as soon as the quartz oscillator is working,

and that the initialization means further comprises means (528) which combine the two power-on reset signals (POR1, POR2).

30. An electronic circuit according to one of the claims 27 to 15 29, characterized in that said initialization means (51) comprise delay means (510).

31. An electronic circuit according to claim 24, characterized in that the energy dissipation of said energy-dissipation circuit (9) can assume at least three specific values.

20 32. An electronic circuit according to claim 18, characterized by means (51) for minimizing the energy dissipation of said energy-dissipation circuit (9) when a voltage is applied to the electronic circuit.

33. An electronic circuit according to claim 18, characterized in that said oscillator (3, 4) is connected to a frequency divider (50).

25 34. An electronic circuit according to claim 18, characterized in that said energy-dissipation control means (5, 6, 7, 30, 31) comprise the following components;



a hysteresis comparator (7) which compares the signal between said first and second inputs (G-, G+), and

an anticoincidence circuit (8) which is connected to the output of said hysteresis comparator (7) and transmits said incrementation signal (UP).

5 35. An electronic circuit according to claim 18, characterized in that said rectifier and voltage-multiplicating circuit (2) comprises at least one capacitor (10, 15, 16) which is charged via one or more passive elements when a voltage is applied to the electronic circuit, said passive element or elements being replaced by active elements (17, 18, 19) as soon as the voltage charged
10 in the capacitor or capacitors (10, 15, 16) suffices to activate the active element or elements.

36. An electronic circuit for regulating the speed of rotation of a microgenerator, comprising:

 a first input (G+) and a second input (G-) which can be
15 connected to the microgenerator (1),

 a rectifier and voltage-multiplicating circuit (2) for rectifying and multiplying the signal between said first and

 second inputs, the rectifier and voltage-multiplicating circuit comprising at least one switch (17) connected between said first input (G-) and
20 a reference point in this electronic circuit, and a comparator (20) for controlling the first switch,

 an oscillator (3, 4) supplying a reference signal of a predetermined frequency,

 an energy-dissipation circuit for braking the microgenerator (1),
25 energy-dissipation control means (5, 6, 7, 8, 30, 31) for controlling the energy dissipation of the energy-dissipation circuit (9) as a function of the reference signal and of the signal between said inputs (G-, G+), and



a stabilized power source (32) which feeds in particular said comparator (20) in the rectifier and voltage-transformer circuit (2),

characterized in that said stabilized power source (32) comprises an initialization transistor (320) permitting current to be fed into or
5 withdrawn from said power source.

37. An electronic circuit according to claim 36, characterized in that said initialization transistor (320) is connected to said first input (G-) and the voltage reference point in such a way that current is supplied or received by said power source as long as said first input (G-) exhibits a potential difference
10 relative to said reference point.

38. An electronic circuit according to claim 36, characterized in that said reference point is the ground, and said initialization transistor (320) is an n-channel field-effect transistor, the gate of which is grounded, and the source of which is connected to said first input (G-).

15 39. An electronic circuit according to the preceding claim, characterized in that said control circuit (20, 21) comprises a comparator (200, 210).

40. An electronic circuit according to claim 36, characterized in that braking is blocked during every other cycle of the signal from the
20 microgenerator.

41. An electronic circuit according to claim 36, characterized by level shifters (301 to 305) which increase the voltage of the signals (Q1-Q5) for controlling said p-channel field-effect transistors (900-906).

42. An electronic circuit according to claim 36, characterized
25 in that said energy-dissipation circuit (9) is connected between said inputs (G-, G+) intended for connection to the microgenerator.



43. An electronic circuit according to claim 36, characterized in that said energy-dissipation circuit (9) is connected between the inputs intended for connection to said capacitor (10) charged by the microgenerator.

5 44. An electronic circuit according to claim 36, characterized in that said energy-dissipation control means (5, 6, 7, 30, 31) have a counter (6), the count of which depends upon the frequency difference between the microgenerator (1) and the oscillator (3, 4), the energy dissipation of the energy-dissipation circuit being a function of said count.

10 45. An electronic circuit according to the preceding claim, characterized in that the count of the counter (6) increases with each pulse of an incrementation signal (UP) coming from the signal between the two inputs (G-, G+) and decreases with each pulse of a decrementation signal (DOWN) coming from said oscillator (3, 4).

15 46. An electronic circuit according to the preceding claim, characterized in that it comprises means (51, rud) for resetting said counter (6) to a predetermined value when a voltage is applied to the circuit.

20 47. An electronic circuit according to claim 36, characterized in that it comprises initialization means (51) which transmit a signal (POR1) of a specific value as long as the current supplied by said stabilized power source (32) does not reach a given value, and a signal of the opposite value is transmitted as soon as the current supplied by said stabilized power source (32) exceeds said predetermined value.

25 48. An electronic circuit according to claim 36, characterized in that it comprises initialization means which transmit a signal (POR2) of a specific value as long as the quartz oscillator is not working, and a signal of the opposite value is transmitted as soon as the quartz oscillator is working.

49. An electronic circuit according to claim 36, characterized in that it comprises initialization means (51) which transmit the following signals:



a first power-on reset signal (POR1) having a specific value as long as the current supplied by said stabilized power source (32) does not reach a given value, and having the opposite value as soon as the current supplied by said stabilized power source (32) exceeds said predetermined
5 value,

a second power-on reset signal (POR2) having a specific value as long as the quartz oscillator is not working, and having the opposite value as soon as the quartz oscillator is working,

and that the initialization means further comprises means (528)
10 which combine the two power-on reset signals (POR1, POR2).

50. An electronic circuit according to one of the claims 47 to 49, characterized in that said initialization means (51) comprise delay means (510).

51. An electronic circuit according to claim 44, characterized
15 in that the energy dissipation of said energy-dissipation circuit (9) can assume at least three specific values.

52. An electronic circuit according to claim 36, characterized by means (51) for minimizing the energy dissipation of said energy-dissipation circuit (9) when a voltage is applied to the electronic circuit.

20 53. An electronic circuit according to claim 36, characterized in that said oscillator (3, 4) is connected to a frequency divider (50).

54. An electronic circuit according to claim 36, characterized in that said energy-dissipation control means (5, 6, 7, 30, 31) comprise the following components;

25 a hysteresis comparator (7) which compares the signal between said first and second inputs (G-, G+), and



an anticoincidence circuit (8) which is connected to the output of said hysteresis comparator (7) and transmits said incrementation signal (UP).

55. An electronic circuit according to claim 36, characterized in that said rectifier and voltage-multiplicating circuit (2) comprises at least one
5 capacitor (10, 15, 16) which is charged via one or more passive elements when a voltage is applied to the electronic circuit, said passive element or elements being replaced by active elements (17, 18, 19) as soon as the voltage charged in the capacitor or capacitors (10, 15, 16) suffices to activate the active element or elements.

10 56. A watch movement containing an electronic circuit for regulating the speed of rotation of a microgenerator (1),

comprising:

a first input (G+) and a second input (G-) which can be connected to the microgenerator (1),

15 an oscillator (3, 4) supplying a reference signal of a predetermined frequency,

an energy-dissipation circuit for braking the microgenerator (1),

energy-dissipation control means (5, 6, 7, 8, 30, 31) for
controlling the energy dissipation of the energy-dissipation circuit (9) as a
20 function of the reference signal and of the signal between said inputs (G-, G+),

a rectifier and voltage-multiplicating circuit (2) for rectifying and multiplying the signal between said first and

second inputs, the rectifier and voltage-transformer circuit comprising at least one capacitor (C1; C2; C3) which can be charged by said
25 microgenerator via at least one switch (17, 18, 19), and



at least one control circuit (20; 21) of said switch or switches
(17, 18, 19),

said control circuit (20; 21) comprising at least one storage
means (201; 211) which in a first phase with blocked switch stores at least one
5 control signal to be applied to said switches (17, 18, 19), and in a second
phase said switches (17, 18, 19) being triggered by means of said control
signal (ser/par).