

TRANSFER DATA SHAPING APPARATUS

Detailed Description of the Invention

Technical Field of the Invention

The present invention relates to a transfer data shaping apparatus.

Prior Art

Fig. 5 is a block diagram for representing the prior art. A comparing means 51 compares transfer data "a" with a preset reference level "R" to binary-quantize this transfer data "a". A sampling means 52 samples the binary-quantized data "b" sequentially outputted from the comparing means 51 in response to a sampling clock "c".

An averaging means 53 adds a predetermined number of data "d" sequentially outputted from the sampling means 52 to each other every sampling clock "c" to average the added data, and thus may function as a low-pass filter (LPF) calculating means. Another comparing means 54 sequentially comparing the added data "e" sequentially outputted from the averaging means 53 with a reference value X to thereby output data "f" based upon this comparison result.

In such a case that a noise component is contained in the transfer data "a", the following problem will occur only when this transfer data "a" is simply binary-quantized by the comparing means 51. That is, only when the transfer data "a" is simply binary-quantized, such a phenomenon will occur that the logic value "1" and the logic value "0" are quickly, repeatedly changed adjacent to a transition point between the logic value "1" and the logic value "0", so that the condition of the output "b" becomes

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unstable. Accordingly, as indicated in Fig. 5, the LPF process is performed by the average means 53 so as to reduce occurrences of the above-described phenomenon.

Problems to be Solved by the Invention

However, even when the LPF process is carried out by employing the arrangement as shown in Fig. 5, if the noise component is increased, then the above-described unstable factor cannot be completely eliminated. Therefore, there is a problem that it is rather difficult to correctly reproduce the transfer data.

An object of the present invention is to provide a transfer data shaping apparatus capable of avoiding that output conditions on a transfer data near a transition point would become unstable, and further capable of correctly reproducing the transfer data even when a noise component is increased.

Summary of the Invention

In accordance with the present invention, a so-called "hysteresis characteristic" is given to digital data sequentially outputted from an averaging means. By giving the hysteresis characteristic, it is possible to prevent output conditions on a transfer data near a transition point for binary quantization from becoming unstable.

That is, a transfer data shaping apparatus, according to the present invention, is comprised of a comparing means for comparing digital data sequentially outputted from the averaging means with a first reference value and a second reference value smaller than said first reference value to output one logic value since said digital data becomes larger than said first reference value until said digital data becomes smaller than said second reference value, and also to output the other logic value since said digital data becomes smaller than said second reference value until said digital data becomes larger than said first reference value.

Embodiment

Fig. 1 is a schematic block diagram for showing a transfer data shaping apparatus, and Fig. 2 is a block diagram for representing a concrete arrangement of the transfer data shaping apparatus of Fig. 1.

A comparing means 1 compares transfer data "a" (for example, demodulated baseband waveform data) with a preset reference level "R" to binary-quantize the transfer data. When the transfer data "a" is larger than the reference level "R", the comparing means 1 outputs a logic value "1", whereas when the transfer data "a" is smaller than the reference level "R", the comparing means 1 outputs another logic value "0".

A sampling means 2 samples the binary-quantized data "b" sequentially outputted from the comparing means 1 in response to a sampling clock "c" (sampling frequency is selected to be "m" times higher than Baud rate of transfer data "a"), and then output digital data "d". An averaging means 3 sequentially averages a predetermined number "n" ($n \leq m$, $n=7$ in this example) of digital data "d" sequentially outputted from the sampling means 2 every sampling clock "c" to thereby output digital data "e", and may function as a low-pass filter (LPF) calculating means. As indicated in Fig. 2, these sampling means 2 and averaging means 3 are arranged by seven D type flip-flops 21 to 27 functioning as a shift register, and an adder 28 for simply adding the output values from the respective D type flip-flops 21 to 27 (namely, adding the respective output values without weighing). As a consequence, an added value "S" obtained from the adder 28 corresponds to averaged data "e".

Another comparing means 4 sequentially compares the digital data "e", namely the

added value "S" sequentially outputted from the averaging means 3 with a reference value A and another reference value B ($A > B$) every sampling clock "c", and thus outputs digital data "f" produced by shaping the digital data "e" by using a so-called "hysteresis characteristic". As indicated in Fig. 2, this comparing means 4 is arranged by a comparator 41 for outputting a logic value "1" when the added value "S" is larger than, or equal to the reference value "A" ($S \geq A$), another comparator 42 for outputting a logic value "1" when the added value "S" is smaller than, or equal to the reference value "B" ($S \leq B$), gates 43 and 44, and also a D type flip-flop 45.

Next, referring to a timing chart shown in Fig. 3, operations of the transfer data shaping apparatus indicated in Fig. 1 and Fig. 2 will now be explained.

First, in order to binary-quantize the transfer data "a" containing the noise component, the transfer data "a" is compared with a preset reference level "R" in the comparing means 1. When the transfer data "a" is larger than the reference level "R", the logic value "1" is outputted from the comparing means 1. When the transfer data "a" is smaller than the reference level "R", the logic value "0" is outputted from the comparing means 1. Thus, the binary-quantized data "b" is sequentially sampled in response to a sampling clock "c" having a sampling frequency "m" times higher than the Baud rate of the transfer data "a". In other words, a series of transfer data "a" are latched by the D type flip-flop 21, and also are sequentially shifted by the D type flip-flops 22 to 27. Each of data "d" outputted from the D type flip-flops 21 to 27 is added to each other in the adder 28. Then, the added value "S" (data "e") is outputted from the adder 28. That is, the data outputted from the D type flip-flops 21 to 27 for the seven sampling clocks are simple-averaged.

The added values "S" sequentially outputted from the adder 28 are successively

compared with the reference value "A" and the reference value "B" every sampling clock "c" in the comparing means 4 having the hysteresis characteristic. A concrete operation performed in this comparing means 4 will now be explained with reference to a timing chart shown in Fig. 3 (especially, (e) and (f)). First, since $S > A$, the logic value outputted from the comparing circuit 41 becomes "1", the logic value outputted from the comparing circuit 42 becomes "0", and the output "f" from the D type flip-flop becomes "1". Subsequently, since $A > S > B$, although the logic value outputted from the comparing circuit 41 becomes "0", the output "f" from the D type flip-flop is still maintained at the logic value "1". Next, when $S < B$, and the logic value of the comparing circuit 42 becomes "1", the output "f" of the D type flip-flop is inverted into "0". Thereafter, since $A > S > B$, although the logic value from the comparing circuit 42 becomes "0", the output "f" of the D type flip-flop is still kept at the logic value of "0". Next, when $S > A$ and the logic value outputted from the comparing circuit 41 becomes 1, the output of the D type flip-flop is inverted into "1". As described above, in the comparing means 4, while the added value "S" is present between the reference value "A" and the reference value "B", namely the added value "S" is defined by $A > S > B$, the output "f" of the D type flip-flop is maintained under the previous output state. That is, the comparing means 4 owns the hysteresis characteristic. Therefore, since the comparing means 4 owns the hysteresis characteristic, it is possible to avoid such a fact that the output condition of the comparing means 4 becomes unstable on a transfer data "a" near the transition point.

Fig. 4 is a block diagram for showing another example of the sampling means 2 and the averaging means 3 indicated in Fig. 2.

In the example shown in Fig. 2, the simple adding process (namely, adding

process of respective output values without weighing these output values) has been performed by directly inputting the respective output signals derived from the D type flip-flops 21 to 27 into the adder 28. In the example shown in Fig. 4, the respective output signals from the D type flip-flops 21 to 27 are entered via multipliers 31 to 37 to the adder 28, so that the respective output values of the D type flip-flops 21 to 27 are weighted to perform the weighted adding process. Concretely speaking, after the respective output values from the D type flip-flops 21 to 27 are multiplied by 1, 2, 2, 3, 2, 2, and 1 by way of the multipliers 31 to 37, respectively, these multiplied values are added to each other by the adder 28. In other words, the data outputted from the D type flip-flops 21 to 27 for seven sampling clocks are weighted-averaged. In this manner, since the respective output values derived from the D type flip-flops 21 to 27 are weighted-averaged, the characteristic as the low-pass filter (LPF) can be improved, and thus the noise eliminating characteristic can be improved.

In accordance with the transfer data shaping apparatus of the present invention, it is possible to avoid such a fact that the output condition of the comparing means becomes unstable on a transfer data near the transition point for binary quantization. As a consequence, even when the noise component contained in the transfer data is large, this transfer data can be correctly reproduced.

Brief Description of the Drawings

Fig. 1 is a schematic block diagram for showing a transfer data shaping apparatus according to an embodiment of the present invention.

Fig. 2 is a block diagram for indicating a concrete circuit arrangement of the transfer data shaping apparatus of Fig. 1.

Fig. 3 is a timing chart for describing operations of the apparatus shown in Fig. 1 and Fig. 2.

Fig. 4 is a block diagram for representing another example of the sampling means 2 and the averaging means 3.

Fig. 5 is a schematic block diagram for showing the conventional transfer data shaping apparatus.

What is claimed is:

1. A transfer data shaping apparatus comprising:

first comparing means for comparing transfer data with a reference level to output first digital data binary-quantized, depending upon a fact as to whether or not said transfer data is higher than said reference level;

sampling means for sampling said first digital data sequentially outputted from said first comparing means by a predetermined sampling clock to thereby output second digital data;

averaging means for sequentially averaging a predetermined number of said second digital data sequentially outputted from said sampling means every one sampling clock to thereby output third digital data; and

second comparing means for comparing said third digital data sequentially outputted from said averaging means with a first reference value and a second reference value smaller than said first reference value to output one logic value since said third digital data becomes larger than said first reference value until said third digital data becomes smaller than said second reference value, and also to output the other logic value since said third digital data becomes smaller than said second reference value until said third digital data becomes larger than said first reference value.

2. A transfer data shaping apparatus as claimed in claim 1 wherein:

the averaging process performed in said averaging means is a simple averaging process.

3. A transfer data shaping apparatus as claimed in claim 2 wherein:

the simple averaging process performed in said averaging means is a simple adding process.



4. A transfer data shaping apparatus as claimed in claim 1 wherein:

the averaging process performed in said averaging means is a simple weighted averaging process.

5. A transfer data shaping apparatus as claimed in claim 4 wherein:

the weighted averaging process performed in said averaging means is a weighted adding process.



* C L M S *

TRANSFER DATA SHAPING APPARATUS**ABSTRACT**

A transfer data shaping apparatus capable of correctly reproducing transfer data is provided as followings.

A transfer data shaping apparatus is comprised of: a comparing means 1 for comparing transfer data "a" with a reference level R to output data "b" binary-quantized, depending upon a fact as to whether or not said transfer data "a" is higher than said reference level R; a sampling means 2 for sampling the data "b" by a predetermined sampling clock "c" to thereby output data "d"; an averaging means 3 for sequentially averaging a predetermined number of the digital data "d" every one sampling clock to thereby output data "e"; and another comparing means 4 for comparing the data "e" with a reference value A and a reference value B to output one logic value since the data "e" becomes larger than said reference value A until the data "e" becomes smaller than said reference value B, and also to output the other logic value since the data "e" becomes smaller than said reference value B until the data "e" becomes larger than said reference value A.

Figure 1

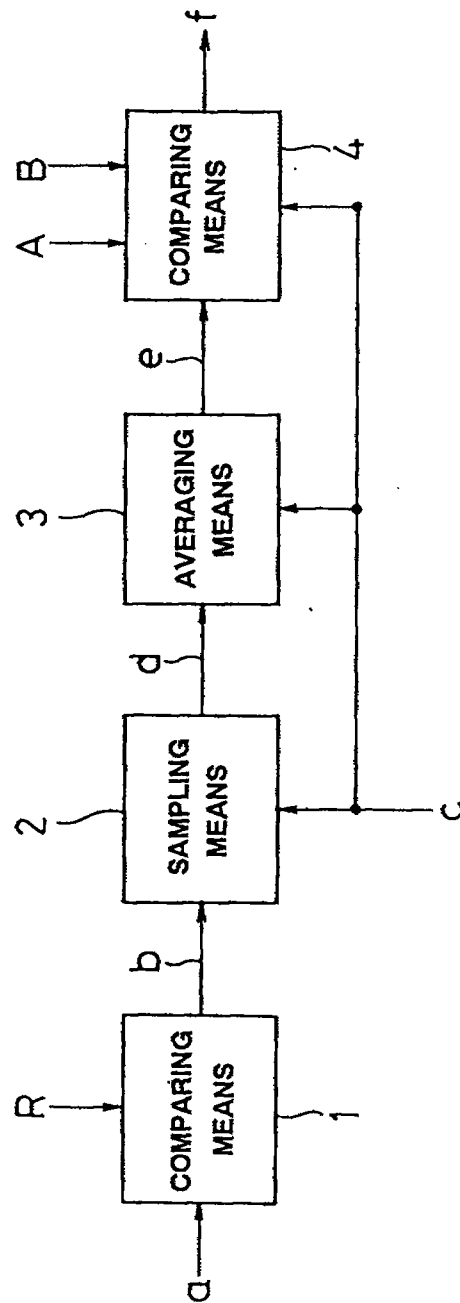


FIG. 1

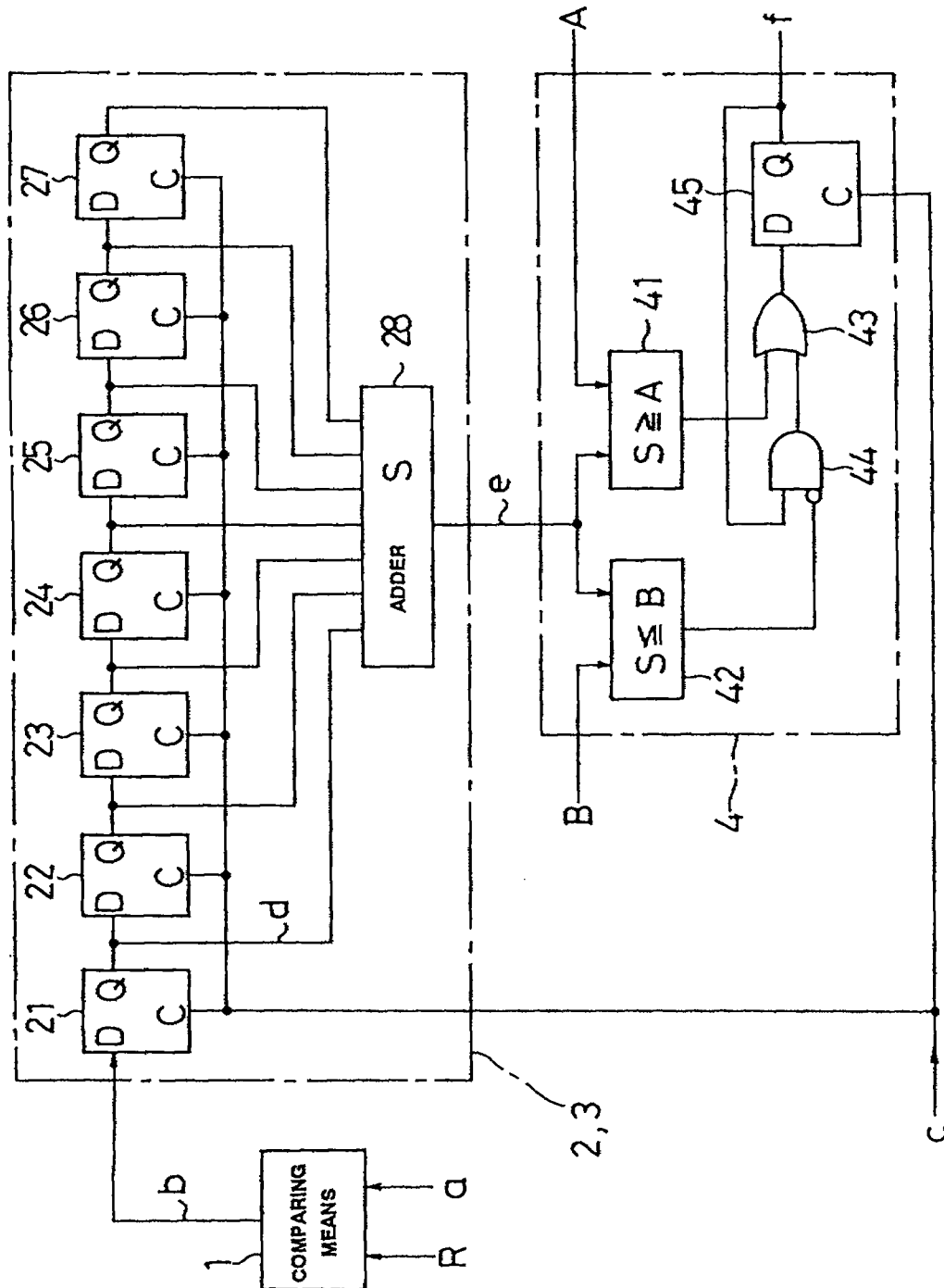


FIG. 2

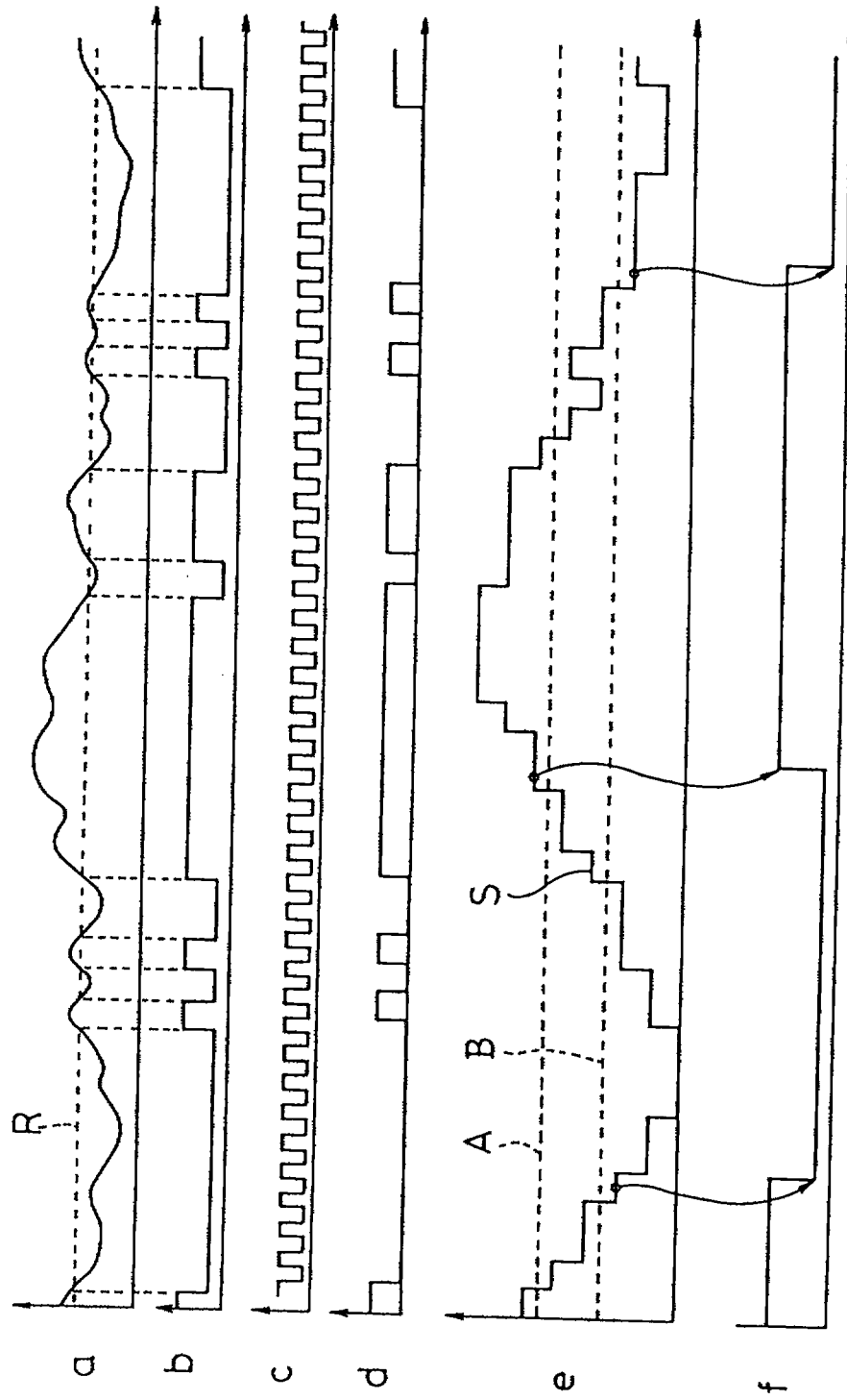


FIG. 3

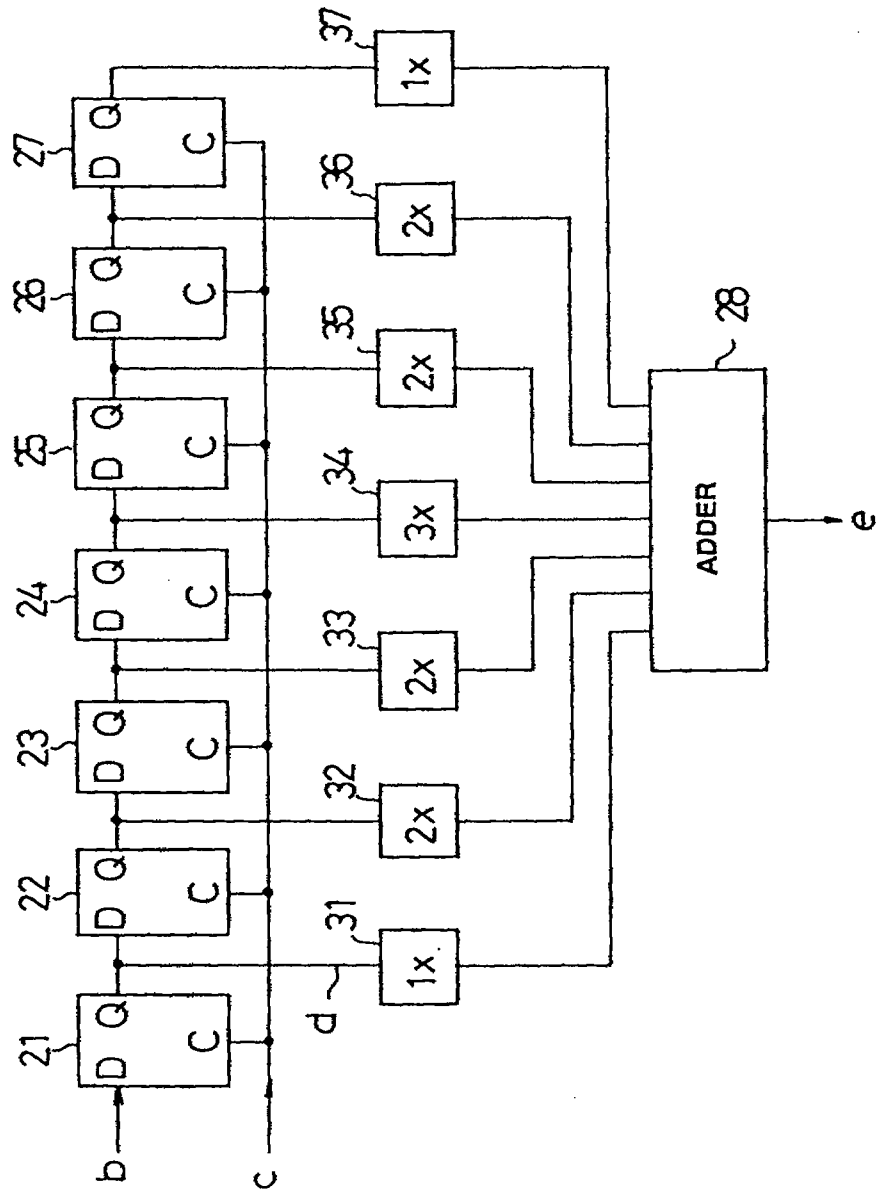


FIG. 4

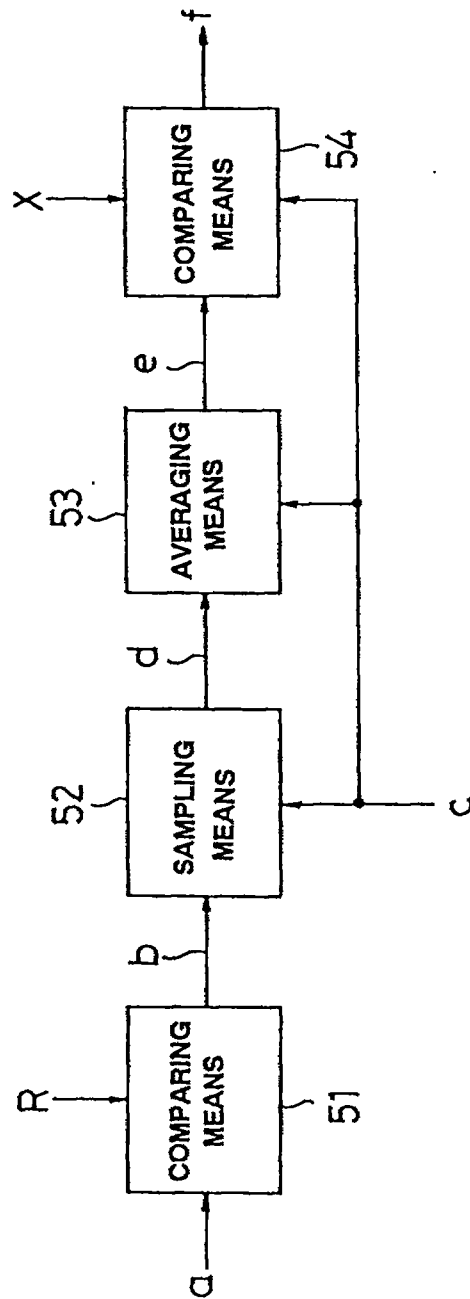


FIG. 5