12. The system of claim 10, wherein a number of row and a number of columns of memory units of the EPROM array of each of the number of EPROM banks is determined by the number of clock cycles associated with a corresponding shift register.

13. A method for three-dimensional addressing of an erasable programmable read only memory (EPROM) memory unit of an integrated print head, comprising:

receiving a number of input signals at a number of shift registers, wherein the number of input signals include a select signal to precharge and advance a shift register of the number of shift registers and a data signal;

generating a row select data signal at a first shift register of the number of shift registers specifying a row portion of a three-dimensional EPROM address;

generating a column select data signal at a second shift register of the number of shift registers specifying a column portion of the three-dimensional EPROM address;

generating a bank select signal at a shift register of the number of shift registers specifying an EPROM bank, of a number of EPROM banks, associated with the row select data signal and the column select data signal; and

addressing an individual EPROM memory unit in three dimensions based on the row select data signal, the column select data signal, and the bank select signal.

14. The method of claim 13, wherein each shift register of the number of shift registers is connected to each EPROM bank of the number of EPROM banks.

15. The method of claim 13, wherein the method includes generating one three-dimensional EPROM address with eight cycles of the number of shift registers.