

Description**METHOD AND APPARATUS FOR COMPILING ONE CIRCUIT IN A SEQUENCE OF CIRCUITS
WITHIN A PROGRAMMABLE GATE ARRAY**5 Technical Field

The present invention relates to methods and apparatus for communicating information, and more particularly, to methods and apparatus for adapting to changing communications services.

10 Background of the Invention

Personal communications is on the brink of an unprecedented expansion of its capabilities. With the advent of advanced personal communications services, such as cellular telephone and low earth orbit (LEO) satellite services, this expansion of capabilities also benefits mobile users. Not only does the expansion of capabilities benefit voice communications, but it also benefits data communications, such as might be used with portable computers and other personal data communicators.

A major difficulty with the expansion of services is that a wide variety of different voice and data communications protocols have been proposed. It can be expected that this variety will increase, both world-wide and within a local area. For example, each communications service has its own technical, geographic and feature sets. Technical parameters include frequency(ies), modulation and protocol used, among others. Geographic parameters are dictated by the particular locale. Feature sets describe whether the service is voice, paging, data, or some combination of these.

As a consequence, a given communications device will become less useful as its user attempts to use it in areas that use incompatible services. For example, as people who rely on mobile communications move through a day, they can move in and out of different coverage areas and their communications needs will change constantly. Further, even within a local area, a given communications device will gradually become less useful as its built-in capabilities are rendered out-of-date by newer services.

It is clearly undesirable for the individual to have to carry a different communication device for each communication service. Also, few individuals really want to know the details and peculiarities of each of the available communication service. Most individuals would much rather have seamless service that is simple, convenient and cost-effective for the user.

Therefore, it is advantageous to have a single personal communications device that will reconfigure itself to be compatible with whatever communications service is desired or needed. This is difficult with today's conventional technology.

Brief Description of the Drawings

Figure 1 is a schematic representation of the interface structure of an embodiment of the present invention.

Figure 2 is a schematic representation of the physical structure of an embodiment of the present invention.

Figure 3 is a block diagram representation of an embodiment of the present invention, when used as a terminal emulator.

Figure 4 is a block diagram representation of an embodiment of the present invention, when used as a facsimile transmitter/receiver emulator.

Figure 5 is a block diagram representation of an embodiment of the present invention, when used as a communications device emulator.

Figure 6 is a block diagram representation of an embodiment of the present invention, when used as a wireless local area network emulator.

Figure 7 is a block diagram representation of the operation of the present invention.

Figure 8 is a block diagram representation of the operation of the present invention in an embodiment that integrates several digital personal communication services.

Figure 9 is a flow chart representation of the call processing operations of the present invention.

Figure 10 is a timing diagram representation of the processing operations of a land-initiated call in accordance with the present invention.

Figure 11 is a timing diagram representation of the processing operations of a portable-initiated call in accordance with the present invention.

Figure 12 is a schematic representation of the functional structure of an embodiment of the present invention.

Figure 13 is a schematic representation of the function of software in the present invention.

Figure 14 is a block diagram representation of the software architecture of the present invention.

Figure 15 is a tabular representation of the dynamic configuration modes of the present invention.

Figure 16 is a schematic representation of the dynamic configuration modes of the present invention.

Figure 17 is a schematic representation of the run-time reconfigurable architecture of the present invention.

Figure 18 is a schematic representation of a symmetrical array structure for use in the present invention.

Figure 19 is a schematic representation of a busing network symmetrical structure for use in the present invention.

Figure 20 is a schematic diagram of a cell structure for use in the present invention.

Figure 21 is a flow chart diagram of the stand-alone design environment of a field programmable gate array for use in the present invention.

Figure 22 is a flow chart diagram of the design environment of a field programmable gate array for use in the present invention.

Figure 23 is a schematic diagram of an analog front end for use in the present invention.

Figure 24 is a schematic diagram of the digital hardware for use in a preferred embodiment of the present invention.

Figures 1-24 present graphic descriptions of the preferred embodiments of the invention which, when combined with the following description of the preferred embodiments will be understood by those skilled in the communication electronics and microelectronics arts.

Description of the Preferred Embodiments of the Invention

Figure 1 is a schematic representation of the interface structure of an embodiment of the present invention. The interface device 50 includes an interface 52 (such as a PCMCIA interface), a protocol 54, an intermediate frequency (IF) stage 56, and a connector 58 (such as an analog pigtail). The interface 52 receives and transmits signals between the interface device 50 and an external device (not shown), such as a computer with a PCMCIA slot. The protocol 54 interprets signals from the interface 52 and transmits the interpretation to the IF stage 56. The protocol 54 also receives signals from the IF stage 56 and transforms them, in accordance with an appropriate protocol, to signals for transmittal through the interface 52. The connector 58 communicates signals with the IF stage 56 for transmittal to and receipt from an external communication service. The external communication service can be connected in either a wired or wireless manner, as will be known by those skilled in the communications and electronics arts.

Figure 2 is a schematic representation of the physical structure of an embodiment of the present invention. In Figure 2, the interface device 50 is shown to include a configurable device 70 (such as a field programmable gate array - FPGA or other sea of gates device), a memory 72 (such as a flash random access memory - RAM), a hard drive 74, and the connector 58. The configurable device 70 connects to an external device (not shown), such as a computer, and processes signals for transmittal to and receipt from the memory 72. The hard drive 74 communicates with the memory 72 and transmits signals to and from the connector 58 for transmittal to and receipt from an external communication service. The external communication service can be connected in either a wired or wireless manner, as will be known by those skilled in the communications and electronics arts.

Figure 3 is a block diagram representation of an embodiment of the present invention, when used as a terminal emulator. The terminal emulator device 90 includes the interface 52, which is connected to a configurable circuit 92, signal processing circuits 94, a first memory 96, and a second memory 98. The signal processing circuits 94 communicate with the configurable

circuit 92, the first memory 96, and the second memory 98. The signal processing circuits 94 also communicate with an external communication service. The external communication service can be connected in either a wired or wireless manner, as will be known by those skilled in the communications and electronics arts.

The configurable circuit 92 is arranged to respond to signals from the interface 52, the signal processing circuits 94, the flash memory 96, and the RAM 98 to cause the proper transmittal of communications signals between the interface 52 and the signal processing circuits 94.

Figure 4 is a block diagram representation of an embodiment of the present invention, when used as a facsimile transmitter/receiver emulator. The facsimile transmitter/receiver emulator 110 includes the interface 52, which is connected to the configurable circuit 92. The configurable circuit 92 is also connected to a first special purpose facsimile circuit 112, a flash memory 114, a RAM 116, a second special purpose facsimile circuit 118, and signal conditioning circuitry 120. The signal conditioning circuitry 120 is adapted to communicate to a compatible device (not shown), such as a telephone or external speaker.

The configurable circuit 92 is arranged to respond to signals from the interface 52, the first and second special purpose facsimile circuits 112 and 118, the flash memory 114, and the RAM 116 to cause the proper transmittal of facsimile signals between the interface 52 and the signals conditioning circuitry 120.

Figure 5 is a block diagram representation of an embodiment of the present invention, when used as a communications device emulator. The communications device emulator 130 includes the interface 52, the configurable circuit 92, an A/D converter 132, special signal conditioning circuitry 134, a flash memory 136, a RAM packet memory 138, and a RAM memory 140. The communications device emulator 130 typically facilitates communications via analog signals, although it can also facilitate communications via digital signals. The signals transmitted through the interface 52 are received and processed by the configurable circuit 92. The configurable circuit 92 communicates with the special signal conditioning circuitry 134, the flash memory 136,

the RAM packet memory 138, and the RAM memory 140. The A/D converter 132 communicates with the flash memory 136, the RAM packet memory 138, and the RAM memory 140. The special signal conditioning circuitry 134 is adapted to communicate to a compatible device (not shown), such as a computer or terminal.

The configurable circuit 92 is arranged to respond to signals from the interface 52, the configurable circuit 92, the special signal conditioning circuitry 134, the flash memory 136, the RAM packet memory 138, and the RAM memory 140 to cause the proper transmittal of facsimile signals between the interface 52 and the special signal conditioning circuitry 134.

Figure 6 is a block diagram representation of an embodiment of the present invention, when used as a wireless local area network emulator. The wireless local area network (LAN) emulator 150 includes the interface 52, the configurable circuit 92, an address conversion circuit 152, an interface circuit 154, a flash memory 156 and a RAM 158. The interface circuit 154 includes a signal processing circuit 160 and a second configurable circuit 162. The configurable circuit 92 communicates with the signal processing circuit 160, the flash memory 156 and the RAM 158. The address conversion circuit 152 communicates with the signal processing circuit 160, the flash memory 156 and the RAM 158. The signals received by the signal processing circuit 160 from the configurable circuit 92 and the address conversion circuit 152 are transformed to a form for processing by the second configurable circuit 162, which can be configured as necessary in accordance with procedures known by those skilled in the relevant arts. The signals resulting from the processing operations of the second configurable circuit 162 are transmitted to a radio communication device such as a baseband transceiver. Similarly, signals from the radio communication device are received by the second configurable circuit 162 and converted to a form compatible with the signal processing circuit 160. The signal processing circuit 160 then produces signals for receipt by the configurable circuit 92 and/or the address conversion circuit 152 which then process and send the signals on to the interface 52.

Figure 7 is a block diagram representation of the operation of the present invention, showing the functions performed by the hardware of the foregoing descriptions.

Figure 8 is a block diagram representation of the operation of the present invention in an embodiment that integrates several digital personal communication services. The personal communicator 170 includes an antenna 172 connected to an RF power amplifier 174. The personal communicator 170 also includes an RF small signal circuit 176, a filter 178 and an IF stage 180. The RF small signal circuit 176 is connected to the RF power amplifier 174. Signals produced by the small signal circuit 176 are passed to the filter 178 and then to the IF stage 180. As shown in Figure 8, the function of these portions of the personal communicator is to serve as a combined voice and RF A/D and D/A device, as well as a homodyne RF transceiver.

The output of the IF stage 180 is passed to a voice A/D and D/A circuit 182. The circuit 182 performs appropriate analog-to-digital and digital-to-analog operations and passes the result on to an integrated baseband voice data and image circuit 184. The circuit 184 includes a microcontroller 186, a modem equalizer 188, a channel coder 190 and a voice coder 192. The microcontroller 186 is connected to the circuit 182 and signals produced by the microcontroller 186 is connected to the modem equalizer 188. The signals produced by the modem equalizer 188 are then passed on to the channel coder 190 which produces signals that are passed on to the voice coder 192. The circuit 184 accordingly serves to convert signals from the circuit 182 to forms appropriate for uses with a speaker 194 and a multimedia terminal 196.

It would also be clear to those skilled in the relevant arts that signals from the speaker 194 and the multimedia terminal 196 can be converted by the personal communicator 170 to a form by transmittal by the antenna 172 to a remote service or user.

Figure 9 is a flow chart representation of the call processing operations of the present invention as would be understood by those skilled in the communications arts. After DC Power Start-up task step (block 500), the next step is to initialize the communicator 170 (block 502) by a dedicated Channel Scan task step. If no valid message is received, the

task returns to the Power Start-up task step (block 500). On the other hand, if a valid message is received, the task proceeds to select a Paging Channel task step (block 504). If not valid message is received the task returns to the Power Start-up task step (block 500). If registration is indicated, the task proceeds to an Autonomous Registration task step (block 508), which will be described subsequently. However, if a valid message is received in the Paging Channel Selection task step (block 504), the task proceeds to an Idle task step (block 506).

In the Idle task step (block 506), there are several options. If 1) no valid message is received, 2) a rescan timer times out after 300 seconds, or 3) a rescan message is received, the task returns to the Power Start-up task step (block 500). If registration is indicated, the task proceeds to the Autonomous Registration task step (block 508). If a call initiate is indicated, the task proceeds to an Origination task step (block 510), which will also be described subsequently. If an order message is received, the task moves to an Order Response task step (block 512), which will also be described subsequently. If a page message is received and a page match occurs, the task moves to a Paging Response task step (block 514), which will also be described subsequently. If an expectant event occurs, the task stays at the Idle task step (block 506).

The Autonomous Registration task step (block 508) involves an access channel scan. If a call initiate is indicated, the task proceeds to the Origination task step (block 510). Otherwise, regardless of whether a valid message is received, the task moves to a Serving System Determination task step (block 516), which will be described subsequently.

If the task is in the Origination task step (block 510), and a valid message is not received, the task moves to the Serving System Determination task step (block 516). On the other hand, if a valid message is received, the task moves to a Conversation task step (block 518), which will also be described subsequently.

From the Order Response task step (block 512), the task proceeds to the Serving System Determination task step (block 516), regardless of whether a valid message is received. From the Paging Response task step (block 514), if no valid message

is received, the task moves to the Serving System Determination task step (block 516). However, if a valid message is received, the task moves to a Waiting for Order task step (block 520).

There are four possible states to reach from the

5 Conversation task step (block 518). If a fade timer times out after 5 seconds, the task then moves to a Transmitter Deactivation task step (block 522). If a release order is received or the conversation is terminated by depressing the END key of the communicator 170, the task moves to a Release Task

10 step (block 524), which will be described subsequently. If either an alert or a maintenance order is received, the task proceeds to a Waiting for Answer task step (block 526). If there is no order or action received, the task returns to the Conversation task step (block 518).

15 From the Waiting for Answer task step (block 526), the task returns to the Conversation task step (block 518) if a conversation enable signal is received by depressing the SEND key of the communicator 170. If a stop alert order is received, the task proceeds to the Waiting for Order task step (block

20 520). If a release order is received, the task moves to the Release task step (block 524). Finally, if either the 5 second fade timer time-out or the 65 second alert timer time-out occurs, the task goes to the Transmitter Deactivation task step (block 522).

25 From the Waiting for Order task step (block 520), the task moves to the Waiting for Answer task step (block 526) if an alert or maintenance order is received. However, if a release order is received, the task proceeds to the Release Task step (block 524). Finally, if the 65 second alert timer time-out or a

30 conversation is terminated by depressing the END key of the communicator 170, the task goes to the Transmitter Deactivation task step (block 522).

From the Release Task step (block 524), the task moves to the Transmitter Deactivation task step (block 522), and from the

35 Transmitter Deactivation task step (block 522), the task proceeds to the Serving System Determination task step (block 516). From the Serving System Determination task step (block 516), the task goes to the Initialization task step (block 502) if the serving system state is not set to NAM. On the other

hand, the task goes to the Paging Channel Selection task step (block 504) if the serving system state is set to NAM.

Figure 10 is a timing diagram representation of the processing operations of a land-initiated call in accordance with the present invention, and Figure 11 is a timing diagram representation of the processing operations of a portable-initiated call in accordance with the present invention. Those skilled in the communications arts will understand that these timing diagrams respectively graphically describe the sequences of transmitted signals needed to process telephone calls initiated from a land base and from a portable user.

As shown in Figure 10, in the case of a land-initiated call, the system first uses all signaling channels to send signals (duration 26 ms) from the bases to the portable units, with an indication to reply on a channel zero. Next, using the appropriate area signaling channel, the portable replies to the base, sending a ready status indication. Following this, again using the area signaling channel, the appropriate base sends a signal to the portable, with a request to switch to voice channel 12. Then, on voice channel 12, the portable replies to the base, indicating the execution of the command. Using the voice channel, the base then sends a ring signal to the portable and, in response, the portable send an off-hook signal to the base, using the voice channel.

In Figure 11, the case of a portable-initiated call is described. Using a portable to base signaling channel, the portable first sends its address and a request channel assignment order. Next, using the assigned channel, the base signals to the portable, giving it its channel assignment. The portable then signals the base on the assigned channel, acknowledging the channel assignment and requesting a dial tone. In response to the request, the base sends the dial tone signal to the portable, using the assigned channel.

Figure 12 is a schematic representation of the functional structure of an embodiment of the present invention. The communications device 200 includes an interface card 202 and an analog pigtail 204. The interface card 202 can be a PCMCIA type II card, for example. The interface card 202 includes a PCMCIA connector 206 for connection to a host system 208. The interface

card 202 also includes a protocol engine 210, a dynamically programmable intermediate modulation stage 212 and a memory portion 214. The protocol engine 210 and the intermediate modulation stage 212 are connected to the PCMCIA connector 206.

5 The memory portion 214, which can include a hard drive, static RAM and flash RAM, communicates with both the protocol engine 210 and the intermediate modulation stage 212.

The interface card 202 is connected to the analog pigtail 204, which provides various other means for communicating with a user, such as an antenna, a modulator, demodulator or modem, a microphone, a speaker, and such other components as can serve to communicate information with others. The personal communications device 200 preferably operates at a UHF frequency (or higher), such as 800-900 MHz, and can serve as a concurrent paging receiver, a fax modem operating at base band or other communications devices known to be in the prior art by those skilled in those arts.

Figure 13 is a schematic representation of the function of software in the present invention, describing the advantages provided by software operating in a computer connected to an accessible network.

Figure 14 is a block diagram representation of the software architecture of the present invention. At the highest levels, the software of the present invention fosters communication with external communications services. These levels of software communicate with software intended for communication within the personal communicator, including host level driver, serial I/O operators, local area networks, and so forth. At a lower level, the software of the personal communicator operates background applications, controls the file system, performs power management, and controls the I/O transport stack. The internal software also acts as an embedded digital signal manager, controls such functions as telephone stacking, call management, call control, and so forth.

35 At a still lower level, the software of the personal communicator drives the reconfigurable operating system which is used to control the reconfigurable circuitry of the personal communicator.

Figure 15 is a tabular representation of the dynamic configuration modes of the present invention, and Figure 16 is a schematic representation of the dynamic configuration modes of the present invention. As shown in Figure 16, the operation of the dynamic configuration modes activates a task stored in a configuration memory 220 and loads that task into a portion of the reconfigurable circuit 222. As conditions dictate, the task may be relocated within the reconfigurable circuit 222 or adjusted to accommodate changing conditions.

Figure 17 is a schematic representation of the run-time reconfigurable architecture of the present invention. Software from a portion of a read-only memory 250 is used to boot up the system when the system is activated. The system is booted up by being loaded into a configurable file working storage 252, which can be a portion of the various memory devices included in the personal communicator. A group of system applications are also stored in a system memory 254, which responds to signals issued by a download control circuit 256. The download control circuit 256 is connected to the interface 52. The interface 52 communicates with the configurable circuit 92. As shown schematically, the configurable circuit 92 is loaded with a number of programs having various desired capabilities.

Under control of signals from the download control 256, a desired capability not already present in the configurable circuit 92 is loaded from the system memory 254 to the working storage 252 and, from there, to the configurable circuit 92. If a capability which is present in the configurable circuit 92 is no longer needed, the software providing the capability is eliminated from the configurable circuit 92 and the software providing the remaining capabilities may be moved around on the configurable circuit 92 before new software for providing a new desired capability is loaded onto the configurable circuit 92.

Figure 18 is a schematic representation of a symmetrical array structure for use in the present invention, and Figure 19 is a schematic representation of a busing network symmetrical structure for use in the present invention.

Figure 20 is a schematic diagram of a cell structure for use in the present invention and more particularly for use in the symmetrical array structures shown in Figures 18 and 19. As will

be understood by those skilled in the arts, the cell structure includes processing elements, logic gates and timing circuitry to accomplish the desired results.

Figure 21 is a flow chart diagram of the stand-alone design environment of a field programmable gate array for use in the present invention. The flow chart diagram shows design entry, logic reduction and optimization, pre-layout timing and function verification, and then schematic regeneration resulting in bit stream generations which comprise the desired software.

Figure 22 is a flow chart diagram of the design environment of a field programmable gate array for use in the present invention, as will be understood by those skilled in the arts.

Figure 23 is a schematic diagram of an analog front end for use in the present invention. The front end 300 includes an antenna 302 and a diplexer 304. Signals received by the antenna 302 and passed through the diplexer 304 pass through the band pass filter 306 and an amplifier 308 to a mixer 310. The mixer 310 mixes the RF signals produced by the amplifier 308 with a local oscillator signal produced by the synthesizer 312, driven by a crystal 314. The signal output by the mixer 310 then passes through a bandpass filter 318 to a user, which may be an analog user or a digital user.

Signals produced by a microphone 320 is received by another mixer 322 which is also provided an RF signal by the synthesizer 312. The output of the mixer 322 passes through a bandpass filter 322 is received by another mixer 322 which is also provided an RF signal by the synthesizer 312. The output of the mixer 322 passes through a bandpass filter 324 to an amplifier 326. The output of the amplifier 326 is input to the diplexer 304 which serves to transfer the signals to the antenna 302 for transmittal as an electromagnetic wave.

Figure 24 is a schematic diagram of the digital hardware for use in a preferred embodiment of the present invention. The apparatus 350 includes the interface 52 and first and second configurable circuits 352 and 354. The first configurable circuit 352 is connected to the interface 52 and the second configurable circuit 354. The interface 52 is also connected to the second interface 354. The apparatus 350 also includes a third configurable circuit 356, a fourth configurable circuit

358, a microcontroller 360, a RAM 362 and a flash RAM 364. The first and second configurable circuit 352 are connected to the third configurable circuit 356, the microcontroller 360, the RAM 362 and the flash RAM 364. The fourth configurable circuit 358 is connected to the third configurable circuit 356 and the microcontroller 360. Under control of the microcontroller 360 the first, second third and fourth configurable circuits 352, 354, 356, and 358 are configured to accomplish the desired function of the apparatus 350 in accordance with the principles discussed in the foregoing, as will be understood by those skilled in the relevant electronics, computer and software arts. The desired capabilities can be stored in the RAM 362 and the flash RAM 364, as discussed above.

While the foregoing is a detailed description of the preferred embodiment of the invention, there are many alternative embodiments of the invention that would occur to those skilled in the art and which are within the scope of the present invention. Accordingly, the present invention is to be determined by the following claims.

Claims

1. A method for compiling one circuit in a sequence of circuits
5 within a programmable gate array (PGA) including a plurality of
logic gates, comprising the steps of:

a) establishing a first subplurality of logic gates in
the PGA, the first subplurality of logic gates constituting
logic gates that are not currently being used as part of an
10 existing circuit in the sequence of circuits;

b) establishing whether any of the existing circuits in
the sequence of circuits are decompilable circuits, each
decompilable circuit including a distinct subplurality of logic
gates in the PGA that are available for use in another circuit
15 in the sequence of circuits;

c) establishing a second subplurality of logic gates in
the PGA, the second subplurality of logic gates constituting
logic gates that are taken from the collection of logic gates
defined as the set union of the first subplurality of logic
20 gates and the distinct subpluralities of unused logic gates in
the existing circuits established as decompilable circuits in
the PGA;

d) determining a third subplurality of logic gates in the
PGA that is a subset of the second subplurality of gates, the
25 third subplurality being connectable to generate the one
circuit; and

e) connecting the gates in the third subplurality of
logic gates in the PGA to compile the one circuit.

30 2. The method of claim 1, wherein step b) includes determining
whether any subset of the existing circuits can be decompiled
and then recompiled to reconstitute the subset of existing
circuits, thereby rendering logic gates in the PGA that are
available for use in another circuit in the sequence of
35 circuits.

3. The method of claim 1, wherein the existing circuits receive
corresponding sets of input signals and generate corresponding
sets of output signals, each of the input signals and the output



signals having a value at a definite time, at least one of the output signals generated by one of the existing circuits being an input signal to one of the other existing circuits, further comprising the step of:

5 f) saving the value of at least one of the input and output signals at the definite time and subsequently applying a signal having the saved value to the one circuit.

4. A method for compiling one circuit in a sequence of circuits
10 within a programmable gate array (PGA) including a plurality of logic gates, comprising the steps of:

a) establishing whether any of the existing circuits in the sequence of circuits are decompilable circuits, each decompilable circuit including a distinct subplurality of logic
15 gates in the PGA that are available for use in another circuit in the sequence of circuits, the decompilable circuits each receiving at least one corresponding input signal and producing at least one corresponding output signal in response to the at least one corresponding input signal, each of the input signals
20 and the output signals having a value at a definite time; and

b) saving the value of at least one of the input or output signals at the definite time.

5. The method of claim 4, further including the steps of:

25 c) decompiling at least one of the decompilable circuits; and

d) applying a signal whose value was saved in step b) to a circuit in the sequence of circuits.

30 6. An apparatus for compiling one circuit in a sequence of circuits within a programmable gate array (PGA) including a plurality of logic gates, the apparatus comprising:

a first electronic circuit to establish a first subplurality
35 of logic gates in the PGA, the first subplurality of logic gates constituting logic gates that are not currently being used as part of an existing circuit in the sequence of circuits;

a second electronic circuit to establish whether any of the existing circuits in the sequence of circuits are decompilable



circuits, each decompilable circuit including a distinct subplurality of logic gates in the PGA that are available for use in another circuit in the sequence of circuits;

5 a third electronic circuit to establish a second subplurality of logic gates in the PGA, the second subplurality of logic gates constituting logic gates that are taken from the collection of logic gates defined as the set union of the first subplurality of logic gates and the distinct subpluralities of unused logic gates in the existing circuits established as
10 decompilable circuits in the PGA;

a fourth electronic circuit to determine a third subplurality of logic gates in the PGA that is a subset of the second subplurality of gates, the third subplurality being connectable to generate the one circuit; and

15 a fifth electronic circuit to connect the gates in the third subplurality of logic gates in the PGA to compile the one circuit.

7. The apparatus of claim 6, wherein the second electronic
20 circuit includes electronic circuitry to determine whether any subset of the existing circuits can be decompiled and then recompiled to reconstitute the subset of existing circuits, thereby rendering logic gates in the PGA that are available for use in another circuit in the sequence of circuits.

25 8. The apparatus of claim 6, wherein the existing circuits receive corresponding sets of input signals and generate corresponding sets of output signals, each of the input signals and the output signals having a value at a definite time, at
30 least one of the output signals generated by one of the existing circuits being an input signal to one of the other existing circuits, the apparatus further comprising:

a memory circuit to save the value of at least one of the input and output signals at the definite time, and

35 a fifth electronic circuit to subsequently apply a signal having the saved value to the one circuit.



9. An apparatus for compiling one circuit in a sequence of circuits within a programmable gate array (PGA) including a plurality of logic gates, the apparatus comprising:

a first electronic circuit to establish whether any of the
5 existing circuits in the sequence of circuits are decompilable circuits, each decompilable circuit including a distinct subplurality of logic gates in the PGA that are available for use in another circuit in the sequence of circuits, the decompilable circuits each receiving at least one corresponding
10 input signal and producing at least one corresponding output signal in response to the at least one corresponding input signal, each of the input signals and the output signals having a value at a definite time; and

a second electronic circuit to save the value of at least
15 one of the input or output signals at the definite time.

10. The apparatus of claim 9, further including:

a third electronic circuit to decompile at least one of the decompilable circuits; and

20 a fourth electronic circuit to retrieve the value of a signal whose value was saved by the second electronic circuit and apply the value to a circuit in the sequence of circuits.

11. An apparatus for compiling one circuit in a sequence of
25 circuits within a programmable gate array (PGA) including a plurality of logic gates, the apparatus comprising:

first means for establishing a first subplurality of logic gates in the PGA, the first subplurality of logic gates constituting logic gates that are not currently being used as
30 part of an existing circuit in the sequence of circuits;

second means for establishing whether any of the existing circuits in the sequence of circuits are decompilable circuits, each decompilable circuit including a distinct subplurality of logic gates in the PGA that are available for use in another
35 circuit in the sequence of circuits;

third means for establishing a second subplurality of logic gates in the PGA, the second subplurality of logic gates constituting logic gates that are taken from the collection of logic gates defined as the set union of the first subplurality



of logic gates and the distinct subpluralities of unused logic gates in the existing circuits established as decompilable circuits in the PGA;

fourth means for determining a third subplurality of logic gates in the PGA that is a subset of the second subplurality of gates, the third subplurality being connectable to generate the one circuit; and

fifth means for connecting the gates in the third subplurality of logic gates in the PGA to compile the one circuit.

12. The apparatus of claim 11, wherein the second means includes electronic circuitry to determine whether any subset of the existing circuits can be decompiled and then recompiled to reconstitute the subset of existing circuits, thereby rendering logic gates in the PGA that are available for use in another circuit in the sequence of circuits.

13. The apparatus of claim 11, wherein the existing circuits receive corresponding sets of input signals and generate corresponding sets of output signals, each of the input signals and the output signals having a value at a definite time, at least one of the output signals generated by one of the existing circuits being an input signal to one of the other existing circuits, the apparatus further comprising:

memory means for saving the value of at least one of the input and output signals at the definite time, and

sixth electronic means for subsequently applying a signal having the saved value to the one circuit.

14. An apparatus for compiling one circuit in a sequence of circuits within a programmable gate array (PGA) including a plurality of logic gates, the apparatus comprising:

first means for establishing whether any of the existing circuits in the sequence of circuits are decompilable circuits, each decompilable circuit including a distinct subplurality of logic gates in the PGA that are available for use in another circuit in the sequence of circuits, the decompilable circuits each receiving at least one corresponding input signal and



producing at least one corresponding output signal in response to the at least one corresponding input signal, each of the input signals and the output signals having a value at a definite time; and

5 second electronic means for saving the value of at least one of the input or output signals at the definite time.

15. The apparatus of claim 14, further including:

10 third electronic means for decompiling at least one of the decompilable circuits; and

 fourth electronic means for retrieving the value of a signal whose value was saved by the second electronic circuit and apply the value to a circuit in the sequence of circuits.

