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## (54) ANGLE MODULATION DETECTOR

(71) We, RCA CORPORATION, a corporation organized under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, New York 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to angle modulation detectors of the quadrature detector type and more particularly to circuitry to reduce the conversion of amplitude modulation of signals to spurious phase modulation within such quadrature detectors. Quadrature detectors are suitable for use in integrated circuit FM detectors used in radio receivers for frequency-modulation broadcasts to the public.

A quadrature detector for angle modulated waves is a detector which comprises a phase-shift network and a phase detecting multiplier (wherein one electrical signal is multiplied by another). The angle-modulated waves are coupled directly to a first input of the multiplier and via the phase-shift network to a second input of the multiplier. When the output of the multiplier is connected to the input of a low pass filter, then if the phase-shift network has a linear phase-shift versus frequency characteristic, the signal level out of the low-pass filter will be proportional to the frequency of the angle-modulated waves.

The quadrature detector is generally preceded by a limiter which removes amplitude variations from the angle-modulated waves, because the quadrature detector is undesirably responsive to amplitude variations. Such amplitude variations of the angle-modulated waves are caused by interference, noise and fading phenomena. The response of the quadrature detector to such amplitude variations would interfere with accurate recovery of the desired signal.

In certain applications it is desirable to introduce a first limiter-amplifier through which the angle-modulated waves are applied to a first one of the input to the multiplier.

This may be done to facilitate direct-coupling of the first input signal into the multiplier in an integrated circuit form of quadrature detector circuit, for instance. The first limiter-amplifier characteristically has time delay which varies in response to changing level of angle-modulated wave input signals. This is an undesired characteristic. Time delay variation with signal level makes the quadrature detector undesirably sensitive to amplitude variations of the angle-modulated waves applied as input to the quadrature detector.

A form of multiplier which is often used in integrated circuit detectors comprises two transistors having joined emitters supplied with a varying current as the first input to the multiplier. A signal voltage applied between the base electrodes of the two transistors is the second input to the multiplier. The product of the two inputs appears in the collector current of one of the transistors, and a signal exactly opposite thereto appears in the collector current of the other of the transistors. If the second input applied between the base electrodes of the multiplier transistors is large, the second input signals will in effect be limited prior to the multiplication process.

The multiplier may be used in balanced form. Two multiplier combinations as previously described are each provided with a first input which first inputs are balanced with respect to each other. That is, the first input signals are similar in waveform except for having opposite directions of swing. The second inputs applied between the base electrodes of the transistors in each multiplier are the same. The collector electrodes of the multipliers are connected so that their output voltages add together to provide increased detector output.

The first inputs of the multipliers described in the previous paragraph are often coupled thereto by way of an emitter-coupled differential amplifier. This differential amplifier has an input signal applied between the base electrodes of its transistors. It is common to make this input signal large enough to drive the differential amplifier into limiting. This will

[Price 25p]

Price 33p

introduce a time delay into the first inputs of the multipliers which will vary non-linearly with signal amplitude and adversely affect the insensitivity of the quadrature detector to amplitude modulation of the signal. The present invention can remedy this defect.

According to the invention, in a quadrature detector in which the signal coupling path to one of the multiplier inputs includes an emitter-coupled differential amplifier-limiter having an undesired characteristic of phase delay variation with variation of its input signal amplitude, a second emitter coupled differential amplifier-limiter having a similar phase delay variation characteristic is included in the signal coupling path to the second of the multiplier inputs. The effect upon the quadrature detector of phase shifts in response to amplitude changes which occur in the first limiter is thereby compensated for by similar phase shifts in response to amplitude changes which occur in the second limiter. In this way, the output of the quadrature detector is rendered substantially insensitive to a wide range of amplitude variations in the angle-modulated waves applied thereto.

Further understanding of the invention may be obtained from the following detailed description, when taken in conjunction with the accompanying drawings, in which:

Figure 1 is a schematic circuit diagram of a balanced angle modulation detector incorporating the principles of the present invention; and

Figures 2A, 2B and 2C are respective plots of the output of an angle modulation detector versus frequency.

Referring to the drawings, Figure 1 shows a quadrature detector comprising transistors 310, 312, 318, 320, 322 and 324, shown as being contained in an integrated circuit structure 14. Integrated circuit chip 14 may contain other circuits not essential for the understanding of this invention and therefore not illustrated. All circuit elements are located on the integrated circuit 14 unless otherwise specified. Transistors 310 and 312 have their emitter electrodes each connected to the collector electrode of a transistor 317 which provides constant-current bias to them.

The emitter electrodes of transistors 318 and 320 are each connected to the collector electrode of transistor 310. The emitter electrodes of transistors 322 and 324 are each connected to the collector electrode of transistor 312. The frequency modulated (FM) signal wave from a previous amplifier-limiter on the integrated circuit 14 (not shown) is applied in push-pull relation to the base electrodes of the transistors 310 and 312 via input points 234 and 236. The phase-shifted FM signal wave is applied in common to the base electrodes of the transistors 318 and 322 as will be subsequently explained. The base electrodes of the transistors 320 and 324 are connected to a constant

voltage at the emitter electrode of a transistor 360.

The collector electrodes of transistors 318 and 324 are coupled together and via a resistor 326 to a point 370. The collector electrodes of transistors 320 and 322 are coupled together and via a resistor 328 to a point 372. Points 370 and 372 are connected to the inputs of subsequent amplifier circuitry (not shown). Dotted resistors 380 and 382 connecting points 370 and 372, respectively, to terminal  $T_{14}$  (B+) represent the equivalent resistances of the inputs of this subsequent amplifier circuitry. Quiescent and signal components of the collector currents of transistors 318 and 324 are provided via the equivalent resistor 308. Quiescent and signal components of the collector currents of transistors 320 and 322 are provided via the equivalent resistor 382.

The base electrode of transistor 360 is connected via a point 306 to a 5.5 volt power supply (not shown) located elsewhere on the integrated circuit 14. The base electrode of transistor 360 is connected to a terminal  $T_{18}$  on the integrated circuit, which terminal is bypassed to ground reference potential via a capacitor 348 outside the integrated circuit. The transistor 360 has its emitter electrode coupled to ground via a resistor 362 and has its collector electrode connected to terminal  $T_{14}$ . Terminal  $T_{14}$  is connected to a source of operating potential (B+) located outside the integrated circuit.

Terminal  $T_{17}$  provides connection between ground potential references within and outside the integrated circuit. The operating potential (B+) may range from 8 to 16 volts referred to ground potential. Point 306 is maintained at a regulated 5.5 volts. The quiescent component of potential at points 234 and 236 is approximately 2.3 volts. The input signal swing is constrained between 1.5 and 3.5 volts approximately.

Preliminary limiter-amplifier circuitry suitable for providing signals to points 234 and 236 of the circuitry shown in Figure 1 is described in our application No. 39831/71 with a serial number 1357352.

To develop the phase-shifted FM signal, the FM signal from points 234 and 236 is applied to the base electrodes of a pair of transistors 332 and 334. The emitter electrodes of the transistors 332 and 334 are connected to the constant current source including the transistor 317. The collector electrode of the transistor 334 is connected to the operating potential connection 306 and the collector electrode of transistor 332 is connected to the emitter electrode of a transistor 338.

A fixed bias is applied to the base electrode of transistor 338 from the emitter electrode of a transistor 336 having its collector and its base electrodes connected to the operating potential connection 306. The collector elec-

trode of transistor 338 is connected to the operating potential supply connection 306 through a resistor 340. The collector electrode of transistor 338 is also connected to a terminal  $T_9$  of the integrated circuit chip 14.

A small capacitance capacitor 342 is shown connected between terminals  $T_9$  and  $T_{13}$ . Capacitor 342 may comprise stray capacitance alone.

Resistor 340 and capacitor 342 in combination with inductors 346 and 350 and a capacitor 351 comprise the phase shift network 62. Inductor 346 is connected between terminals  $T_{12}$  and  $T_9$ . Inductor 350 and capacitor 351 are connected in parallel combination between terminals  $T_{12}$  and  $T_{13}$ . Except for the resistor 340 and capacitor 342, the elements of the phase shift network 62 are located outside the integrated circuit.

The parallel combination of capacitor 351 and inductor 350 resonates near the center frequency of the applied wave. Capacitor 351, inductor 346, and inductor 350 are adjusted to cause  $90^\circ$  phase shift through the phase shift network 62 to occur at the unmodulated carrier frequency. A different carrier frequency causes a different phase shift through the phase shift network 62.

The terminal  $T_{12}$  is connected to the base electrode of an emitter-follower transistor 352. The collector electrode of transistor 352 is connected to terminal  $T_{14}$  (B+) and its emitter electrode is coupled to ground reference potential via a resistor 354.

The collector electrode of transistor 317 is connected to the emitter electrodes of transistors 310, 312, 332 and 334. Transistor 317 is arranged for constant collector current flow. Its emitter electrode is coupled via resistor 319 to ground potential. Its base electrode and the base electrode of a transistor 325 are each connected to the emitter electrode of a transistor 323.

The emitter electrode of transistor 325 is coupled via a resistor 321 to ground potential. The collector electrode of transistor 325 is connected to the base of transistor 323 and coupled via a resistor 327 to operating potential connection 306. The collector electrode of transistor 323 is shown connected to operating potential connection 306.

The emitter electrodes of transistors 310 and 312 are connected together and to a constant current source including transistor 317. The frequency modulated wave, coupled to points 234 and 236, switches the constant current flow between the transistors 310 and 312. In like manner, the phase shifted FM signal switches the current flow through transistors 318 and 322 relative to the current flow through the transistors 320 and 324, respectively. The phase of the phase shifted signal changes as a function of the frequency modulation (deviation) of the applied signal wave. As a result, when transistor 310 conducts, the

relative conduction angles of the transistors 318, 320 into the load resistors 380 and 382, respectively, are a function of the signal modulation.

This causes the output voltage of the detector, appearing between points 370 and 372, to vary from a positive voltage through zero to a minus voltage directly dependent upon the variations in the phase shift between the in-phase signal wave and the phase shifted signal wave. Therefore, if the quadrature ( $90^\circ$  phase) relationship between the signal waves at the carrier frequency is not maintained, the zero output voltage will be offset resulting in an unbalanced detector characteristic. An unbalanced detector characteristic causes the positive and negative halves of the detected signal waves to be unsymmetrical, thereby introducing non-linear distortion to the recovered signal wave.

Figure 2 shows the variation of detector output voltage as a function of frequency variation for three reception conditions. With no modulation on an input carrier wave and a perfect quadrature relationship between the in-phase and phase shifted signal waves appearing at the inputs to the switching transistors 318, 320, 322 and 324, the average detector output voltage will be zero as described above. This is shown at cross-over point 702 in Figures 2A and 2C.

Figure 2A shows the detector output voltage when a low level or weak signal wave is received. The wave is of insufficient amplitude to be limited. The wave is both amplitude modulated and frequency modulated. The change in output voltage at a given frequency is caused by the amplitude modulation of the frequency modulation signal wave envelope. To obtain the detector output voltage shown in Figure 2A at all signal levels where limiting occurs the quadrature relationship between the in-phase and phase shifted unmodulated carrier wave must be maintained at all signal levels.

Figure 2B shows the detector output voltage when the quadrature relationship between the signal waves in the in-phase and phase shifting transmission paths is not maintained at all signal levels. The signal levels are the same as those used in obtaining Figure 2A. It will be noted that the cross-over point 702 is shifted from the zero voltage axis. This results in the non-linear distortion of the recovered signal wave, as mentioned earlier.

Figure 2C shows the detector output voltage characteristic when: (1) limiting is maintained in both signal wave paths and (2) the quadrature relationship between in-phase and phase shifted carrier wave is maintained over a wide range of higher signal levels.

The quadrature detector shown in Figure 1 is an embodiment of the invention. A quadrature relationship can be maintained between unmodulated signal waves in the in-phase and

phase shifted signal wave paths at all signal levels. The detector has an output voltage versus frequency characteristic in accordance with Figure 2A at low signal levels and Figure 2C at higher signal levels.

Under weak signal conditions, the frequency modulated signal wave obtained from the output of preceding IF amplifier-limiter circuitry will have undesirable amplitude modulation appearing on it. Therefore, as much additional limiting as possible should be provided by the detector circuit itself to reduce the amount of AM recovered on the detected signal. Unfortunately, however, when the differential amplifier comprising transistors 310 and 312 are driven sufficiently hard to contribute a substantial amount of limiting, the variation in the phase delay of this differential amplifier as a function of signal amplitude will degrade the AM suppression of the detector. If there were no compensating variation of phase delay in the phase-shifting transmission path, the variation of phase delay in the in-phase transmission path will be indistinguishable from the desired angular modulation of the signal input. This spurious phase modulation component will be detected by the quadrature detector, which is undesirable. This limitation is overcome by the present embodiment of the invention shown in Figure 1.

The circuit of Figure 1 is constructed as described above, so that the same limiting and phase delay of signal take place in both the main signal wave path and the phase-shifted signal wave path. The equalization of delays in the two signal wave paths is extremely important, since it prevents the shift in the cross-over point 702 and permits the desired low-level operation shown in Figure 2A. As mentioned above, in the prior art, a quadrature detector circuit driven directly from the output signal at low signal levels, may exhibit a shifted detected cross-over point as shown at point 702 in Figure 2B.

The amplitude modulation of the angle modulated signal wave envelope when amplified or amplified and limited by a differential amplifier (such as formed by transistors 310, 312 or by transistors 332, 334) is subjected to a phase delay. The magnitude of this phase delay is a non-linear function of the amplitude of the signal wave envelope. That is, the phase delays for the maximum (crest) and minimum (trough) of the amplitude modulation are not equal. If this delay difference is  $\Delta t$ , then the amount the signal wave is shifted in phase is given by:

$$\Delta\theta = \Delta t \times f \times 360^\circ$$

where:

$\Delta\theta$  = the phase shift in degrees  
 $\Delta t$  = time in seconds  
 $f$  = frequency in Hz

This has the same effect as tuning the phase shift network (62),  $\Delta\theta$  degrees apart for the maximum and minimum of the AM modulation cycle. With equal non-linear phase delays introduced in both the in-phase and phase-shifted signal wave paths, as provided by the circuitry of Figure 1, the effective dynamic detuning on the maximum and minimum of the AM modulation cycle is substantially eliminated.

The use of two differential amplifiers comprising transistors 310, 312 and 332, 334, respectively, and operating in parallel overcomes the problem of a shift in cross-over point (Figure 2B) with input signal wave level. This results because any phase delay introduced in the in-phase signal wave path through transistors 310 and 312 is exactly offset by the delay in the signal wave path through transistors 332 and 334.

There is no relative delay then between the inputs of the multiplier transistors 318, 320, 322, 324, and the conduction angles of the multiplier transistors is unaffected by the delays. This makes the quadrature detector insensitive to the delay through the differential amplifier comprising transistors 310 and 312. The phase shifts caused by time delay through the differential amplifier transistors 310, 312 or 332, 334 is decreased about  $10^\circ$  when they are driven into hard limiting operated with high level input signals. In prior art circuits the differential amplifier comprising transistors 310, 312 is used alone. There is no auxiliary differential amplifier comprising transistors 332, 334 operated in parallel therewith to provide signals to the phase-shift network 62. Therefore, in the prior art circuits, the quadrature relationship between the signal waves in the in-phase and phase-shifted path is destroyed as the input level changes from the below limiting level to the limiting level with the cross-over point 702 (Figure 2B) shifting.

A small amount of additional compensation for time delays in the two signal paths is obtained by use of the common-base amplifier transistor 338 in the phase-shifted signal path. The non-linear delay of transistor 338 in the phase-shifted signal wave path provides a counterpart to non-linear delays caused by transistors 324, 318, 320, and 322 in the in-phase signal wave path.

The circuit arrangement described above will exhibit an unchanging delay difference at the collector electrodes of multiplier transistors 318 and 322 between the in-phase and phase-shifted signal wave paths because the phase-shifted signal wave is applied to the input base electrodes in order to control or gate the collector currents and the in-phase signal wave is applied to the emitter electrodes. The response to phase-shifted signals applied to the base electrodes of the multiplier transistors 318, 322 is delayed more than the response to the signals applied to their emitter electrodes. This

time delay corresponds to increased phase lag in the phase-shifted signal path. If the phase-shifted signal wave transmission path is to provide an overall  $90^\circ$  leading phase shift for unmodulated carrier wave, then the phase shift network must provide more than  $90^\circ$  of phase shift. Then this unvariant time delay may be compensated for. The disadvantage of such practice is that a single section of phase shift network cannot provide more than  $90^\circ$  of phase shift, so additional elements are required in the phase shift network.

In the embodiment of the present invention shown in Figure 1, the phase-shift network is devised to provide almost  $90^\circ$  of lag (phase retardation) rather than  $90^\circ$  of lead (phase advance). The phase-shift network lag is adjusted so that its approximately  $80^\circ$  of phase shift plus the additional  $10^\circ$  provided by the lag in driving the base electrodes of multiplier transistors 318 and 322 provides a total of  $90^\circ$  phase shift for the unmodulated carrier signal.

The additional  $10^\circ$  delay introduced between the base and collector electrodes of transistors 318 and 322 remains substantially constant, since the signal waves reaching the base electrodes are always maintained within the linear operating range for the usable input signal range. This is done by selecting the load resistor 340 to be of sufficiently low resistance that the auxiliary differential amplifier 332, 334 cannot provide overly large voltage swings at terminal  $T_0$ , even when the amplifier is driven into full limiting. The band-pass filter characteristic of the phase-shift network filters the phase-shifted wave appearing at terminal  $T_{12}$  making it essentially the same waveshape at all input signal levels. The input signal wave appearing at points 234 and 236 may be of sufficient magnitude to have been limited by a preceding intermediate frequency amplifier-limiter. Then it would be substantially a square wave signal with steep wave fronts, and the problem the present invention overcomes would not be presented.

When the input signal wave to the preceding limiter-amplifier is too small to maintain it well into limiting, the voltage appearing at points 234 and 236 more closely resembles a sine wave with sloping sides. The phase of the sine wave is shifted approximately  $10^\circ$  when it is amplified in transistors 310 or 312, as measured between their base electrode voltages and the collector currents they provide to the emitter electrodes of the multiplier transistors 318 and 320. About  $3^\circ$  more phase shift occurs in the sine wave before it appears at the collector electrodes of switching transistors 318 and 322.

The input signal wave is also coupled to transistors 332 and 334 which provide a delay of  $10^\circ$  between the sine wave signals, as measured between their base voltages and collector currents. This delay is equal to the delay

introduced by transistors 310 and 312. The signal wave appearing at the collector electrode of transistor 322 is fed to the emitter electrode of transistor 338 and is subjected to approximately  $3^\circ$  more phase shift lag before appearing at the collector of transistor 338. This phase shift lag is equal to the  $3^\circ$  phase shift lag introduced by switching transistors 318 and 322. The signal wave appearing at terminal  $T_0$  is coupled to inductors 346 and 350 and capacitor 351, which in conjunction with the collector load resistor 340, introduce a phase lag of approximately  $80^\circ$  with respect to the signal wave at terminal  $T_0$ .

Therefore, the signal wave appearing at terminal  $T_{12}$  lags behind the in-phase signal wave by this amount. The signal wave at terminal  $T_{12}$  is subjected to a minimal delay when it is coupled via the base-emitter electrodes of transistor 352 to the base electrode of multiplier transistor 318. Here, however, the phase shifted signal wave undergoes a phase shift lag of an additional  $10^\circ$  when it is coupled from the base electrodes to the collector electrodes of transistors 318 or 322.

The sum total phase shift lag, therefore, includes the  $10^\circ$  introduced by transistors 332 or 334, which is equal to the  $10^\circ$  introduced by transistor 310 or 312. The  $3^\circ$  phase shift lag introduced by transistor 338 is equal to the  $3^\circ$  phase shift lag introduced by multiplier transistors 318 and 322. At this point, no contribution has been made to separate the phase relationship of the two signal waves. An additional phase shift lag of approximately  $80^\circ$  is introduced by inductors 346 and 350 and capacitors 342 and 351, cooperating with resistor 340. Transistor 318 introduces approximately an additional  $10^\circ$  phase shift lag. This causes the phase-shifted signal wave to be substantially  $90^\circ$  behind the in-phase signal wave, as far as the responses to them at the collector electrodes of multiplier transistors 318 and 322 are concerned.

Accordingly, a balanced FM detector circuit of the type shown in Figure 1 provides superior amplitude modulation rejection, an improved limiting threshold, and a minimum of non-linear distortion.

Certain modifications of the embodiment shown in Figure 1 are within the contemplated scope of the invention. For instance, the emitters of transistors 310, 312, 332 and 334 are shown as being connected to the collector electrode of a single constant-current transistor 317. Since transistors 310 and 332 have their base emitter junctions connected in parallel, they will have equal current flows through them. Similarly, transistors 312 and 334, having their base-emitter junctions in parallel connection, will have equal current flows through them.

This same result can be obtained by coupling the joined emitters of transistors 332 and 334 to the collector electrode of a constant-

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current transistor different from, but similar to, a constant-current transistor with its collector electrode connected to the joined emitters of transistors 310 and 312. The base-emitter

5 biasing of the constant-current transistor 317 or its equivalent constant-current transistors can be effected by other well known means different than that shown.

10 The phase shift network 62 may be modified. For instance, the phase-shift network might comprise a double-tuned transformer, with primary and secondary windings tuned for anti-resonance at unmodulated carrier wave frequency and coupling between windings

15 selected for quadrature phase shift at unmodulated carrier wave frequency. The primary winding of such a transformer would be driven from the output of the auxiliary differential amplifier. The primary winding could, for example,

20 be driven from the collector electrode of transistor 338, instead of resistor 340 and capacitor 342. The ends of the secondary winding would be coupled to the joined base electrodes of transistors 318 and 322 and to the

25 joined base electrodes of transistors 320 and 324, respectively. The secondary winding could be connected at one end to a bias potential to provide single-ended phase-shifted signal drive to the multiplier transistors 318, 320,

30 322, 324 in a manner analogous to that shown in Figure 1. Alternatively, the secondary winding could be center-tapped, with the center-tap connected to a bias potential so that push-pull phase-shifted signals are supplied to the

35 multiplier transistors 318, 320, 322, 324.

While the phase-shifted signal path is most conveniently applied to the base electrodes of the multiplier transistors 318, 320, 322, 324 and the in-phase signal path to their emitter electrodes, the signal paths can be connected

40 in opposite manner.

#### WHAT WE CLAIM IS:—

1. A quadrature detector of angle modulated waves including a phase detecting multiplier having first and second inputs to receive signals to be multiplied thereby, first and second coupling means respectively coupling said first and second inputs of said multiplier to the input of the quadrature detector, one of said coupling means including a phase shift network, said first coupling means including a first emitter-coupled differential amplifier-limiter having an undesired characteristic of phase delay variation with variation of its input signal amplitude, and said second coupling means including a second emitter-coupled differential amplifier-limiter having a characteristic of phase delay variation with variation of its input signal amplitude similar to that of said

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first limiter, whereby said quadrature detector is rendered relatively insensitive to said undesired characteristic.

2. A quadrature detector as claimed in claim 1, wherein said multiplier comprises at least

first and second transistors with emitter electrodes connected together to form one of said inputs of said multiplier, and with base electrodes at least one of which forms the other multiplier input, said output of said multiplier being obtained from at least one of the collector electrodes of said first and said second transistors; said first limiter comprising third and fourth transistors having joined emitter electrodes connected to receive operating current, the base electrodes of said third and fourth transistors being coupled to the input of said quadrature detector, and the collector electrodes thereof forming the outputs of said first limiter with one of them connected to said first input of said multiplier; said second limiter comprising fifth and sixth transistors having joined emitter electrodes connected to receive operating current, base electrodes each of which is connected to a different one of said base electrodes of said third and fourth transistors, and collector electrodes forming first and second outputs of said second limiter, respectively; and said phase-shift network being frequency dependent and having an input coupled to said first output of said second limiter and having an output coupled to said second input of said multiplier to provide phase shifted signal voltages thereto.

3. A quadrature detector as claimed in claim 2, characterized by a seventh transistor connected in a common-base amplifier configuration with an input coupled from said first output of said second limiter and with an output coupled to said frequency-dependent phase-shift network.

4. A quadrature detector as claimed in claim 2 or 3, wherein said emitter electrodes of said third, fourth, fifth and sixth transistors are connected in common to a source of operating current.

5. A quadrature detector as claimed in any of claims 2, 3 and 4 wherein the amplitude of the output of said second limiter is limited to a small value such that the response of said output of said multiplier to said phase shifted signal voltages applied thereto does not show appreciable non-linear phase delay as a function of signal amplitudes.

6. A quadrature detector (of angle modulated waves) as claimed in any of claims 2—5 wherein the connected emitter electrodes of said first and second transistors form the first multiplier input connected to the collector electrode of one of said third and fourth transistors, and wherein an additional two transistors having base electrodes respectively connected to said base electrodes of said first and second transistors, and having collector electrodes respectively connected to said collector electrodes of said second and first transistors, have their emitter electrodes joined together and connected to the collector electrode of the other one of said third and fourth transistors.

7. A quadrature detector substantially as



current transistor different from, but similar to, a constant-current transistor with its collector electrode connected to the joined emitters of transistors 310 and 312. The base-emitter

5 biasing of the constant-current transistor 317 or its equivalent constant-current transistors can be effected by other well known means different than that shown.

The phase shift network 62 may be modified. For instance, the phase-shift network might comprise a double-tuned transformer, with primary and secondary windings tuned for anti-resonance at unmodulated carrier wave frequency and coupling between windings selected for quadrature phase shift at unmodulated carrier wave frequency. The primary winding of such a transformer would be driven from the output of the auxiliary differential amplifier. The primary winding could, for example, be driven from the collector electrode of transistor 338, instead of resistor 340 and capacitor 342. The ends of the secondary winding would be coupled to the joined base electrodes of transistors 318 and 322 and to the joined base electrodes of transistors 320 and 324, respectively. The secondary winding could be connected at one end to a bias potential to provide single-ended phase-shifted signal drive to the multiplier transistors 318, 320, 322, 324 in a manner analogous to that shown in Figure 1. Alternatively, the secondary winding could be center-tapped, with the center-tap connected to a bias potential so that push-pull phase-shifted signals are supplied to the multiplier transistors 318, 320, 322, 324.

While the phase-shifted signal path is most conveniently applied to the base electrodes of the multiplier transistors 318, 320, 322, 324 and the in-phase signal path to their emitter electrodes, the signal paths can be connected in opposite manner.

#### WHAT WE CLAIM IS:—

1. A quadrature detector of angle modulated waves including a phase detecting multiplier having first and second inputs to receive signals to be multiplied thereby, first and second coupling means respectively coupling said first and second inputs of said multiplier to the input of the quadrature detector, one of said coupling means including a phase shift network, said first coupling means including a first emitter-coupled differential amplifier-limiter having an undesired characteristic of phase delay variation with variation of its input signal amplitude, and said second coupling means including a second emitter-coupled differential amplifier-limiter having a characteristic of phase delay variation with variation of its input signal amplitude similar to that of said first limiter, whereby said quadrature detector is rendered relatively insensitive to said undesired characteristic.

2. A quadrature detector as claimed in claim 1, wherein said multiplier comprises at least

first and second transistors with emitter electrodes connected together to form one of said inputs of said multiplier, and with base electrodes at least one of which forms the other multiplier input, said output of said multiplier being obtained from at least one of the collector electrodes of said first and said second transistors; said first limiter comprising third and fourth transistors having joined emitter electrodes connected to receive operating current, the base electrodes of said third and fourth transistors being coupled to the input of said quadrature detector, and the collector electrodes thereof forming the outputs of said first limiter with one of them connected to said first input of said multiplier; said second limiter comprising fifth and sixth transistors having joined emitter electrodes connected to receive operating current, base electrodes each of which is connected to a different one of said base electrodes of said third and fourth transistors, and collector electrodes forming first and second outputs of said second limiter, respectively; and said phase-shift network being frequency dependent and having an input coupled to said first output of said second limiter and having an output coupled to said second input of said multiplier to provide phase shifted signal voltages thereto.

3. A quadrature detector as claimed in claim 2, characterized by a seventh transistor connected in a common-base amplifier configuration with an input coupled from said first output of said second limiter and with an output coupled to said frequency-dependent phase-shift network.

4. A quadrature detector as claimed in claim 2 or 3, wherein said emitter electrodes of said third, fourth, fifth and sixth transistors are connected in common to a source of operating current.

5. A quadrature detector as claimed in any of claims 2, 3 and 4 wherein the amplitude of the output of said second limiter is limited to a small value such that the response of said output of said multiplier to said phase shifted signal voltages applied thereto does not show appreciable non-linear phase delay as a function of signal amplitudes.

6. A quadrature detector (of angle modulated waves) as claimed in any of claims 2—5 wherein the connected emitter electrodes of said first and second transistors form the first multiplier input connected to the collector electrode of one of said third and fourth transistors, and wherein an additional two transistors having base electrodes respectively connected to said base electrodes of said first and second transistors, and having collector electrodes respectively connected to said collector electrodes of said second and first transistors, have their emitter electrodes joined together and connected to the collector electrode of the other one of said third and fourth transistors.

7. A quadrature detector substantially as

hereinbefore described with reference to the accompanying drawings.

- 5 8. An integrated circuit embodying a quadrature detector according to any preceding claim, with possible exception of elements of said phase shifting network.

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