METHODS AND APPARATUS FOR CONTROLLING A PLASMA PROCESSING SYSTEM

BACKGROUND OF THE INVENTION

[0001] In the semiconductor industry, the use of RF driven plasma chambers for manufacturing silicon wafers is commonplace. There exists a common need within such applications to monitor the sheath voltage, and specifically how the sheath voltage relates to the DC bias potential of the wafer itself.

[0002] Currently, there are several techniques to ascertain wafer potential, as well as sheath and bulk plasma potential. With respect to the wafer DC bias potential, one monitoring method includes measuring the self-bias voltage of the wafer by detecting the leakage current between the wafer and the electrostatic chuck (ESC) while varying an applied DC voltage to the ESC. While this technique is used within some current production settings, the computed value is highly dependent upon the magnitude of the leakage current, which is coupled to the type of ESC in the system. The method of detecting leakage current through the wafer to the ESC is also highly dependent upon different types of backside wafer films.

[0003] Another method for ascertaining the wafer bias potential is through the use of silicon carbide pins attached to the outer edge of the ESC and in contact with the plasma. However, such pins are consumables and have to be replaced frequently within production environments.

[0004] A third method for detecting the DC bias on the wafer is through a RF voltage probe at the ESC and a signal processing unit which computes the wafer voltage from the peak to peak RF voltage. This method provides a means for detecting the wafer DC bias voltage without a probe in direct contact with the plasma by scaling the RF voltage at the ESC to a DC value through the use of a calibrated gain and offset. This method assumes a purely linear relationship to the RF peak to peak voltage and the DC potential of the wafer which is not the case for multi-frequency plasmas. Figure 1 shows the correlation of wafer bias to RF Vpp. In Figure 1, when a linear fit is applied, the R-squared value is significantly less than one [e.g., R-sq: .90].

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

[0007] Fig. 1 shows the correlation of wafer bias to RF Vpp.

[0008] Fig. 2 shows the correlation of the wafer bias to the output of the disclosed RF voltage transfer function, with an R-squared value significantly closer to one.

[0009] Fig. 3 depicts testing confirming the relationship between the plasma potential as seen by a Si carbide pin and the wafer potential as measured by a wired wafer.

[00010] Fig. 4 shows the voltage seen by the Si HER (Hot Edge Ring) during a HARC (High Aspect Ratio Contact) process using 2MHz, 27MHz, and 60MHz on a Lam DFC2300 Flex45 platform versus the voltage seen by Si carbide pin.

[00011] Fig. 5A depicts a system with a RF driven plasma that consists of an ESC power by three RF generators.

[00012] Fig. 5B illustrates an embodiment of the disclosed invention, where a voltage probe, consisting of a capacitive divider network, is attached to the RF rod in close proximity to the ESC base plate as well as a signal conditioning and signal processing apparatus.

[00013] Fig. 5C is an embodiment of an analog RF voltage signal conditioning network with a digital signal processing unit.

[00014] Figs. 6 – 10 discuss the high impedance RF voltage probe for computing wafer potential based on frequency dependent RF voltage signals.

DETAILED DESCRIPTION OF EMBODIMENTS

[00015] The present invention will now be described in detail with reference to a few embodiments thereof as illustrated in the accompanying drawings. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process steps and/or structures have not been described in detail in order to not unnecessarily obscure the present invention.

[00016] Various embodiments are described herein below, including methods and techniques. It should be kept in mind that the invention might also cover articles of manufacture that includes a computer readable medium on which computer-readable instructions for carrying out embodiments of the inventive technique are stored. The computer readable medium may include, for example, semiconductor, magnetic, opto-magnetic, optical, or other forms of computer readable medium for storing computer readable code. Further, the invention may also cover apparatuses for practicing embodiments of the invention. Such apparatus may include

circuits, dedicated and/or programmable, to carry out tasks pertaining to embodiments of the invention. Examples of such apparatus include a general-purpose computer and/or a dedicated computing device when appropriately programmed and may include a combination of a computer/computing device and dedicated/programmable circuits adapted for the various tasks pertaining to embodiments of the invention.

[00017] Embodiments of the disclosed invention will provide the end user the ability to measure the wafer bias potential by appropriately filtering and conditioning the RF voltage at the ESC and utilizing a transfer function that accounts for contribution of multiple RF frequencies in biasing the wafer. Figure 2 shows the correlation of the wafer bias to the output of the disclosed RF voltage transfer function, with an R-squared value significantly closer to one [e.g., R-sq: .97].

[00018] This invention was conceived while attempting to improve an existing method of measuring DC bias Potential with a silicon carbide pin. The wear rate of this pin as well as the quartz insulating material which housed the pin was found to be a limiting factor for production throughput. It has been determined that although a non-linear relationship existed between the RF voltage and wafer potential in a multi-frequency plasma, a transfer function could be used to derive wafer potential based upon the contribution of each individual frequency driving the plasma.

[00019] Testing has been done to confirm the relationship between the plasma potential as seen by a Si carbide pin and the wafer potential as measured by a wired wafer, depicted in Figure 3. It is then shown that the disclosed transfer function was significantly correlated to the voltage signal seen by the existing Si carbide pin.

[00020] Figure 4 shows the voltage seen by the Si HER (Hot Edge Ring) during a HARC (High Aspect Ratio Contact) process using 2MHz, 27MHz, and 60MHz on a Lam DFC2300 Flex45 platform (available from Lam Research Corporation of Fremont, CA) versus the voltage seen by Si carbide pin. Given the aforementioned correlation of the Si carbide pin to the wired wafer, the commutative property provides credence to the statement that a transfer function involving individual RF voltages driving plasma is also a valid representation of the plasma sheath voltage at the wafer interface. In one or more embodiments, state-space analysis may be performed on the RF voltage to derive the transfer functions. State-space modeling is well-known and will not be elaborated here. In one or more embodiments, known transient handling techniques may be applied to improve robustness.

[00021] The features and advantages of embodiments of the invention may be better understood with reference to the figures and discussions that follow.

[00022] Generally speaking, the ability to indirectly measure the DC component of the plasma sheath potential within a RF driven plasma is dependent on a voltage probe connected to the RF rod in close proximity to the ESC. Figure 5A depicts a system with a RF driven plasma that consists of an ESC 502 power by three RF generators 504A, 504B, and 504C via an impedance matching network 506. These RF generators provide different RF frequencies as shown although the number of frequencies employed, the exact frequencies employed as well as the number of RF generators employed may vary according to applications. An RF rod or another suitable RF sensing mechanism in close proximity (i.e., sufficiently close as to be able to sense the RF voltage) to base plate 508 (or another non-plasma exposing component associated with the ESC) provides a RF voltage to capacitive divider network 530. Capacity divider 530 will be discussed in greater details herein in connection with Fig. 5B. The output of capacitive divider network 530 is then provided to a signal conditioning and processing block 532, which will be discussed in greater details in connection with Fig. 5C herein below.

[00023] Figure 5B illustrates an example embodiment of the disclosed invention, where a voltage probe, including a capacitive divider network 530, is coupled to the RF rod (or another suitable RF sensing mechanism) in close proximity to the ESC base plate as well as coupled to a signal conditioning and signal processing apparatus. In the example of Fig. 5B, capacitor C1 is in series with capacitor C2, which is then in series with the parallel capacitors C3/C4. The voltage signal is obtained as shown in Fig. 5B. The capacitive divider voltage probe provides a high impedance path for the RF voltage to be sensed without unduly perturbing the RF power driving the plasma.

[00024] The specific make up of the capacitive divider is dependent upon the RF generators driving the plasma, with the highest frequency generator being the dominant factor. The capacitive divider also sufficiently attenuates the voltage signal by providing a low impedance path to ground in parallel with a 50-ohm coaxial cable responsible for carrying the voltage signal to the signal conditioning and signal processing apparatus. Note that these values are provided as example and for reference only and are not limiting. In the example of Fig. 5B the input impedance is significantly high [$Z = 1/(\omega * C)$, when $\omega = 60$MHz, $C = .5$pF then $Z \sim 33$Kohms] and the impedance to ground is low (~31ohms @ 60Mhz).

[00025] The RF voltage signal is then conditioned through a network of analog or digital filters. Figure 5C is an example embodiment of an analog RF voltage signal conditioning network of the type implemented in block 532 of Fig. 5A. At the input of the analog RF voltage signal conditioning network, the signal is split into a number of separate channels (4 in the example of Fig 5C) to allow for RF filtering of specific RF frequencies responsible for driving the plasma. In this embodiment, the RF generator frequencies are 2MHz, 27MHz, and 60MHz. One channel is not filtered, which maintains the broadband voltage frequency spectrum. In this embodiment the four channels are converted to a DC signal via a passive peak detector [e.g., 1N5711 diode], although an active peak detector could be used as well.

[00026] The DC signals are then converted to digital signals in order to be processed by the digital signal processor, where the individual signals are calibrated and inputted into the wafer bias transfer function. The output of the transfer function is then fed back to the bias compensation network. It should be noted that the disclosed analog signal conditioning network could be accomplished entirely within the digital domain. In this instance, there would be no need for a signal splitter or analog filters, simply an analog to digital converter (ADC) and a signal processing unit (DSP, FPGA, CPLD or the like), with the signal processing unit responsible for all filtering, peak detection, calibration, and transfer function computation.

[00027] In one or more embodiments, the calibration of each voltage channel is performed by applying a gain and offset to each channel. The gain and offset for each channel (2MHz, 27MHz, 60MHz and broadband unfiltered voltages in the example of Figs. 5A-5C) is determined by the signal response of a given channel and its correlation to the wafer bias. For the filtered channels, this is accomplished by characterizing a given filtered channel response to the wafer bias for that unique single frequency. For instance, the response of the 2MHz channel would be correlated to the wafer bias for plasma being driven by 2MHz only and the subsequent gain and offset would be used to calibrate this channel. This is repeated for 27MHz and 60MHz. The broadband signal is calibrated by correlating the wafer bias for plasma being driven by all three frequencies and each subsequent variation (2MHz only, 2 MHz and 27MHz, 60MHz only, 27MHz and 60MHz, etc…).

[00028] An important factor into the calibration is also the response of the capacitive divider voltage probe530. The capacitive divider tends to have a unique signal response for each frequency. As a suggested solution, a network analyzer can be used to characterize the response

of the capacitive divider voltage sensor, and this response can then used to modify the aforementioned calibration coefficients accordingly. This is an important component in manufacturing accurate and repeatable instruments.

[00029] The transfer function for computing wafer bias in composed of four inputs: the calibrated DC voltage signals for 2MHz, 27MHz, and 60MHz as well as the unfiltered broadband signal. The voltage signals are then multiplied by a set of coefficients. Each coefficient is a function of a given frequency mixture driving the plasma. The coefficients are derived through, for example, principal component analysis (PCA) of the matrix consisting of the wafer bias and the four voltage signals (2MHz, 27MHz, 60MHz, and broadband). The individual resultants of the coefficient multiplication are then summed, producing a wafer bias value. Conditional statements and weighting factors can also be used to optimize the coefficients and thus optimize the transfer function result.

[00030] Figs. 6 – 10 further discuss the high impedance RF voltage probe for computing wafer potential based on frequency dependent RF voltage signals. In Fig. 6, a linear transfer function is created and the example flowchart illustrates how this linear transfer function may be employed to produce the wafer bias value. Fig. 7 is a flowchart illustrating the use of a non-linear transfer function to produce the wafer bias value. Non-linear transfer functions are believed to be better able to approximate the wafer bias value from the RF voltage in some, if not most, situations. Figs. 8, 9, and 10 are further explanation of the merits of each approach (linear vs. nonlinear). Both approaches provide a way, in accordance with embodiments of the invention, to correlate the sensed RF voltage to the wafer bias voltage, especially in multi-frequency applications. The wafer bias voltage may then used as a feedback or control signal for the ESC power supply and/or bias compensation network and/or other subsystems in the plasma processing system.

[00031] While this invention has been described in terms of several preferred embodiments, there are alterations, permutations, and equivalents, which fall within the scope of this invention. It should also be noted that there are many alternative ways of implementing the methods and apparatuses of the present invention. Although various examples are provided herein, it is intended that these examples be illustrative and not limiting with respect to the invention.

CLAIMS

What is claimed is:

1. A method for controlling a plasma processing system operating using multiple RF frequencies, comprising:

obtaining an RF voltage signal from an RF sensing mechanism via a high impedance path;

processing said RF voltage signal to obtain a plurality of signals, said plurality of signals including at least individual signals corresponding to individual ones of said multiple RF frequencies;

inputting said plurality of signals into a transfer function; and

providing an output of said transfer function as a control signal to control at least a subsystem of said plasma processing system.

2. The method of claim 1 wherein said RF sensing mechanism is sufficiently proximate to a non-plasma exposing component of said ESC sub-system to obtain said RF voltage signal.

3. The method of claim 2 wherein said non-plasma exposing component is a base plate.

4. The method of claim 3 wherein said RF sensing mechanism is an RF rod.

5. The method of claim 1 wherein said high impedance path is implemented at least by a capacitor divider network.

6. The method of claim 1 wherein said plurality of signals also include at least a signal corresponding to an unfiltered broadband version of said RF voltage signal.

7. The method of claim 1 wherein said processing includes calibrating said plurality of signals.

8. The method of claim 1 wherein said transfer function represents a linear transfer function.

9. The method of claim 8 wherein said linear transfer function is obtained using multi-variate analysis.

10. The method of claim 1 wherein said transfer function represents a non-linear transfer function.

11. The method of claim 10 wherein said non-linear function is obtained using a power equation.

12. The method of claim 1 wherein said processing includes at least analog filtering.

13. The method of claim 1 wherein said processing includes at least digital signal processing.

14. A plasma processing system configured for processing at least one wafer disposed on an electrostatic chuck (ESC), comprising:

an RF sensing mechanism, said RF sensing mechanism is sufficiently proximate to a non-plasma exposing component of said ESC to obtain an RF voltage signal.;

a high impedance arrangement coupled to said RF sensing mechanism to facilitate acquisition of said RF voltage signal while reducing perturbation of RF power driving a plasma in said plasma processing system;

a signal processing arrangement configured to receive said RF voltage signal and to apply one of a digital and analog version of said RF voltage signal to a transfer function to obtain a transfer function output; and

an ESC power supply subsystem configured to receive said transfer function output as a feedback signal to control said plasma processing system during processing of said at least one wafer.

15. The plasma processing system of claim 14 wherein said non-plasma exposing component is a base plate.

16. The plasma processing system of claim 14 wherein said RF sensing mechanism is an RF rod.

17. The plasma processing system of claim 14 wherein said high impedance arrangement is implemented at least by a capacitor divider network.

18. The plasma processing system of claim 14 wherein said RF voltage signal is processed by said signal processing arrangement into a plurality of signals that includes at least a signal corresponding to an unfiltered broadband version of said RF voltage signal.

19. The plasma processing system of claim 18 wherein said processing includes calibrating said plurality of signals.

20. The plasma processing system of claim 14 wherein said transfer function represents a linear transfer function.

21. The plasma processing system of claim 14 wherein said transfer function represents a non-linear transfer function.