FIG. 1

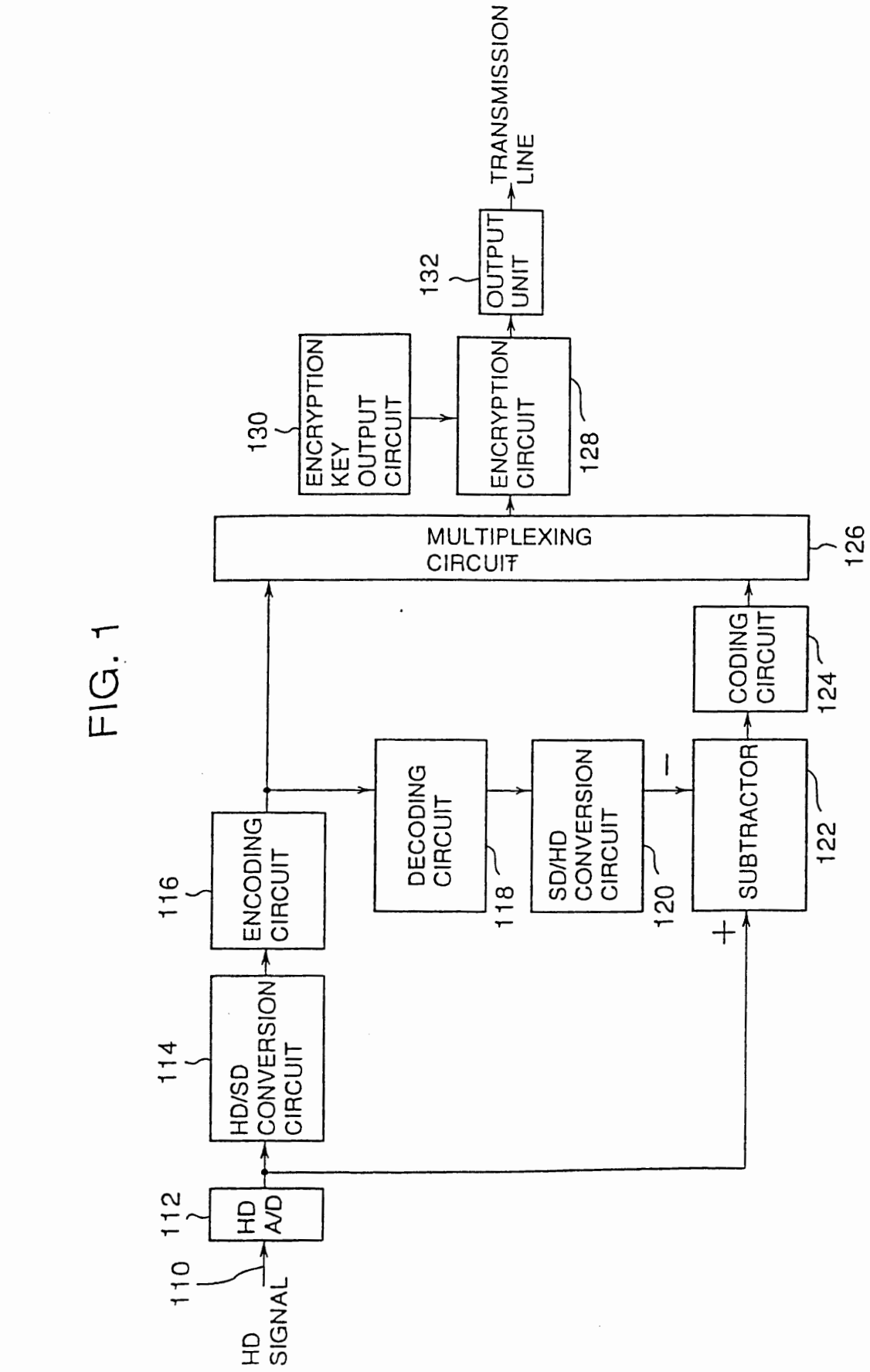

HD SIGNAL
110
HD A/D
112
HD/SD CONVERSION CIRCUIT
114
ENCODING CIRCUIT
116
DECODING CIRCUIT
118
SD/HD CONVERSION CIRCUIT
120
SUBTRACTOR
122
CODING CIRCUIT
124
MULTIPLEXING CIRCUIT
126
ENCRYPTION CIRCUIT
128
ENCRYPTION KEY OUTPUT CIRCUIT
130
OUTPUT UNIT
132
TRANSMISSION LINE
+
-

FIG. 2

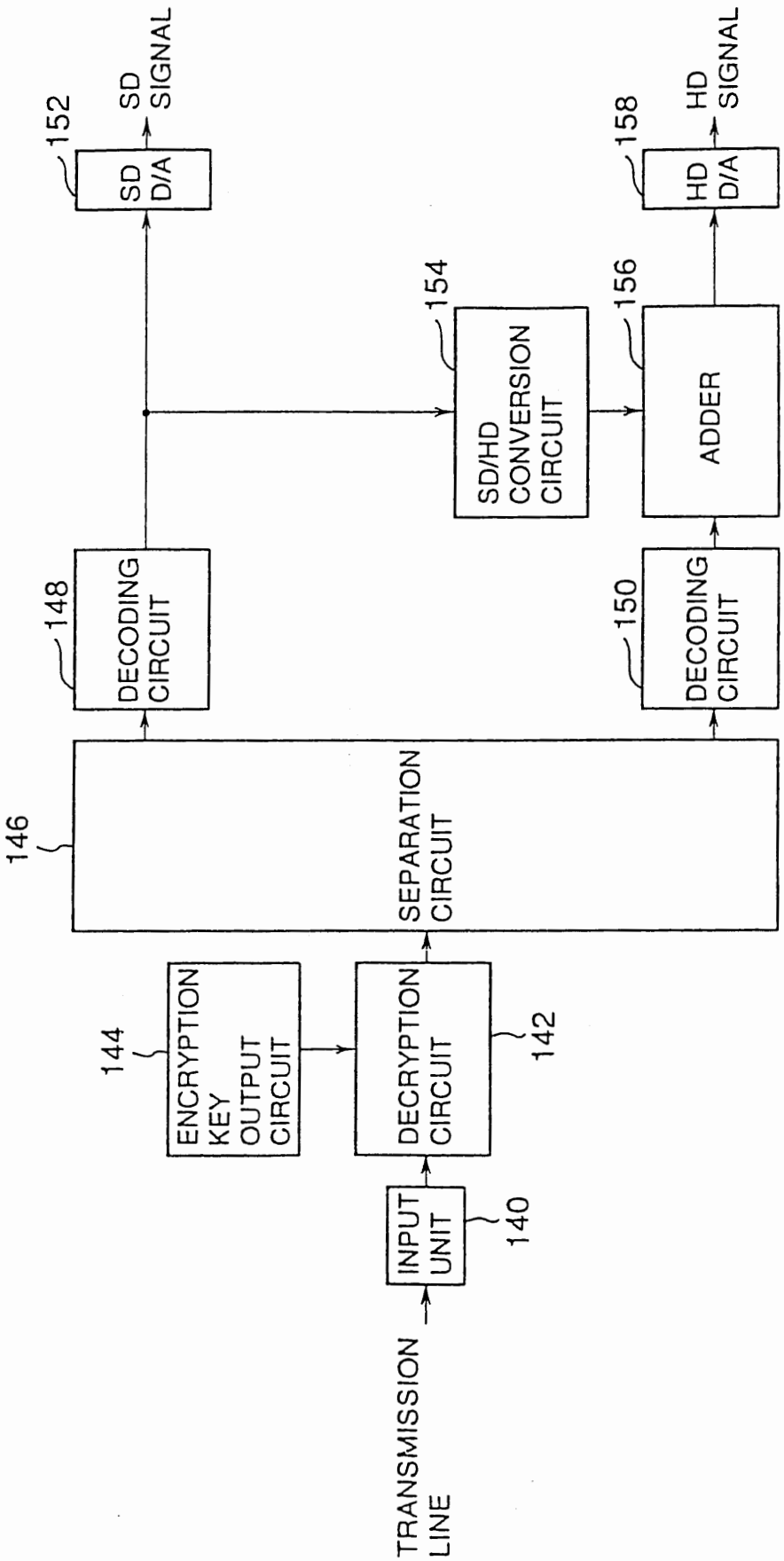

TRANSMISSION LINE
INPUT UNIT
140
DECRYPTION CIRCUIT
142
ENCRYPTION KEY OUTPUT CIRCUIT
144
SEPARATION CIRCUIT
146
DECODING CIRCUIT
148
DECODING CIRCUIT
150
SD D/A
152
SD SIGNAL
SD/HD CONVERSION CIRCUIT
154
ADDER
156
HD D/A
158
HD SIGNAL

FIG. 3

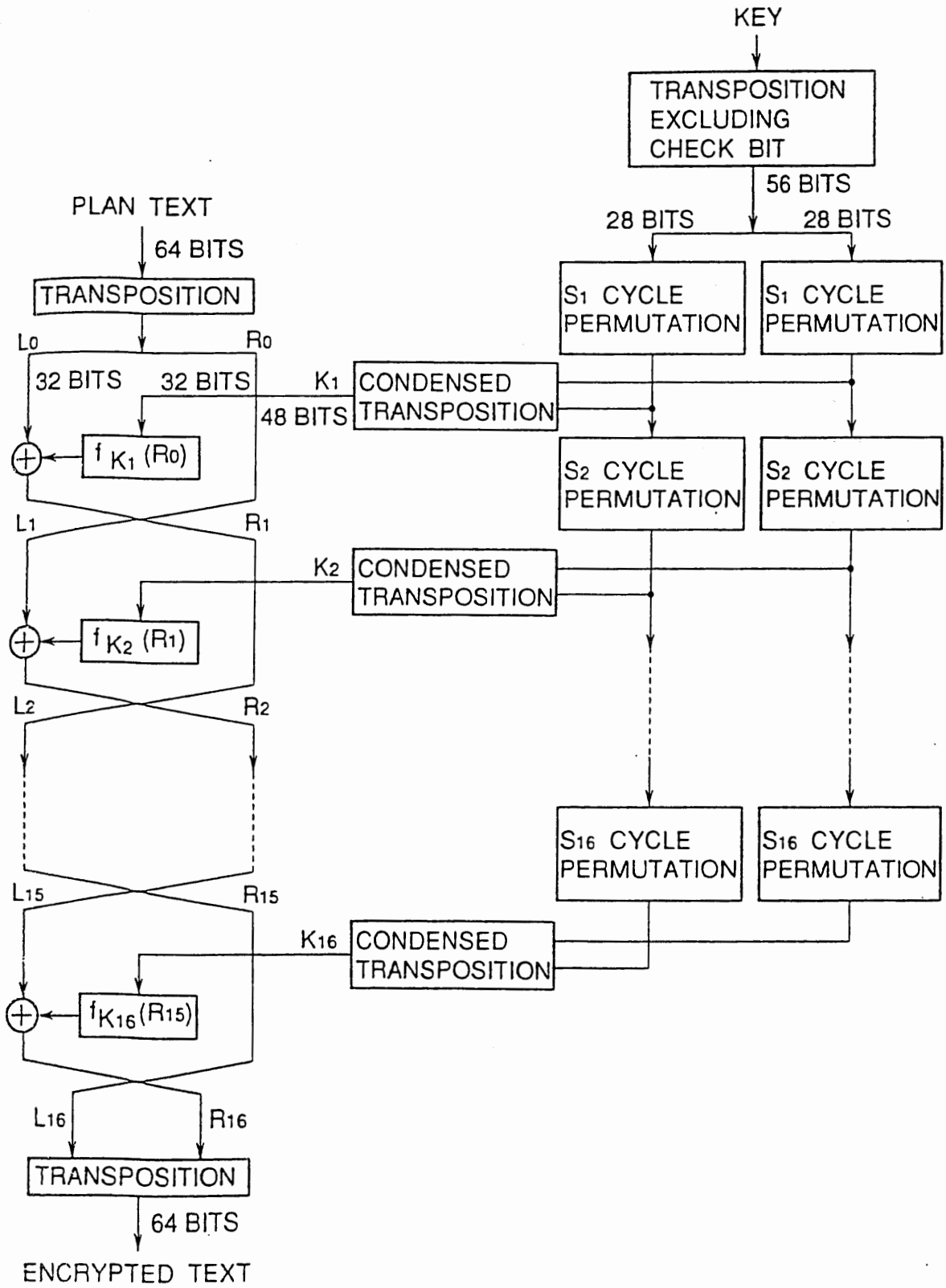

KEY
TRANSPOSITION EXCLUDING CHECK BIT
56 BITS
28 BITS
28 BITS
PLAN TEXT
64 BITS
TRANSPOSITION
S1 CYCLE PERMUTATION
S1 CYCLE PERMUTATION
L0
R0
32 BITS
32 BITS
K1
48 BITS
CONDENSED TRANSPOSITION
f K1 (R0)
S2 CYCLE PERMUTATION
S2 CYCLE PERMUTATION
L1
R1
K2
CONDENSED TRANSPOSITION
f K2 (R1)
L2
R2
S16 CYCLE PERMUTATION
S16 CYCLE PERMUTATION
L15
R15
K16
CONDENSED TRANSPOSITION
f K16 (R15)
L16
R16
TRANSPOSITION
64 BITS
ENCRYPTED TEXT

FIG. 4

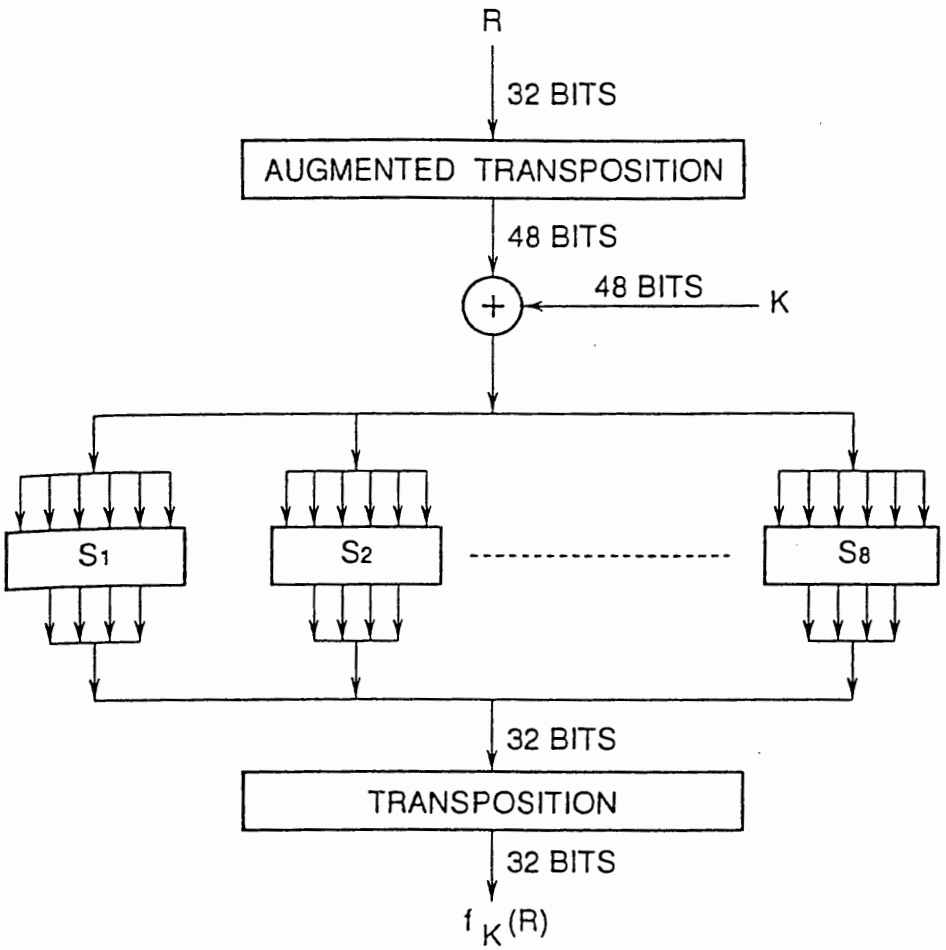

R
32 BITS
AUGMENTED TRANSPOSITION
48 BITS
48 BITS
K
S1
S2
S8
32 BITS
TRANSPOSITION
32 BITS
f K (R)

FIG. 5

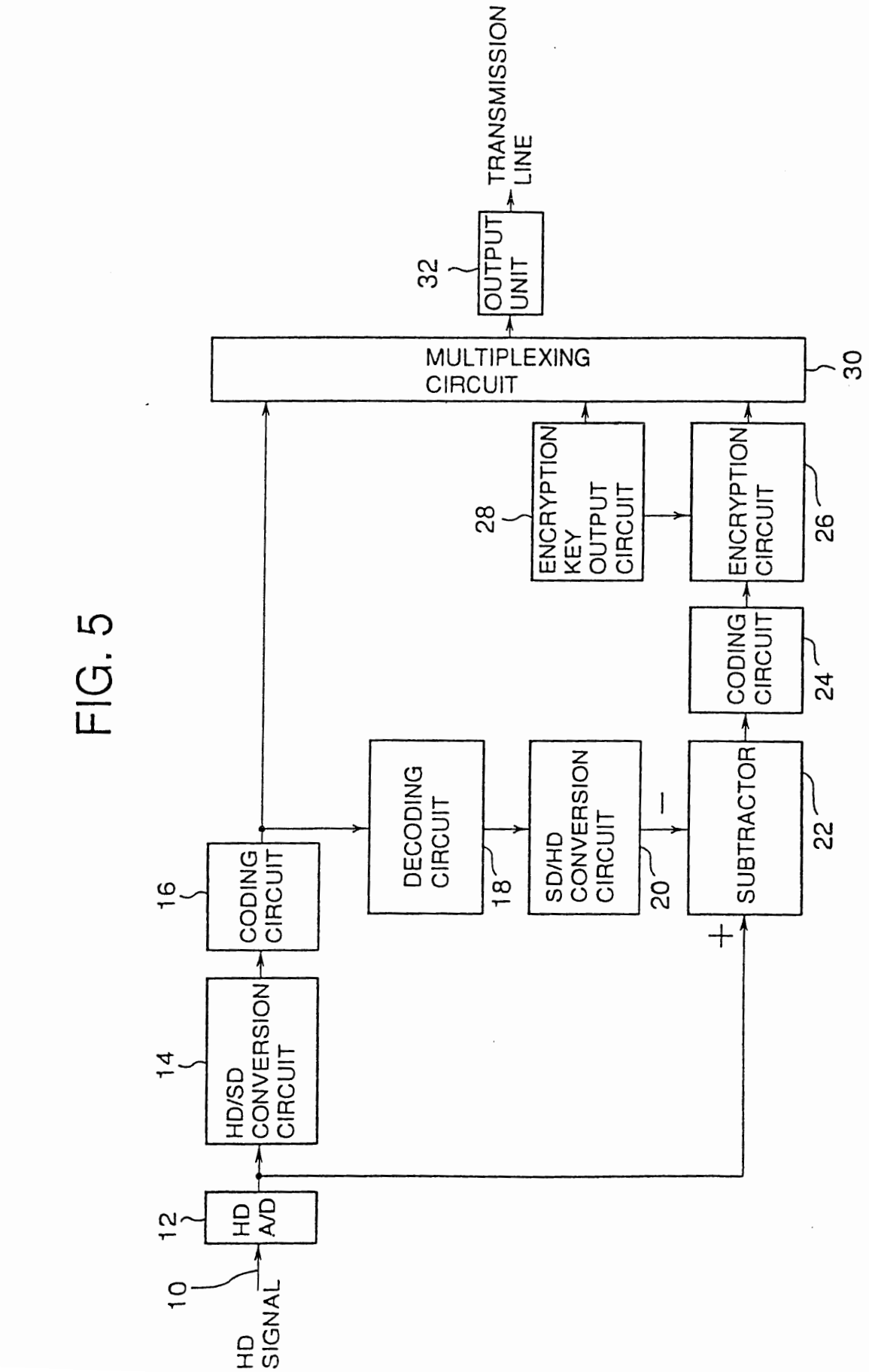

HD SIGNAL
10
HD A/D
12
HD/SD CONVERSION CIRCUIT
14
CODING CIRCUIT
16
DECODING CIRCUIT
18
SD/HD CONVERSION CIRCUIT
20
SUBTRACTOR
22
CODING CIRCUIT
24
ENCRYPTION CIRCUIT
26
ENCRYPTION KEY OUTPUT CIRCUIT
28
MULTIPLEXING CIRCUIT
30
OUTPUT UNIT
32
TRANSMISSION LINE
+
−

FIG. 6

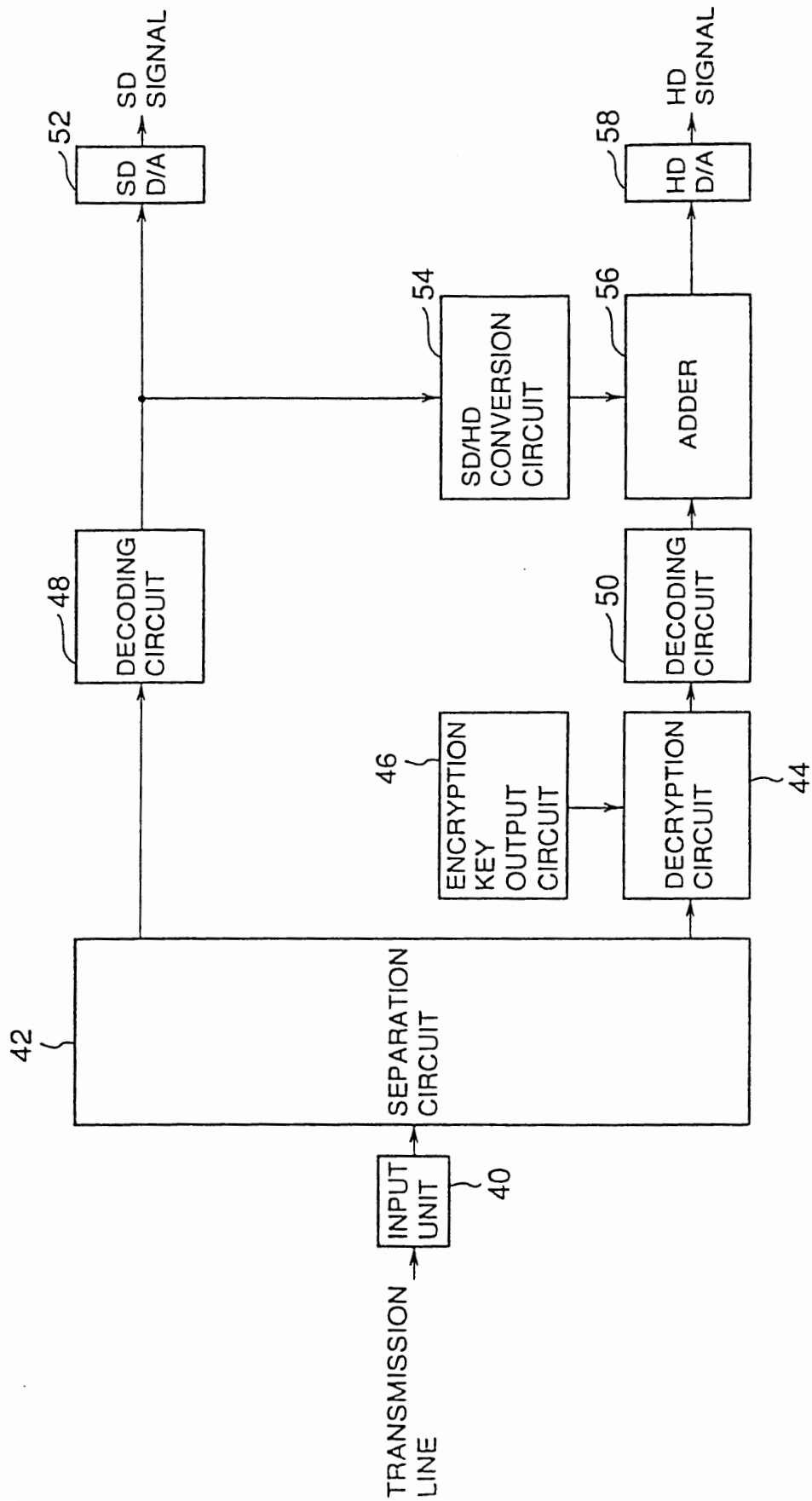

TRANSMISSION LINE
INPUT UNIT
40
SEPARATION CIRCUIT
42
DECODING CIRCUIT
48
SD D/A
52
SD SIGNAL
ENCRYPTION KEY OUTPUT CIRCUIT
46
DECRYPTION CIRCUIT
44
DECODING CIRCUIT
50
SD/HD CONVERSION CIRCUIT
54
ADDER
56
HD D/A
58
HD SIGNAL

FIG. 7

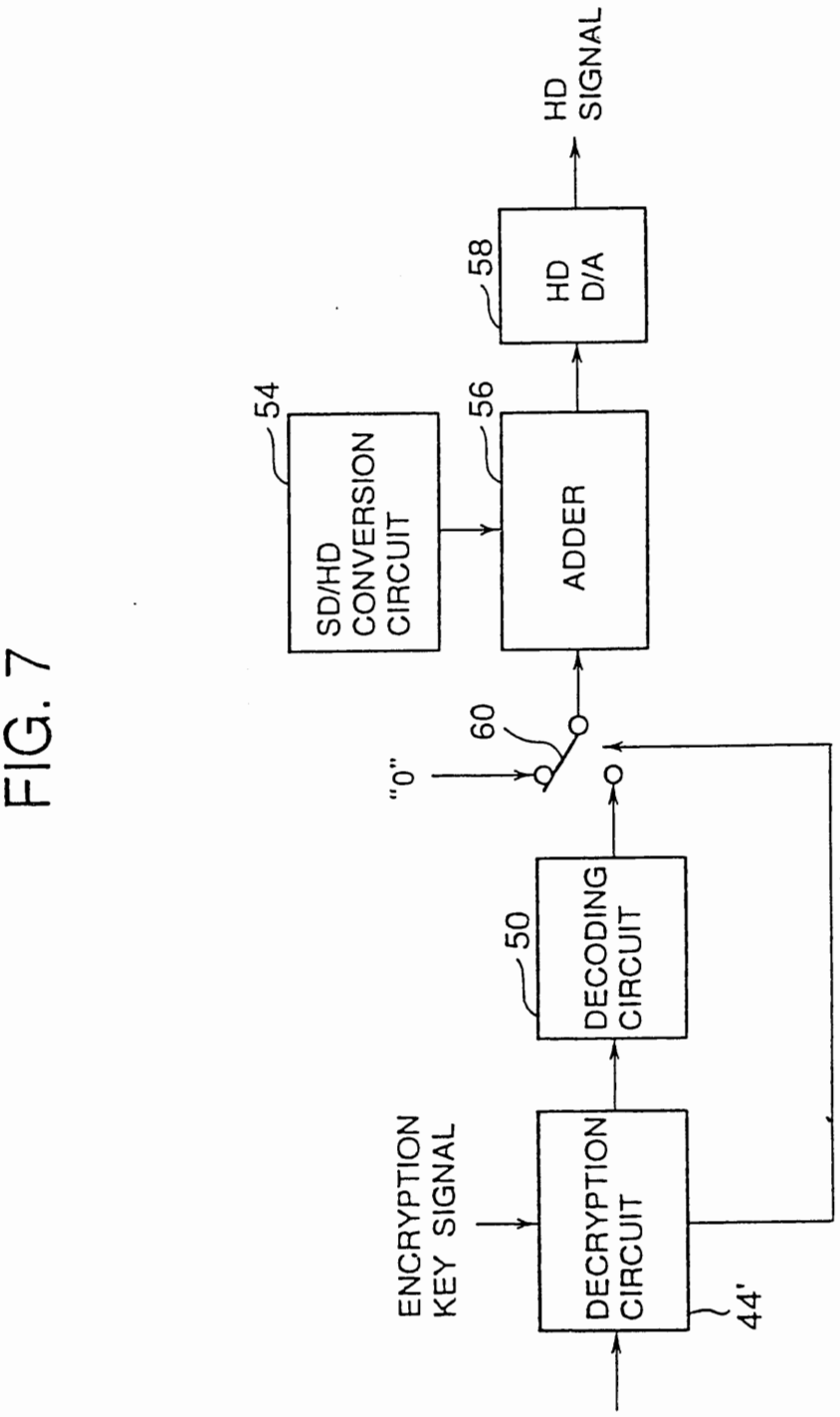

ENCRYPTION KEY SIGNAL
DECRYPTION CIRCUIT
44'
DECODING CIRCUIT
50
"0"
60
ADDER
56
SD/HD CONVERSION CIRCUIT
54
HD D/A
58
HD SIGNAL

FIG. 8

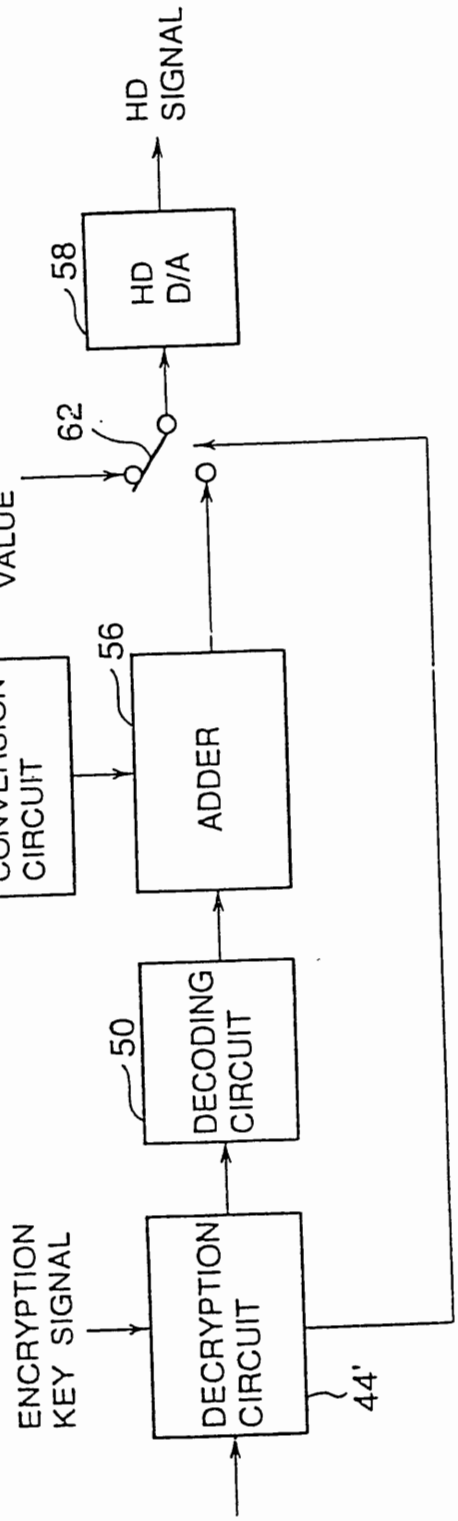

ENCRYPTION KEY SIGNAL
DECRYPTION CIRCUIT
44'
DECODING CIRCUIT
50
ADDER
56
SD/HD CONVERSION CIRCUIT
54
"PREDETERMINED VALUE"
62
HD D/A
58
HD SIGNAL

FIG. 9

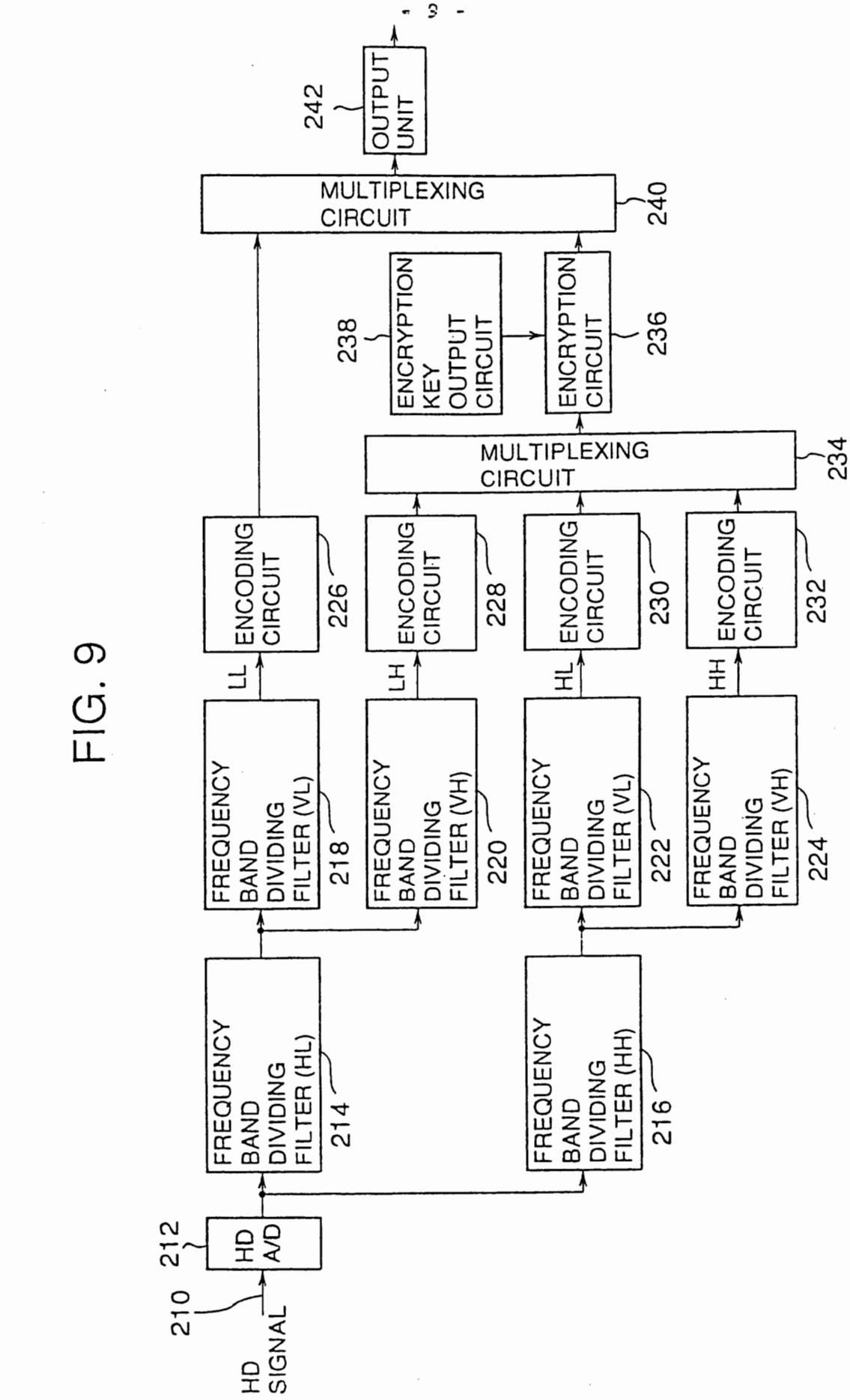

HD SIGNAL
210
212
HD A/D
FREQUENCY BAND DIVIDING FILTER (HL)
214
FREQUENCY BAND DIVIDING FILTER (VL)
218
FREQUENCY BAND DIVIDING FILTER (VH)
220
FREQUENCY BAND DIVIDING FILTER (HH)
216
FREQUENCY BAND DIVIDING FILTER (VL)
222
FREQUENCY BAND DIVIDING FILTER (VH)
224
LL
LH
HL
HH
ENCODING CIRCUIT
226
ENCODING CIRCUIT
228
ENCODING CIRCUIT
230
ENCODING CIRCUIT
232
MULTIPLEXING CIRCUIT
234
ENCRYPTION KEY OUTPUT CIRCUIT
238
ENCRYPTION CIRCUIT
236
MULTIPLEXING CIRCUIT
240
OUTPUT UNIT
242

FIG. 10

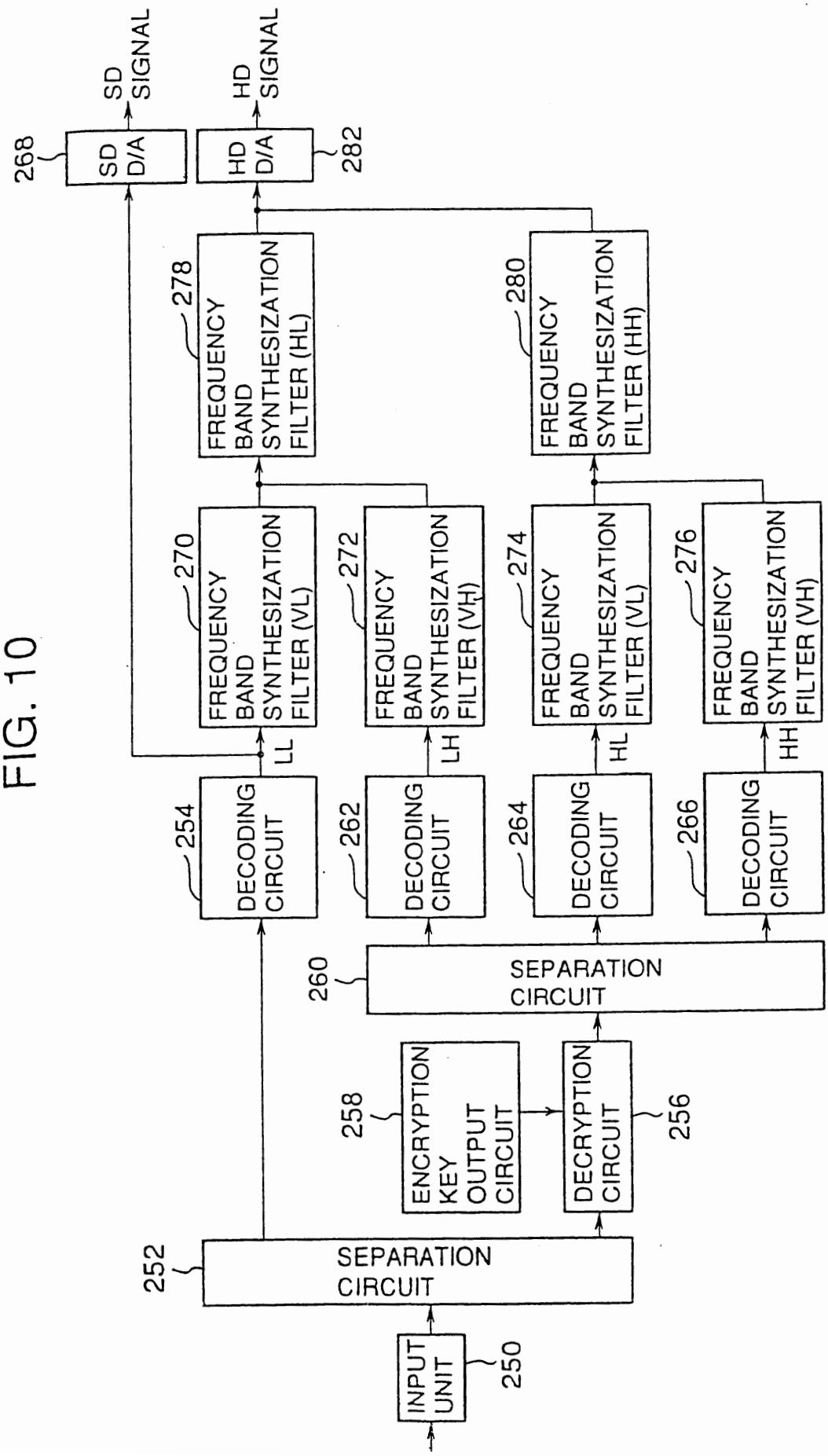

INPUT UNIT
250
SEPARATION CIRCUIT
252
ENCRYPTION KEY OUTPUT CIRCUIT
258
DECRYPTION CIRCUIT
256
SEPARATION CIRCUIT
260
DECODING CIRCUIT
254
DECODING CIRCUIT
262
DECODING CIRCUIT
264
DECODING CIRCUIT
266
LL
LH
HL
HH
FREQUENCY BAND SYNTHESIZATION FILTER (VL)
270
FREQUENCY BAND SYNTHESIZATION FILTER (VH)
272
FREQUENCY BAND SYNTHESIZATION FILTER (VL)
274
FREQUENCY BAND SYNTHESIZATION FILTER (VH)
276
FREQUENCY BAND SYNTHESIZATION FILTER (HL)
278
FREQUENCY BAND SYNTHESIZATION FILTER (HH)
280
SD D/A
268
HD D/A
282
SD SIGNAL
HD SIGNAL

FIG. 11

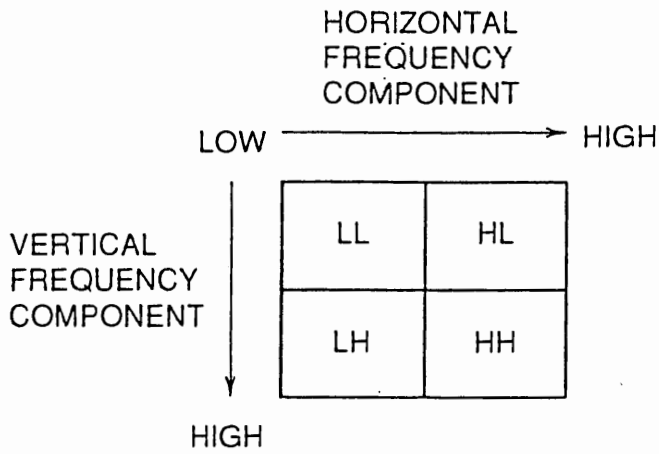

HORIZONTAL
FREQUENCY
COMPONENT
LOW
HIGH
VERTICAL
FREQUENCY
COMPONENT
LL
HL
LH
HH
HIGH

FIG. 12

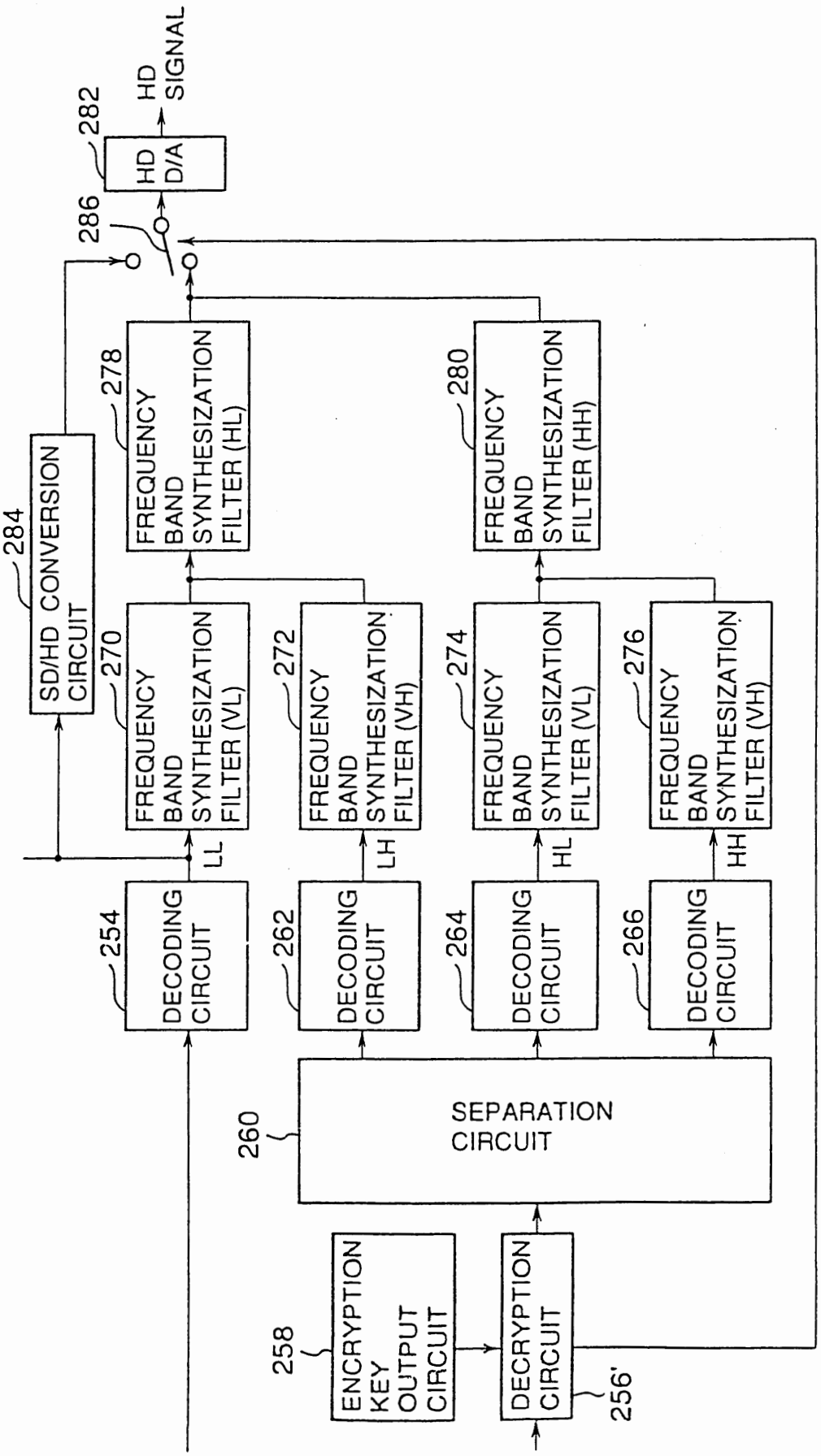

ENCRYPTION KEY OUTPUT CIRCUIT
258
DECRYPTION CIRCUIT
256'
SEPARATION CIRCUIT
260
DECODING CIRCUIT
254
DECODING CIRCUIT
262
DECODING CIRCUIT
264
DECODING CIRCUIT
266
LL
LH
HL
HH
FREQUENCY BAND SYNTHESIZATION FILTER (VL)
270
FREQUENCY BAND SYNTHESIZATION FILTER (VH)
272
FREQUENCY BAND SYNTHESIZATION FILTER (VL)
274
FREQUENCY BAND SYNTHESIZATION FILTER (VH)
276
SD/HD CONVERSION CIRCUIT
284
FREQUENCY BAND SYNTHESIZATION FILTER (HL)
278
FREQUENCY BAND SYNTHESIZATION FILTER (HH)
280
286
HD D/A
282
HD SIGNAL

FIG. 13

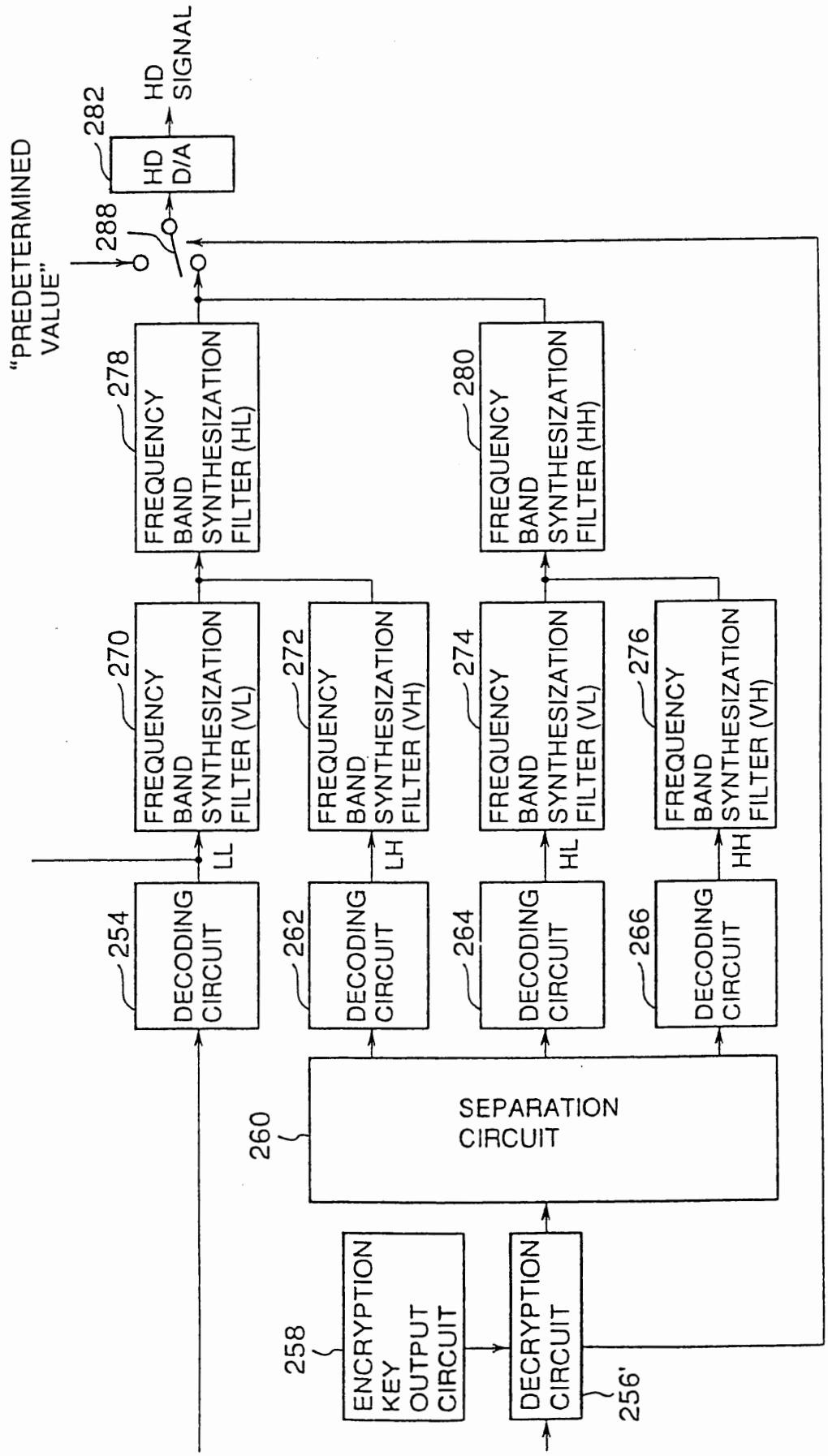

"PREDETERMINED VALUE"
288
282
HD D/A
HD SIGNAL
278
FREQUENCY BAND SYNTHESIZATION FILTER (HL)
280
FREQUENCY BAND SYNTHESIZATION FILTER (HH)
270
FREQUENCY BAND SYNTHESIZATION FILTER (VL)
272
FREQUENCY BAND SYNTHESIZATION FILTER (VH)
274
FREQUENCY BAND SYNTHESIZATION FILTER (VL)
276
FREQUENCY BAND SYNTHESIZATION FILTER (VH)
LL
LH
HL
HH
254
DECODING CIRCUIT
262
DECODING CIRCUIT
264
DECODING CIRCUIT
266
DECODING CIRCUIT
260
SEPARATION CIRCUIT
258
ENCRYPTION KEY OUTPUT CIRCUIT
DECRYPTION CIRCUIT
256'

FIG. 14

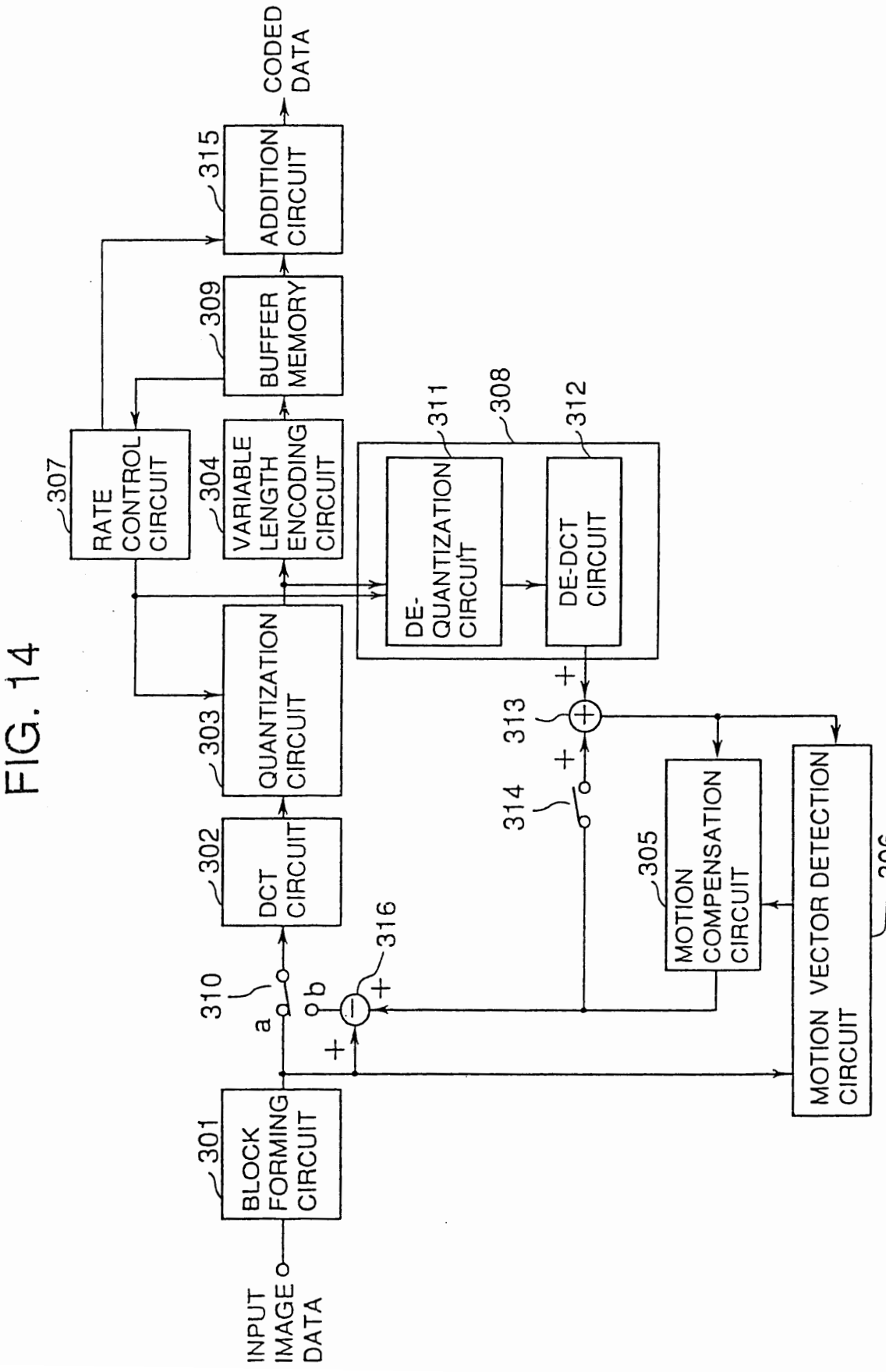
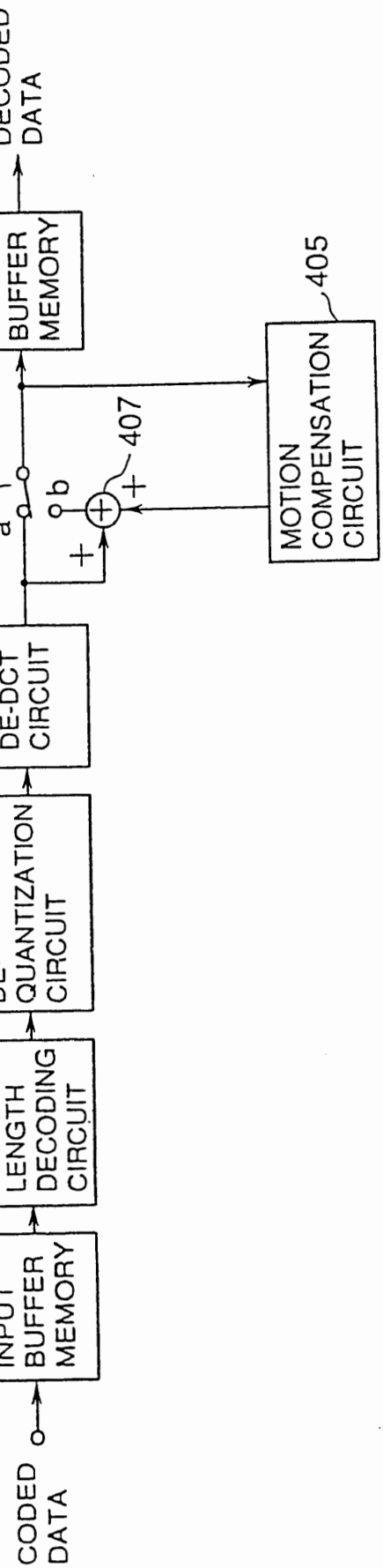

INPUT IMAGE DATA
301 BLOCK FORMING CIRCUIT
310
a
b
302 DCT CIRCUIT
303 QUANTIZATION CIRCUIT
316
307 RATE CONTROL CIRCUIT
304 VARIABLE LENGTH ENCODING CIRCUIT
309 BUFFER MEMORY
315 ADDITION CIRCUIT
CODED DATA
308
311 DE-QUANTIZATION CIRCUIT
312 DE-DCT CIRCUIT
313
314
305 MOTION COMPENSATION CIRCUIT
306 MOTION VECTOR DETECTION CIRCUIT

FIG. 15


CODED DATA
401
INPUT BUFFER MEMORY
402
VARIABLE LENGTH DECODING CIRCUIT
403
DE-QUANTIZATION CIRCUIT
404
DE-DCT CIRCUIT
408
a
b
407
+
+
406
OUTPUT BUFFER MEMORY
DECODED DATA
405
MOTION COMPENSATION CIRCUIT