CLAIMS

1. A device, comprising:

a middle well comprising a fluidic tunnel;

a cis well associated with a cis electrode, wherein a first nanoscale opening is disposed between the cis well and the middle well;

a trans well associated with a trans electrode, wherein a second nanoscale opening is disposed between the trans well and the middle well; and

a field effect transistor (FET) positioned between the first nanoscale opening and the second nanoscale opening, the FET comprising:

a source, a drain, and a channel connecting the source to the drain, wherein the channel comprises a gate oxide layer having an upper surface fluidically exposed to the middle well,

wherein the middle well fluidically connects the cis well to the trans well, and wherein the fluidic tunnel extends through the channel.

2. A device, comprising:

a middle well comprising a fluidic tunnel;

a cis well associated with a cis electrode, wherein a first nanoscale opening is disposed between the cis well and the middle well;

a trans well associated with a trans electrode, wherein a second nanoscale opening is disposed between the trans well and the middle well; and

a field effect transistor (FET) positioned between the first nanoscale opening and the second nanoscale opening, the FET comprising:

a source, a drain, and a channel connecting the source to the drain, wherein the channel comprises a gate oxide layer having an upper surface and a lower surface, the surfaces fluidically exposed to the middle well,

wherein the middle well fluidically connects the cis well to the trans well, and wherein the fluidic tunnel extends through the channel.

3. A device, comprising:

a middle well comprising a fluidic tunnel;

a cis well associated with a cis electrode, wherein a first nanoscale opening is disposed between the cis well and the middle well;

a trans well associated with a trans electrode, wherein a porous structure is disposed between the trans well and the middle well; and

a field effect transistor (FET) positioned between the first nanoscale opening and the porous structure, the FET comprising:

a source, a drain, and a channel connecting the source to the drain, wherein the channel comprises a gate oxide layer having an upper surface fluidically exposed to the middle well,

wherein the middle well fluidically connects the cis well to the trans well, and wherein the fluidic tunnel extends through the channel.

4. A device, comprising:

a middle well comprising a fluidic tunnel;

a cis well associated with a cis electrode, wherein a first nanoscale opening is disposed between the cis well and the middle well;

a trans well associated with a trans electrode, wherein a second nanoscale opening is disposed between the trans well and the middle well; and

a field effect transistor (FET) positioned between the first nanoscale opening and the second nanoscale opening, the FET comprising:

a source, a drain, and a channel connecting the source to the drain, wherein the channel comprises a gate oxide layer having an upper surface fluidically exposed to the middle well,

wherein the middle well fluidically connects the cis well to the trans well, and wherein the fluidic tunnel does not extend through the channel.

5. A device, comprising:

a middle well comprising a fluidic tunnel;

a cis well associated with a cis electrode, wherein a first nanoscale opening is disposed between the cis well and the middle well;

a trans well associated with a trans electrode, wherein a second nanoscale opening is disposed between the trans well and the middle well; and

a field effect transistor (FET) positioned between the first nanoscale opening and the second nanoscale opening, the FET comprising:

a source, a drain, and a channel connecting the source to the drain, wherein the channel comprises a gate oxide layer having an upper surface and a lower surface, the surfaces fluidically exposed to the middle well,

wherein the middle well fluidically connects the cis well to the trans well, and wherein the fluidic tunnel does not extend through the channel.

6. A device, comprising:

a middle well comprising a fluidic tunnel;

a cis well associated with a cis electrode, wherein a first nanoscale opening is disposed between the cis well and the middle well;

a trans well associated with a trans electrode, wherein a porous structure is disposed between the trans well and the middle well; and

a field effect transistor (FET) positioned between the first nanoscale opening and the porous structure, the FET comprising:

a source, a drain, and a channel connecting the source to the drain, wherein the channel comprises a gate oxide layer having an upper surface fluidically exposed to the middle well,

wherein the middle well fluidically connects the cis well to the trans well, and wherein the fluidic tunnel does not extend through the channel.

7. The device as defined in any of claims 1-6, wherein the FET is a nanowire transistor.

8. The device as defined in claim 7, wherein the channel has a length along a direction from the source to the drain, a height along a direction from the cis electrode to the trans electrode, and a width along a direction at least substantially orthogonal to both the length and the height, and wherein the length is at least about 10 times the width or the height.

9. The device as defined in claim 8, wherein an intersection between the fluidic tunnel and the channel in a plane defined by the length and the width is disc shaped.

10. The device as defined in any of claims 1-6, wherein the FET is a nanosheet transistor.

11. The device as defined in claim 10, wherein the channel has a length along a direction from the source to the drain, a height along a direction from the cis electrode to the trans electrode, and a width along a direction at least partially orthogonal to both the length and the height, wherein the length is at least about 5 times the height, and wherein the width is at least about 5 times the height.

12. The device as defined in claim 11, wherein an intersection between the fluidic tunnel and the channel in a plane defined by the length and the width is oblong shaped.

13. The device as defined in any of claims 1-6, wherein the FET further comprises a plurality of channels, wherein each of the plurality of channels comprises a gate oxide layer having an upper surface and a lower surface fluidically exposed to the middle well, and wherein the fluidic tunnel extends through each of the plurality of channels.

14. The device as defined in claim 3 or claim 6, wherein the porous structure comprises a SiCOH film.

15. The device as defined in any of claims 1-6, further comprising a membrane positioned between the cis well and the middle well, wherein the first nanoscale opening extends through the membrane.

16. The device as defined in claim 15, wherein the membrane is selected from the group consisting of a lipid and a biomimetic equivalent of a lipid.

17. The device as defined in claim 15, wherein the first nanoscale opening extends through: a polynucleotide nanopore; a polypeptide nanopore; or a carbon nanotube, disposed in the membrane.

18. The device as defined in claim 15, wherein the membrane is a synthetic membrane, and wherein the first nanoscale opening is a solid-state nanopore.

19. The device as defined in any of claims 1-6, wherein the device comprises a nanopore sequencer.

20. The device as defined in any of claims 1-6, wherein the gate oxide layer has a thickness between about 1 to about 10 nm.

21. The device as defined in any of claims 1-6, wherein the gate oxide layer has a thickness between about 2 and about 4 nm.

22. The device as defined in claims 1, 2, or 3, wherein the gate oxide layer further comprises a vertical surface fluidically exposed to the fluidic tunnel.

23. An array of a plurality of the nanopore sequencers as defined in claim 19, wherein:

each of the plurality of the nanopore sequencers shares a common cis electrode and a common trans electrode; or

each of the plurality of the nanopore sequencers has a distinct cis electrode and a distinct trans electrode; or

each of the plurality of the nanopore sequencers shares a common cis electrode and has a distinct trans electrode; or

each of the plurality of the nanopore sequencers has a distinct cis electrode and shares a common trans electrode.

24. A device, comprising:

a middle well;

a cis well associated with a cis electrode, wherein a first nanoscale opening is disposed between the cis well and the middle well;

a trans well associated with a trans electrode, wherein a second nanoscale opening is disposed between the trans well and the middle well; and

a field effect transistor (FET) positioned between the first nanoscale opening and the second nanoscale opening, the FET comprising:

a source, a drain, and a channel connecting the source to the drain, wherein the source, drain and channel are vertically stacked, and wherein the

channel comprises a gate oxide layer having a vertical surface fluidically exposed to the middle well,

wherein the middle well fluidically connects the cis well to the trans well, and

wherein the vertical direction is a direction from the cis electrode to the trans electrode.

25. A device, comprising:

a middle well;

a cis well associated with a cis electrode, wherein a first nanoscale opening is disposed between the cis well and the middle well;

a trans well associated with a trans electrode, wherein a porous structure is disposed between the trans well and the middle well; and

a field effect transistor (FET) positioned between the first nanoscale opening and the porous structure, the FET comprising:

a source, a drain, and a channel connecting the source to the drain, wherein the source, drain and channel are vertically stacked, and wherein the channel comprises a gate oxide layer having a vertical surface fluidically exposed to the middle well,

wherein the middle well fluidically connects the cis well to the trans well, and

wherein the vertical direction is a direction from the cis electrode to the trans electrode.

26. The device as defined in any of claims 24 or 25, wherein the FET is a nanowire transistor.

27. The device as defined in any of claims 24 or 25, wherein the FET is a nanosheet transistor.

28. The device as defined in any of claims 24 or 25, wherein the FET further comprises a plurality of channels, wherein each of the plurality of channels comprises a gate oxide layer having two additional vertical surfaces fluidically exposed to the middle well.

29. The device as defined in claim 25, wherein the porous structure comprises a SiCOH film.

30. The device as defined in any of claims 24 or 25, further comprising a membrane positioned between the cis well and the middle well, wherein the first nanoscale opening extends through the membrane.

31. The device as defined in claim 30, wherein the membrane is selected from the group consisting of a lipid and a biomimetic equivalent of a lipid.

32. The device as defined in claim 30, wherein the first nanoscale opening extends through: a polynucleotide nanopore; a polypeptide nanopore; or a carbon nanotube, disposed in the membrane.

33. The device as defined in claim 30, wherein the membrane is a synthetic membrane, and wherein the first nanoscale opening is a solid-state nanopore.

34. The device as defined in any of claims 24 or 25, wherein the gate oxide layer has a thickness between about 1 to about 10 nm.

35. The device as defined in any of claims 24 or 25, wherein the gate oxide layer has a thickness between about 2 and about 4 nm.

36. The device as defined in any of claims 24 or 25, wherein the device comprises a nanopore sequencer.

37. An array of a plurality of the nanopore sequencers as defined in claim 36, wherein:

each of the plurality of the nanopore sequencers shares a common cis electrode and a common trans electrode; or

each of the plurality of the nanopore sequencers has a distinct cis electrode and a distinct trans electrode; or

each of the plurality of the nanopore sequencers shares a common cis electrode and has a distinct trans electrode; or

each of the plurality of the nanopore sequencers has a distinct cis electrode and shares a common trans electrode.

38. A device, comprising:

a middle well;

a cis well associated with a cis electrode, wherein a first nanoscale opening is disposed between the cis well and the middle well;

a trans well associated with a trans electrode, wherein a second nanoscale opening is disposed between the trans well and the middle well; and

a field effect transistor (FET) positioned between the first nanoscale opening and the second nanoscale opening, the FET comprising:

a source, a drain, and a channel connecting the source to the drain, wherein the channel comprises a gate oxide layer operably connected to a metal structure,

wherein the middle well fluidically connects the cis well to the trans well, and

wherein the metal structure has at least one surface fluidically exposed to the middle well.

39. A device, comprising:

a middle well;

a cis well associated with a cis electrode, wherein a first nanoscale opening is disposed between the cis well and the middle well;

a trans well associated with a trans electrode, wherein a porous structure is disposed between the trans well and the middle well; and

a field effect transistor (FET) positioned between the first nanoscale opening and the porous structure, the FET comprising:

a source, a drain, and a channel connecting the source to the drain, wherein the channel comprises a gate oxide layer operably connected to a metal structure,

wherein the middle well fluidically connects the cis well to the trans well, and

wherein the metal structure has at least one surface fluidically exposed to the middle well.

40. The device as defined in any of claims 38 or 39, wherein the gate oxide layer is not fluidically exposed.

41. The device as defined in any of claims 38 or 39, wherein the at least one fluidically exposed surface of the metal structure is formed of a corrosion-resistant material.

42. The device as defined in any of claims 38 or 39, wherein the metal structure has at least one partially vertical surface, least two partially vertical surfaces, at least one partially horizontal surface, at least two partially horizontal surfaces, or any combination thereof, fluidically exposed to the middle well, wherein the vertical direction is a direction from the cis electrode to the trans electrode, and wherein the horizontal direction is orthogonal to the vertical direction.

43. The device as defined in any of claims 38 or 39, wherein the metal structure has at least one cup-shaped substructure fluidically exposed to the middle well.

44. The device as defined in any of claims 38 or 39, wherein the portion of the metal structure fluidically exposed to the middle well comprises at least one hole or opening.

45. The device as defined in any of claims 38 or 39, wherein the portion of the metal structure fluidically exposed to the middle well comprises at least two holes or openings.

46. The device as defined in any of claims 38 or 39, wherein the FET is a nanowire transistor.

47. The device as defined in claim 46, wherein the channel has a length along a direction from the source to the drain, a height along a direction at least partially orthogonal to the length, and a width along a direction at least partially orthogonal to both the length and the height, wherein the length is at least about 10 times the width or the height.

48. The device as defined in any of claims 38 or 39, wherein the FET is a nanosheet transistor.

49. The device as defined in claim 48, wherein the channel has a length along a direction from the source to the drain, a height along a direction at least substantially

orthogonal to the length, and a width along a direction at least partially orthogonal to both the length and the height, wherein the length is at least about 5 times the height, and wherein the width is at least about 5 times the height.

50. The device as defined in claim 39, wherein the porous structure comprises a SiCOH film.

51. The device as defined in any of claims 38 or 39, further comprising a membrane positioned between the cis well and the middle well, wherein the first nanoscale opening extends through the membrane.

52. The device as defined in claim 51, wherein the membrane is selected from the group consisting of a lipid and a biomimetic equivalent of a lipid.

53. The device as defined in claim 51, wherein the first nanoscale opening extends through: a polynucleotide nanopore; a polypeptide nanopore; or a carbon nanotube, disposed in the membrane.

54. The device as defined in claim 51, wherein the membrane is a synthetic membrane, and wherein the first nanoscale opening is a solid-state nanopore.

55. The device as defined in any of claims 38 or 39, wherein the gate oxide layer has a thickness between about 1 to about 10 nm.

56. The device as defined in any of claims 38 or 39, wherein the gate oxide layer has a thickness between about 2 and about 4 nm.

57. The device as defined in any of claims 38 or 39, wherein the device comprises a nanopore sequencer.

58. An array of a plurality of the nanopore sequencers as defined in claim 57, wherein:

each of the plurality of the nanopore sequencers shares a common cis electrode and a common trans electrode; or

each of the plurality of the nanopore sequencers has a distinct cis electrode and a distinct trans electrode; or

each of the plurality of the nanopore sequencers shares a common cis electrode and has a distinct trans electrode; or

each of the plurality of the nanopore sequencers has a distinct cis electrode and shares a common trans electrode.