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ABSTRACT

A Viterbi detector is modified to reduce its implementation complexity. A partial-response signal may be viewed as a sequence of expected samples generated from a finite-state-machine model. In a typical Viterbi demodulator implemented using the add, compare, select (ACS) method, each state in the expected sample sequence model is associated with a hardware module to perform the functions of adding new branch error metrics to path error metrics, comparing path error metrics, and selecting the path having the lowest path error metric. In this invention, an ACS module may have two or more sequence-model states dynamically associated with it, such that at some times one sequence-model state is associated with it and at other times another sequence-model state is associated with it. This reduces the number of ACS modules required and also reduces the size/complexity of the demodulator's path memories which must store one path for each ACS module. Groups of sequence-model states may be chosen to share an ACS module without significant loss in performance as compared to the original, unreduced Viterbi demodulator. The invention supports a wide range of sample models by making the expected sample sequence of an isolated medium transition programmable. The invention reduces the speed at which the detector circuitry must operate relative to the sample rate by allowing multiple samples to be processed simultaneously. Several reduced detectors for specific sample sequence models are presented for particular applications. The

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invention is applicable to other types of viterbi detectors, such as decoders for convolutional codes.

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