METHOD OF ENCAPSULATING THIN SEMICONDUCTOR CHIP-SCALE PACKAGES

ABSTRACT

An apparatus for the fabrication of a semiconductor device comprising: a mold having top and bottom halves, each with cavities for holding semiconductor chips pre-assembled on an electrically insulating interposer; one of said halves having a plurality of runners and a plurality of gates for feeding encapsulation material into said cavities; said plurality of runners comprising pairs of runners parallel to each other, having gates opposite to each other, thereby forming dual gates; each pair of runners being configured such that encapsulation material will exit from adjacent gates concurrently; and each pair of dual gates being structured such that they fill the cavity between them uniformly with encapsulation material, thereby encapsulating thin semiconductor devices.

Figure 11