WHAT IS CLAIMED IS:

1. A method, comprising:

coupling a known signal to an impedance;

observing a current through the impedance for a number of cycles to establish a first average current corresponding to a time related parameter of the known signal;

coupling an unknown periodic signal to the impedance;

observing the current through the impedance for a number of cycles to establish a second average current corresponding to a time related parameter of the unknown periodic signal; and

determining a timing characteristic of the unknown signal by comparing the first and second currents.

2. The method of claim 1, wherein the known signal is a clock signal with a known frequency.

3. The method of claim 1, wherein the impedance is a linear impedance.

4. The method of claim 3, wherein the impedance is a resistor.

5. The method of claim 1, wherein the impedance is a non-linear impedance.

6. The method of claim 1, wherein the known signal is a DC voltage.

7. The method of claim 1, wherein the known signal is a time varying periodic signal of a fixed duty cycle.

8. The method of claim 1, wherein determining a timing characteristic by comparing further comprises taking a ratio of the first and second currents.

9. An apparatus, comprising:

an impedance having an input for selectively receiving a time varying periodic signal or a known voltage signal; and

a current output coupled to the impedance;

wherein an active time of the time varying periodic signal is determined by evaluating a ratio of a first average current observed at the current output while the time varying periodic signal is coupled to the input of the impedance to a second average current observed at the current output while the known voltage signal is coupled to the input of the impedance.

10. The apparatus of claim 9, wherein the known voltage signal is a DC voltage.

11. The apparatus of claim 9, wherein the known voltage signal is a known clock signal.

12. The apparatus of claim 9, wherein the time varying periodic signal is a clock signal of unknown duty cycle.

13. The apparatus of claim 12, wherein the duty cycle for the clock signal is determined by multiplying the ratio of the first average current to the second average current by the time duration for a single clock period.

14. The apparatus of claim 9, and further comprising a time to current converter, comprising:

a first logic gate for receiving a clock input and a delayed clock input and having an output corresponding to the overlap time of the clock input and the delayed clock input; and

a second logic gate for receiving the output of the first logic gate and a DC input, and having an output coupled to the impedance;

wherein the time varying periodic signal is input to the clock input and to the delayed clock input.

15. The apparatus of claim 9, wherein the impedance comprises a resistor.

16. A method, comprising:

providing an impedance having an input and a current output;

coupling a known signal to the impedance;

measuring a first current that is an average current through the impedance over a number of clock cycles;

coupling a time varying periodic signal of unknown timing characteristics to the impedance;

measuring a second current that is the average current through the impedance due to the time varying periodic signal over a number of cycles; and

determining at least one unknown timing characteristic of the time varying periodic signal by forming a ratio of the second current to the first current and multiplying the ratio by the time duration of a clock period;

wherein the at least one unknown timing characteristic includes one selected from a group consisting essentially of a duty cycle, frequency, and a delay.

17. The method of claim 16, wherein providing the impedance comprises providing a linear impedance.

18. The method of claim 16, wherein providing the impedance comprises providing a resistor formed on an integrated circuit.

19. The method of claim 16, and further comprising:

coupling a clock signal of a known duty cycle to a first input of a logic gate;

coupling an inverted form of the clock signal to a device under test;

receiving a delayed clock signal from the device under test and coupling the delayed clock signal to a second input of the logic gate; and

coupling the output of the logic gate to the impedance.

20. The method of claim 19, and further comprising:

measuring a first average current in the impedance over a clock period of the clock signal, the current responsive to an output of the logic gate when the clock signal and the delayed clock signal overlap; and

determining the delay in the device under test by calculating a ratio of the first average current to a second average current measured in the impedance from a DC level voltage over a clock period.

WHAT IS CLAIMED IS:

1. A method, comprising:

coupling a known signal to an impedance through a first logic element;

observing a first current through the impedance for a number of cycles to establish a first average current corresponding to a time related parameter of the known signal;

inverting a first clock signal to generate an inverted first clock signal;

delaying the first clock signal to generate a delayed first clock signal, the delay of the delayed first clock signal corresponding to a delay created by inverting the first clock signal;

generating a delayed signal by passing the inverted first clock signal through a device under test;

generating an unknown periodic signal by logically combining the delayed signal with the delayed first clock signal, the unknown periodic signal having a logical "on" state indicating a non-overlapping time of the delayed signal compared to the delayed first clock signal;

coupling the unknown periodic signal to the impedance through the first logic element, the first logic element selectively providing the unknown periodic signal or the known signal to the impedance;

observing a second current through the impedance for a number of cycles to establish a second average current corresponding to a time related parameter of the unknown periodic signal; and

determining a timing characteristic of the unknown signal by comparing the first and second currents, the timing characteristic being determined independent of the physical value of the impedance.

2. The method of claim 1, wherein the known signal is a clock signal with a known frequency.

3. The method of claim 1, wherein the impedance is a linear impedance.

4. The method of claim 3, wherein the impedance is a resistor.

5. The method of claim 1, wherein the impedance is a non-linear impedance.

6. The method of claim 1, wherein the known signal is a DC voltage.

7. The method of claim 1, wherein the known signal is a time varying periodic signal of a fixed duty cycle.

8. The method of claim 1, wherein determining a timing characteristic by comparing further comprises taking a ratio of the first and second currents.

9. An apparatus, comprising:

a time to current converter, comprising:

a first logic gate for receiving a delayed signal from a device under test and a delayed clock input, the first logic gate outputting a time varying periodic signal having a high logic state corresponding to the non-overlapping time of the high logic states of delayed signal and the delayed clock input; and

a second logic gate coupled at a first input to the output of the first logic gate and coupled at a second input to a known voltage signal input;

an impedance having an input coupled to the output of the second logic gate for selectively receiving the time varying periodic signal or a known voltage signal; and

a current output coupled to the impedance;

wherein an active time of the time varying periodic signal is determined by evaluating a ratio of a first average current observed at the current output while the time varying periodic signal is coupled to the input of the impedance to a second average current observed at the current output while the known voltage signal is coupled to the input of the impedance.

10. The apparatus of claim 9, wherein the known voltage signal is a DC voltage.

11. The apparatus of claim 9, wherein the known voltage signal is a known clock signal.

12. The apparatus of claim 9, wherein the time varying periodic signal is a clock signal of unknown duty cycle.

13. The apparatus of claim 12, wherein the duty cycle for the clock signal is determined by multiplying the ratio of the first average current to the second average current by the time duration for a single clock period.

14. The apparatus of Claim 9, wherein the known voltage signal is a DC voltage signal.

15. The apparatus of claim 9, wherein the impedance comprises a resistor.

16. A method, comprising:

providing an impedance having an input and a current output;

coupling a known signal to the impedance;

measuring a first current that is an average current through the impedance over a number of clock cycles;

coupling an inverted form of a clock signal having a known duty cycle to a device under test;

coupling a delayed clock signal to a first input of a logic gate, the delayed clock signal being a delayed form of the clock signal, a delay of the delayed clock signal matching the delay of the inverted form of the clock signal;

receiving a test signal from the device under test and coupling the test signal to a second input of the logic gate;

generating a time varying periodic signal of unknown timing characteristics with the logic gate by logically combining the test signal with the delayed clock signal;

coupling the time varying periodic signal of unknown timing characteristics to the impedance;

measuring a second current that is the average current through the impedance due to the time varying periodic signal over a number of cycles; and

determining at least one unknown timing characteristic of the time varying periodic signal by forming a ratio of the second current to the first current and multiplying the ratio by the time duration of a clock period;

wherein the at least one unknown timing characteristic includes one selected from a group consisting essentially of a duty cycle, frequency, and a delay.

17. The method of claim 16, wherein providing the impedance comprises providing a linear impedance.

18. The method of claim 16, wherein providing the impedance comprises providing a resistor formed on an integrated circuit.

19. The method of claim 16, and further comprising:

measuring a first average current in the impedance over a clock period of the clock signal, the current responsive to an output of the logic gate when the clock signal is not overlapped by the delayed clock signal; and

determining the delay in the device under test by calculating a ratio of the first average current to a second average current measured in the impedance from a DC level voltage output by the logic gate over a clock period.

20. The method of Claim 16, wherein the known signal is a DC signal.