**CLAIMS**

1. A manufacturing method of a semiconductor chip stack package, the method comprising:

forming a chip in which an interconnection pad is formed on one surface thereof;

performing hydrophilic surface treatment of an attachment surface of the chip to have a hydrophilic surface;

performing hydrophobic surface treatment of a region of the attachment surface of the chip subjected to the hydrophilic surface treating that does not contact another chip to have a hydrophobic surface;

aligning chips of regions where a hydrophilic surface treated portion is exposed to contact each other;

firstly fixing the chips by applying heat or pressure; and

bonding wires to respective interconnection pads of the aligned chips.

2. The method of claim 1, wherein in the hydrophilic surface treatment, a layer using a hydrophilic material is formed on the attachment surface of the chip.

3. The method of claim 1, wherein the hydrophilic surface treatment is plasma processing.

4. The method of claim 1, wherein in the aligning, water drop is applied to one surface of each of the chips to form a wetting layer, and thereafter the chips contact each other to be self-aligned.

5. The method of claim 1, wherein in the hydrophobic surface treatment, a hydrophobic material is applied to the chip subjected to the hydrophilic surface treatment.

6. The method of claim 5, wherein the hydrophobic material is selected from a group consisting $CF_4$, a self-assembled monolayer (SAM), or polytetrafluoroethylene (PTFE).

7. The method of claim 1, wherein after the firstly fixing the chip, the circumferences of the stacked chips are secondly fixed by using an adhesive.

8. The method of claim 1, wherein the hydrophilic surface treatment to the bonding of the wires is repeatedly performed at a predetermined time.

9. A semiconductor chip stack package, comprising:

a plurality of chips having a plate shape in which an interconnection pad is formed on one surface thereof and having a hydrophilic surface except for a predetermined region where the interconnection pad is formed to be fixed to each other by self-aligning; and

wires connected to the interconnection pads of the chips.

## CLAIMS

1. A manufacturing method of a semiconductor chip stack package, the method comprising:

forming a chip in which an interconnection pad is formed on one surface thereof;

performing hydrophilic surface treatment of an attachment surface of the chip to have a hydrophilic surface;

performing hydrophobic surface treatment of a region of the attachment surface of the chip subjected to the hydrophilic surface treating that does not contact another chip to have a hydrophobic surface, the another chip having an interconnection pad exposed through a hydrophilic surface and being positioned opposite to the interconnection pad of the chip in a direction perpendicular to a stacking direction of the chips;

aligning regions of the chips where a hydrophilic surface treated portion on each chip being partially exposed to contact each other;

firstly fixing the chips; and

bonding wires to respective interconnection pads of the aligned chips.

2. The method of claim 1, wherein in the hydrophilic surface treatment, a layer using a hydrophilic material is formed on the attachment surface of the chip.

3. The method of claim 1, wherein the hydrophilic surface treatment is plasma processing.

4. The method of claim 1, wherein in the aligning, water drop is applied to one surface of each of the chips to form a wetting layer, and thereafter the chips contact each other to be self-aligned.

5. The method of claim 1, wherein in the hydrophobic surface treatment, a hydrophobic material is applied to the chip subjected to the hydrophilic surface treatment.

6. The method of claim 5, wherein the hydrophobic material is selected from a group consisting $CF_4$, a self-assembled monolayer (SAM), or polytetrafluoroethylene (PTFE).

7. The method of claim 1, wherein after the firstly fixing the chips, the circumferences of the stacked chips are secondly fixed by using an adhesive.

8. The method of claim 1, wherein the hydrophilic surface treatment, hydrophobic surface treatment and the bonding of the wires are repeatedly performed for a predetermined duration of time.