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(54) IMPROVEMENTS IN OR RELATING TO CHARGE COUPLED MEMORY DEVICES

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195 Broadway, New York City, New York State, United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to charge coupled memory devices.

Memory devices have been fabricated using an MIS structure in which the storage capacity of each charge storage site is selectively fixed, by adjusting the electrical capacity at each site of the MIS structure, in accordance with input information. With the storage capacity of each site independently fixed, charge can be repeatedly accumulated in the same fixed pattern and as the charge is shifted out, the signal level will correspond to the input information.

These devices in their basic form are a dynamic memory store, although with the incorporation of recirculation and regeneration, the storage duration can be extended to provide an essentially permanent memory feature.

According to the present invention a charge-coupled memory device comprises a semiconducting or insulating or semi-insulating semiconductor body having means associated therewith for effecting storage of charge carriers at discrete storage sites at or near the surface of the body, means which when suitably energised effect transfer of stored charges between storage sites and to a detection site at which the charge magnitude may be detected, in which means are provided individual to at least one selected storage site to control the accumulation of charge carriers at the selected storage site so as to provide the site with a distinct memory function. Thus a memory function is built into each storage site so that

recirculation and regeneration is not necessary.

Memory devices of the present invention may be of one of two forms. In one, the storage capacity of each site is permanently fixed, generally by the structural characteristics of the device, to give a "read only" memory.

In the other are permanent memories in which the storage capacity of the sites can be conveniently adjusted or reprogrammed. The adjustable feature enables these devices, if desired, to be operated in a nonpermanent mode. All of these devices share the common feature that the electrical capacitance of the MIS storage elements is selectively altered. In the usual case it will be preferable to employ parallel readout for these devices although with suitable adjustment of the accumulation and shift potentials, serial readout can be used.

Structures in which the capacitance is permanently fixed include those in which the physical thickness of the insulating layer is varied according to the information programme. Alternatively, at least two (two for digital devices) different insulators are used, different in the sense that they exhibit significantly different dielectric properties. Included under this device concept are homogeneous insulators in which the dielectric strength is locally altered as by selective diffusion or implantation of more, or less, conductive ions.

The electrical capacitance of the individual MIS elements can also be fixed by selecting the properties of the metal. Using metal conductors having different work functions results in storage elements with different capacitances.

Preferred from the standpoint of versatility are those embodiments wherein the storage capacity of the individual sites can be conveniently adjusted with new information. In one such embodiment, floating or dielectrically isolated capacitors are provided at each memory site. Information is shifted into the charge coupled register by normal charge

coupled action and is transferred to the isolated capacitors by a prescribed read-in process. The charge remains in the isolated capacitor as long as desired depending upon the effectiveness of the dielectric isolation. The amount of this charge, in an analogue sense, or the presence or absence of charge, in a digital sense, determines the charge capacity of the storage element. The information in the memory elements can be erased conveniently for reprogramming.

The invention will be more clearly understood from the following detailed description of various embodiments. In the drawing:

Fig. 1 is a front section of a portion of a charge coupled memory device according to one embodiment of this invention;

Figs. 2A and 2B are plan and sectional views of an alternative charge coupled memory device employing parallel coupling;

Fig. 3 is a perspective view of a further embodiment of the invention;

Fig. 4 is a front sectional view of a charge coupled memory device in which the memory is semipermanently fixed;

Fig. 5 is a current-voltage plot describing a property of the insulating barrier between the storage medium and the memory controlling element in the device of Fig. 4; and

Figs. 6A and 6B are plots of the band structure of the memory element of Fig. 4 with and without fixed charge in the memory controlling element.

In the device represented by Fig. 1, a series of conventional charge coupled elements are shown in combination with memory storage elements.

With a three wire drive scheme, as in this device, every third electrode is used for accumulation. The structure includes a semiconductor body 10, an insulating layer 11, metal drive electrodes 12a—12d, 13a—13d, and 14a—14d and their associated conductors 12, 13 and 14. Of the drive electrodes, 12a—12d comprise accumulation stages and provide the memory function. As shown in the figure certain of these, i.e., 12b and 12d, have thick insulating layers 15 additionally provided. Thus the capacitance of these elements is less than that of the elements comprising electrodes 12a and 12c. With a bias on conductor 12, carriers are allowed to accumulate under conductors 12a—12d to their equilibrium value. The accumulation process can be facilitated by several methods. Illuminating the semiconductor body 10 produces an excess of free carrier by photon absorption. Alternatively, carriers can be shifted in by charge coupled action and allowed to equilibrate to the capacity of each element. A similar result is conveniently obtained by driving all elements to avalanche so that carriers are injected at each site. Accumulation also occurs

inherently due to thermal processes. This last mechanism is attractive in its simplicity and is adequate except where very short accumulation periods are required. The accumulated carriers are then shifted out by normal charge coupled action by sequentially biasing conductors 12, 13 and 14. The signal produced by carriers accumulated under electrodes 12a and 12c will be larger than the corresponding signal from elements associated with electrodes 12b and 12d.

Using this series readout mode the variation in capacitance of the accumulation elements may in some cases interfere with the shift operation. However, this can be minimized if the drive or shift potentials are large (e.g., at least twice) the potential used for accumulation.

A preferred way of avoiding the problem just alluded to is to use parallel coupling. An embodiment illustrating this expedient is shown in plan view in Fig. 2A. In this device the charge coupled array of elements 12a—12d, 13a—13d, and 14a—14d are similar to those of Fig. 1. The three wire drive conductors 12, 13 and 14 are biased in sequence to affect the shift mechanism. The accumulation or memory stage is parallel to the shift row and comprises a single conductor strip 17 with a bias connection 16. Memory elements are shown at 12a' and 12c'. These elements are simply thin portions in a relatively thick insulator 11'. The structure is evident from Fig. 2B which is a section through element 12c'. The high capacitance associated with these elements will allow accumulation of carriers for, for example, a digital "one", as compared with the absence of carriers accumulated adjacent electrodes 12b and 12d, which might represent digital "zeros". When the accumulation is complete, conductor 12 is biased and the sequential shift operation produces the digital signal at the output. For this segment of the device, that signal would be 0101.

Charge transfer between the accumulation or memory stage and the charge coupled line is to be avoided during the shift operation. Several simple techniques can be used, to achieve this. For example, the accumulation process can be made long in comparison to the readout time so that interaction during readout will involve too few carriers to impair the signal. Alternatively, the bias on electrode 17 is removed during the shift operation so that no carriers will accumulate.

The accumulation elements 12a'—12c' can be physically isolated from the charge coupled line with a gate electrode. This will be evident from the discussion below in connection with Fig. 3.

There are various convenient ways of fabricating the structure of Figs. 1 and 2A taking advantage of known semiconductor processing techniques. For example, the insulator

can be deposited to the thickness desired at elements 12b and 12d (i.e., the combined thickness of layers 11 and 15 in Fig. 1 or the thickness of layer 11' in Fig. 2A) and then selectively etched to form the thinned regions. Alternatively a composite layer such as SiO₂ and Si₃N₄ can be deposited which is then selectively etched with a preferential etchant to give the desired structure. These techniques are well known.

Another means for obtaining a difference in storage capacity between selected elements is to use metal electrodes having significantly different work functions. The structure in this case would be essentially that shown in Fig. 1 except that the insulating layer would be uniform in thickness at each element associated with electrodes 12a, 12b, 12c and 12d. Electrodes 12a and 12c would be, e.g. platinum, with electrodes 12b and 12d tungsten. The difference in work function between these metals is approximately 1.0 volts, giving an easily detectable variation in charge storage with normal bias voltages.

The parallel coupling arrangement of Fig. 2A can be easily adapted to this embodiment. This would require simply that electrode 17 be segmented so that regions 12a' and 12c' are covered with platinum and regions 12b and 12d with tungsten. A common conductor 16 is still appropriate as these sites are normally biased simultaneously.

A modification of the parallel coupling memory of Fig. 2A is shown in Fig. 3. For illustration, this device employs the two wire scheme described in our co-pending application No. 21833/71 (Serial No. 1,340,620). In this case every other element comprises a memory stage. The device includes the familiar semiconductor storage medium, 30, insulating layer 31, and the sequence of drive electrodes 32a, 33a, 32b, 33b, 32c, 33c, 32d, 33d, 32e and 33e, all connected to conductors 32 and 33 as shown. The sequential drive operation is described completely in the application alluded to above and the function of the stepped insulator and the drive electrode configuration will not be repeated here. The front portion of the semiconductor 30 is not covered with insulator and contains a continuous longitudinally extending diffused region 34 which forms with the substrate a p-n junction. An electrode 35 is provided to externally short the junction. This p-n junction functions similarly to the source of an IGFET and provides a continuous supply of charge carriers in close proximity to the electrode sequence 32a to 33e, but as yet uncoupled to it. The coupling is made selectively by gate electrodes 36, 37 and 40. Gates at 38 and 39 are intentionally omitted as called for by the memory code. When the gate electrodes are biased via conductor 41, charge flows from the source junction 34 to the region under the gates. Conductor 32

is biased coincidentally with conductor 41 and charge flows through the biased gates into the charge coupled line. The charge accumulated under the associated drive electrodes 32a, 32b, 32c, 32d and 32e is shifted out in the normal way by sequentially biasing conductors 32 and 33. The binary signal derived from this sequence would be 10011.

These memory stages resemble hybrid IGFETS with a p-n junction source and an MIS drain.

At this point it is evident that the device of Fig. 3 can alternatively be made with individual p-n junctions made at selected sites and with a continuous gate electrode.

It is also worth noting that these devices are digital and in the form shown do not have analog capability. They are also characteristically distinct from the other devices described herein in that those devices involve programming the inherent storage capacity of selected storage sites while these embodiments function by charging only selected elements of a charge coupled line (all elements have essentially the same charge capacity) and wherein the charging is accomplished by coupling to an instantaneous supply of carriers. Note that in the device of Fig. 2A the charging of the charge coupled line is selective but the supply of carriers requires a finite accumulation period. Consequently, it is evident that devices of the type suggested by Fig. 3 are inherently faster.

An embodiment of a charge coupled memory device in which the memory can be adjusted is shown in Fig. 4. The substrate 50 is of semiconductor material such as silicon, and the three electrodes 51, 52 and 53 comprise the three wire drive system with associated conductors 54, 55 and 56. This drive scheme is exemplary only. The intermediate layer, which is normally a homogeneous insulator of an MIS structure, in this case contains the memory element. A thin insulating layer 57 covers substrate 50 and separates it from the floating capacitor plate 58. The capacitor plate may be of metal or semiconductor material and serves simply to store charge. A second insulating layer 59 isolates the capacitor from the drive electrodes 51, 52 and 53. The insulating layer 57 is sufficiently conducting so as to allow charge to be transferred between the capacitor plate 58 and the substrate 50. The insulating layer 59 should be sufficiently thick to prevent significant amounts of charge from leaking from the drive electrodes 51, 52 and 53 under normal bias conditions.

The partially conducting insulator 57 should exhibit the non-ohmic behaviour described by Fig. 5. Charge stored at the semiconductor-insulator interface should not leak to the capacitive memory plate except during the read operation. If the insulator is non-ohmic, a threshold field, E_t, allows fields

above this value to be used for reading into and erasing the memory, while the use of a field below E_t permits normal storage and drive functions without affecting the memory.

5 The read-in operation through which the floating capacitor plate 58 is charged is described by Figs. 6A and 6B. Fig. 6A is a band structure diagram of the device of Fig. 4 without charge being present at the semiconductor-insulator interface (n-type semiconductor), while Fig. 6B is a corresponding band structure diagram with charge stored at the interface. The presence or absence of charge (or the amount of charge) is the information being read into the memory and can be placed locally on the memory plate by normal charge coupled action. With the charge pattern in place in the semiconductor body 50 a relatively large voltage V_1 is imposed across the composite structure. The magnitude of V_1 is such that with no charge at the interface (Fig. 6A) the electric field at the barrier between the floating capacitor 58 and the semiconductor 50 is low enough to prevent conduction, i.e., below the threshold field E_t . However, with positive charge at the interface, there is a larger voltage drop across the insulator as compared to the semiconductor, resulting in a field across the thin insulator greater than E_t . This larger field allows conduction of electrons through the thin insulator 57 and leaves a net positive charge in the floating capacitor. This charge is effectively isolated and will decay with a time characteristic of the leakage current for fields below E_t . The operating voltages are chosen smaller in magnitude than V_1 so that the leakage current is kept acceptably small. With proper choice of the insulator 57 and the drive voltage, the charge decay time can be made essentially infinite. A positive voltage equal to or exceeding V_1 on electrode 52 will extract majority carriers from the semiconductor and erase the charge.

45 The amount of charge read into the capacitor 58 will determine the storage capacity for holes of the semiconductor-insulator interface. Thus the memory can be made analog as well as digital.

50 The read operation requires simply the accumulation of carriers in each of the memory stages (in this case those associated with conductor 55) to the extent of its capacity. With an n-type semiconductor a negative voltage is impressed on the conductor 55 associated with the memory element comprising electrode 52, and holes are allowed to accumulate to their thermal equilibrium value. The charge is then shifted out by charge coupled action. The accumulation of carriers can be accelerated by photo-induced holes or by shifting in charge by charge coupled action at a large negative voltage and then making the voltage less negative so that each site becomes saturated.

The accumulation of carriers can be selectively controlled by focusing a light image on the substrate and comparing the spatial intensity of the image with the memory. In this way the device can be made to function as an image comparator or for pattern recognition.

The capacitive memory plates are similar in function and structure to the floating gate field effect transistor described in Bell System Technical Journal, July-August 1967, pp. 1288—1300.

The following is a specific example of this embodiment of the invention and prescribes appropriate dimensions from which all the devices described herein can be conveniently derived.

The device of Fig. 4 is made with 10 ohm-cm silicon as the substrate material 50. The thin insulating layer 57 is SiO_2 grown or deposited to a thickness of 10Å to 1000Å. The capacitor memory plates 58 are platinum or silicon with a thickness of 100Å to 1000Å. The plate thickness is not functionally important and the range given is simply convenient. A thick plate 58 risks dielectric discontinuity in the insulator 59. The voltage required for conduction between plate 58 and substrate 50 is of the order of 50 millivolts per angstrom of insulator. Therefore the voltage range corresponding approximately to the threshold field E_t of Fig. 5 would range from 0.5 volts to 50 volts for the recommended range of insulator thickness. The insulator 59 can also be SiO_2 with a thickness of the order of 200Å to 10000Å and, for reasons evident from the foregoing description, at least twice the thickness of the insulating layer 57. If the insulating layers are composed of different materials, e.g., a combination of SiO_2 and Si_3N_4 , then the thickness and dielectric strengths of the materials should be chosen so that the insulator 57 has at least twice the conduction of the layer 59 for a given write voltage. The drive electrodes 51, 52, and 53 can be of any conducting material such as gold, platinum or polycrystalline silicon. The memory plates 58 can also be formed of semiconductor material such as silicon. Advantageously the memory plates and the substrate 50 are of different conductivity type.

The memory devices have been described with a conventional semiconductor substrate and the depletion mode of operation. The memory mechanism will function in an equivalent manner with the enhancement type charge coupled device using insulating or semi-insulating semiconductor material as described and claimed in our aforementioned pending application No. 21832/71. The term insulating or semi-insulating semiconductor material refers to those materials defined in that application.

Alternative structures can be used for the

floating plate capacitor shown in Fig. 4. For example if two different insulating materials are deposited in a dual layer, charge is typically trapped at the interface. This charge resides in deep traps and these traps can be depleted and replenished via the mechanism described above. The interfacial traps can be thought of as directly analogous to the memory plate 58 of Fig. 4. A useful combination of insulators for this embodiment are $\text{SiO}_2\text{--Si}_3\text{N}_4$ and $\text{SiO}_2\text{--Al}_2\text{O}_3$. The latter combination is convenient from the point of view of fabrication. A dual layer of silicon and aluminium can be deposited and then anodized, e.g., by plasma anodization. The technique provides good control over the interface properties. A similar result would be expected for Si_3N_4 and AlN . An explanation of these interfacial states and the mechanism for filling and emptying them is described in RCA Review, Vol. 30, June 1969, pp. 335—382.

Another related charge storage mechanism relies on deep traps in the bulk of the insulator. Taking advantage of these, a very simple memory device can be constructed. It requires simply a homogeneous insulating layer between the drive electrodes and the storage mechanism. Thus it is different from the basic charge coupled device in the voltages used for operation. The basic charge coupled device can use drive voltages of different values but all these would be below the threshold for conduction across the insulator. In the normal operating mode, carrier injection to or from the storage mechanism is undesirable. Thus the provision of a bias means for impressing a voltage large enough to fill or empty traps in the insulator with an operating sequence appropriate to the memory mode differentiates this device from the conventional charge coupled device. For this mode of operation, the insulating layer advantageously has at least 10^{16} deep charge carrier traps per cm^3 .

Yet another embodiment in which the storage site capacitance can be semipermanently adjusted uses a structure with a stepped insulator similar to those of Figs. 1 and 2A except that the thickness of the insulator can be adjusted by using, as the insulating material, a thermoplastic material of the type described in the Journal of Applied Physics, Dec. 1959, pp. 1870—1873, and RCA Review Vol. XXIII September 1962, p. 413. These materials are typically polymers with a low-temperature glass transition. When they are heated to their plastic transformation point in the presence of an electric field they constrict in the direction of the field until the electrostatic forces balance the surface tension forces. Lowering the temperature will freeze the material in the deformed state, and raising the temperature again in the absence of a field will allow the surface tension

forces to restore the material to its original state. Thermoplastics are not very compressible so that constriction will displace the plastic from the area under the electrode.

The device just described functions basically in the same manner as those described in connection with Fig. 1 except for the memory read-in. To accomplish the latter, charge representing the desired memory code is shifted into electrodes 12a, 12b, 12c and 12d. Following the previous example this will leave charge at sites accompanying electrodes 12a and 12c with no charge below electrodes 12b and 12d. The thermoplastic layer is then heated causing constriction of the plastic at sites 12a and 12c and no constriction at sites 12b and 12d. Cooling the thermoplastic leaves the desired stepped insulator.

Extension of this scheme to analogue memory devices is straightforward.

WHAT WE CLAIM IS:—

1. A charge coupled memory device comprising a semiconducting or insulating or semi-insulating semiconductor body having means associated therewith for effecting storage of charge carriers at discrete storage sites at or near the surface of the body, means which when suitably energised effect transfer of stored charges between storage sites and to a detection site at which the charge magnitude may be detected, in which means are provided individual to at least one selected storage site to control the accumulation of charge carriers at the selected storage site so as to provide the site with a distinct memory function.
2. A device according to claim 1, wherein the storage capacity of selected sites differs, when in use, by a predetermined amount from that of the remaining sites so that accumulation of charge carriers at these selected sites provides distinctive output signals.
3. A device according to claim 2, wherein the said selected sites differ structurally from the remaining sites so as to produce the desired difference of capacity.
4. A device according to claim 1, wherein the said selected sites are adapted to have their storage capacity adjusted when in use to produce the desired difference of capacity.
5. A device according to claim 1, 2 or 3, wherein the storage sites comprise MIS regions.
6. A device according to claim 5, wherein the said structural difference comprises a difference in the thickness of the insulating layer.
7. A device according to claim 5, with claim 3 wherein the said structural difference is effected by using metal layers having different work functions.
8. A device according to claim 6, wherein the insulating layer comprises electrostrictive



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floating plate capacitor shown in Fig. 4. For example if two different insulating materials are deposited in a dual layer, charge is typically trapped at the interface. This charge resides in deep traps and these traps can be depleted and replenished via the mechanism described above. The interfacial traps can be thought of as directly analogous to the memory plate 58 of Fig. 4. A useful combination of insulators for this embodiment are SiO_2 — Si_3N_4 and SiO_2 — Al_2O_3 . The latter combination is convenient from the point of view of fabrication. A dual layer of silicon and aluminium can be deposited and then anodized, e.g., by plasma anodization. The technique provides good control over the interface properties. A similar result would be expected for Si_3N_4 and AlN . An explanation of these interfacial states and the mechanism for filling and emptying them is described in RCA Review, Vol. 30, June 1969, pp. 335—382.

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forces to restore the material to its original state. Thermoplastics are not very compressible so that constriction will displace the plastic from the area under the electrode.

The device just described functions basically in the same manner as those described in connection with Fig. 1 except for the memory read-in. To accomplish the latter, charge representing the desired memory code is shifted into electrodes 12a, 12b, 12c and 12d. Following the previous example this will leave charge at sites accompanying electrodes 12a and 12c with no charge below electrodes 12b and 12d. The thermoplastic layer is then heated causing constriction of the plastic at sites 12a and 12c and no constriction at sites 12b and 12d. Cooling the thermoplastic leaves the desired stepped insulator.

Extension of this scheme to analogue memory devices is straightforward.

WHAT WE CLAIM IS:—

1. A charge coupled memory device comprising a semiconducting or insulating or semi-insulating semiconductor body having means associated therewith for effecting storage of charge carriers at discrete storage sites at or near the surface of the body, means which when suitably energised effect transfer of stored charges between storage sites and to a detection site at which the charge magnitude may be detected, in which means are provided individual to at least one selected storage site to control the accumulation of charge carriers at the selected storage site so as to provide the site with a distinct memory function.
2. A device according to claim 1, wherein the storage capacity of selected sites differs, when in use, by a predetermined amount from that of the remaining sites so that accumulation of charge carriers at these selected sites provides distinctive output signals.
3. A device according to claim 2, wherein the said selected sites differ structurally from the remaining sites so as to produce the desired difference of capacity.
4. A device according to claim 1, wherein the said selected sites are adapted to have their storage capacity adjusted when in use to produce the desired difference of capacity.
5. A device according to claim 1, 2 or 3, wherein the storage sites comprise MIS regions.
6. A device according to claim 5, wherein the said structural difference comprises a difference in the thickness of the insulating layer.
7. A device according to claim 5, with claim 3 wherein the said structural difference is effected by using metal layers having different work functions.
8. A device according to claim 6, wherein the insulating layer comprises electrostrictive



material the thickness of which is temporarily fixed by electrostrictive means.

9. A device according to claim 1 wherein the body has a first insulating layer thereon, a plurality of spaced plates overlying the first layer, a second insulating layer covering the plates and the first layer, the second layer having in use not more than half the conduction of the first layer with respect to charges stored on the plates and a plurality of drive electrodes positioned on the second layer some of which lie above the plates, the first insulating layer exhibiting when in use a partially conducting non-ohmic characteristic.

10. A device according to claim 9 wherein the body is of silicon.

11. A device according to claim 10, wherein the first and second layers are of silicon dioxide.

12. A device according to claim 9, 10 or 11 wherein the plates are of metal.

13. A device according to claim 9, 10 or 11 wherein the plates are of semiconductor material.

14. A device according to claim 1 wherein the said sites are formed by a first insulating layer on the body and a second insulating layer on the first layer forming deep charge carrier traps at the interface between the layers and conductor means on the second insulating layer, the arrangement being such that a first bias voltage shifts the charge into or out of a charge coupled site and a second voltage, larger than the first causes charge to flow from the body to the deep traps.

15. A device according to claim 1 wherein the sites comprise an insulating layer having at least 10^{16} deep charge traps per cubic centimeter and a drive electrode on the insulating layer and means for shifting charge into and out of sites comprising a charge coupled element adjacent thereto, the arrangement being such that application of a bias voltage between the drive electrode and the body causes conduction of carriers between the body and the deep traps.

16. A device according to claim 14 wherein the first insulating layer is of silicon dioxide and the second of silicon nitride.

17. A device according to claim 14 wherein the first layer is of silicon dioxide and the second is of aluminium oxide.

18. A device according to claim 1 wherein the sites comprise insulated gate field effect devices each having a source region, an MIS drain region and selected ones having a common gate, the drain regions being disposed to form a charge coupled line, the arrangement being such that the applications of bias to the common gate and drain regions and of a sequential bias to successive drain regions will shift charge along the line.

19. A device according to claim 18 wherein the source region of such devices is provided by a common p-n junction.

20. A device according to claim 1 wherein the sites comprise insulated gate field effect devices each having an MIS drain region and selected ones having a source region and a gate region common to at least two devices the drain regions of these at least two devices being side-by-side to form a charge coupled line, the arrangement being such that the application of a bias to the gate and drain regions and of a sequential bias to the successive drain regions will shift charge along the line.

21. A device according to claim 20 wherein the selected source regions are provided by p-n junctions.

22. A device according to claim 18, 19, 20 or 21 wherein the body is of silicon and the insulator is of silicon dioxide.

23. A charge coupled memory device arranged and adapted to operate substantially as herein described with reference to and as shown in Fig. 1 or Figs. 2A and 2B or Fig. 3 or Fig. 4, 5, 6A and 6B of the drawings.

24. A charge coupled memory arrangement employing a device according to claim 23.

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