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(71) Applicant (for all designated States except US): **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95052 (US).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **WIJERATNE, Sampul** [LK/US]; 16187, NW RYEGRASS STREET, Portland, Oregon 97229 (US).

(74) Agents: **VINCENT, Lester J.** et al.; **BLAKELY SOKOLOFF TAYLOR & ZAFMAN**, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 950025 (US).

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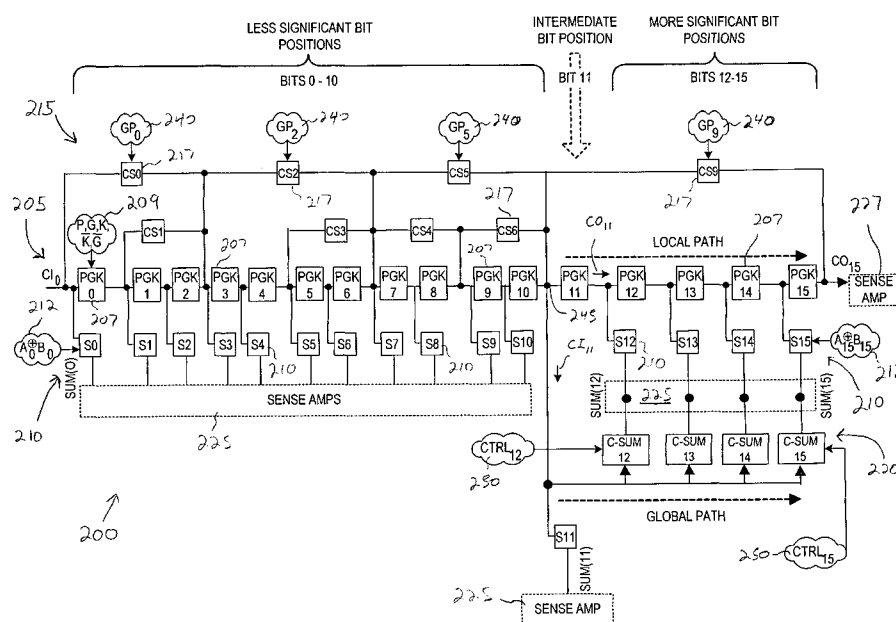
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(54) Title: CARRY-SKIP ADDER HAVING MERGED CARRY-SKIP CELLS WITH SUM CELLS



(57) Abstract: A multi-bit adder includes a carry chain, a carry-skip network, sum cells, and a carry-sum cell. The carry chain propagates, generates, or kills carry-in bits. The carry-skip network is coupled to the carry chain to selectively skip the carry-in bits over at least one portion of the carry chain. The sum cells are coupled along the carry chain to sum the carry-in bits with corresponding bits of two operands to generate a multi-bit resultant. The carry-sum cell is coupled to receive one of the carry-in bits to a single intermediate bit position on the carry chain and to generate one bit of the multi-bit resultant having a more significant bit position than the single intermediate bit position.