

CORRECTED VERSION

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
11 March 2004 (11.03.2004)

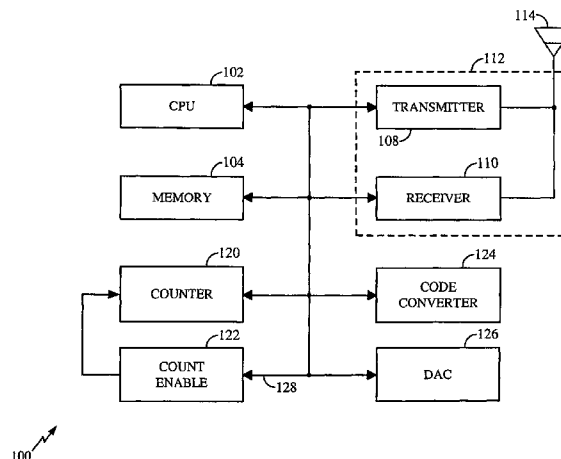
PCT

(10) International Publication Number
WO 2004/021589 A1

- (51) International Patent Classification⁷: **H04B 1/30**, H04L 25/06
- (21) International Application Number: PCT/US2003/027016
- (22) International Filing Date: 28 August 2003 (28.08.2003)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
10/233,364 29 August 2002 (29.08.2002) US
- (71) Applicant: **QUALCOMM INCORPORATED** [US/US];
5775 Morehouse Drive, San Diego, CA 92121 (US).
- (72) Inventors: **SCHLEGEL, Nikolai**; 11995 Wilmington Road, San Diego, CA 92128 (US). **HOLENSTEIN, Christian**; 4424 Felton Street, San Diego, CA 92103 (US). **FILIPOVIC, Daniel**; 429 South Sierra Avenue, #341, Solana Beach, CA 92075 (US). **KASTURI, Nitin**; 859 University Avenue #16, Los Gatos, CA 95032 (US).
- (74) Agents: **MINHAS, Sandip, S.** et al.; QUALCOMM Incorporated, 5775 Morehouse Drive, San Diego, CA 92121 (US).
- (81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
- Published:
— with international search report

[Continued on next page]

(54) Title: APPARATUS AND METHOD FOR DC OFFSET COMPENSATION IN A DIRECT CONVERSION RECEIVER



(57) Abstract: An apparatus for coarse compensation of a direct current (DC) offset in a direct to baseband receiver architecture utilizes a serial analog to digital converter (ADC), such as a Delta-Sigma converter, to convert the received signal to digital form. The output of the ADC is sampled for a predetermined number of samples and a counter coupled to the ADC is incremented each time the sample generated by the ADC is a logic one. The counter is not incremented if the sample from the ADC is a logic zero. After the predetermined number of samples is obtained, the counter value is indicative of the DC offset in the received signal. The counter value may be converted by a code converter to a correction value for easy operation of a digital to analog converter (DAC). If the number of samples from the ADC is a power of two, the code converted may be readily implemented by simply inverting the most significant bit (MSB) from the counter to thereby generate a twos complement version of the counter value. The correction value is coupled to the DAC to generate a compensation signal, which is provided to the received signal path in the form of a feedback signal to compensate for the DC offset.

WO 2004/021589 A1



(48) Date of publication of this corrected version:

6 May 2004

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(15) Information about Correction:

see PCT Gazette No. 19/2004 of 6 May 2004, Section II