

DESCRIPTION

**METHOD FOR USING SPUTTERING TARGET AND
METHOD FOR MANUFACTURING OXIDE FILM**

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TECHNICAL FIELD

[0001]

The present invention relates to an object, a method, or a manufacturing method. In addition, the present invention relates to a process, a machine, manufacture, or a composition of matter. In particular, the present invention relates to, for example, a semiconductor device, a display device, a light-emitting device, a power storage device, a driving method thereof, or a manufacturing method thereof. The present invention particularly relates to a semiconductor device, a display device, or a light-emitting device each including an oxide semiconductor, for example. The present invention further particularly relates to a sputtering target and a manufacturing method thereof, for example. Alternatively, the present invention relates to an oxide film formed by a sputtering method, using the sputtering target, and a semiconductor device including the oxide film, for example.

[0002]

In this specification, a semiconductor device generally refers to a device which can function by utilizing semiconductor characteristics; an electro-optical device, a semiconductor circuit, and an electronic device are all included in the category of the semiconductor device.

25 BACKGROUND ART

[0003]

A technique by which a transistor is formed using a semiconductor thin film formed over a substrate having an insulating surface has been attracting attention. The transistor is applied to a wide range of electronic devices such as an integrated circuit (IC) or an image display device (display device). As a semiconductor thin film applicable to the transistor, a silicon film is widely known; moreover, an oxide semiconductor film has been attracting attention as another material.

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[0004]

For example, disclosure is made of a transistor including an amorphous oxide semiconductor film containing In, Ga, and Zn and having an electron carrier concentration of lower than 10^{18} /cm³, and a sputtering method is considered the most suitable as a method for forming the amorphous oxide semiconductor film (see Patent Document 1).

[0005]

Although an oxide semiconductor containing a plurality of metal elements has high controllability of carrier density, there have been problems in that such an oxide semiconductor is made amorphous easily and instable in physical properties.

[0006]

On the other hand, it is reported that a transistor including a crystalline oxide semiconductor film has excellent electrical characteristics and reliability compared with a transistor including an amorphous oxide semiconductor film (see Non-Patent Document 1).

[Reference]

[0007]

[Patent Document 1] Japanese Published Patent Application No. 2006-165528

[Non-Patent Document]

[0008]

[Non-Patent Document 1] Shunpei Yamazaki, Jun Koyama, Yoshitaka Yamamoto, and Kenji Okamoto, "Research, Development, and Application of Crystalline Oxide Semiconductor" *SID 2012 DIGEST*, pp. 183-186.

DISCLOSURE OF INVENTION

[0009]

An object of the present invention is to provide a method for manufacturing a crystalline oxide film, which is a method for forming an oxide film containing a plurality of metal elements.

[0010]

Another object of the present invention is to provide a sputtering target which enables the oxide film to be formed.

[0011]

Another object of the present invention is to provide a method for using the sputtering target.

[0012]

5 Another object of the present invention is to provide a transistor which has stable electrical characteristics with the use of the oxide film.

[0013]

Another object of the present invention is to provide a highly reliable semiconductor device including the transistor.

10 [0014]

An object of one embodiment of the present invention is to provide a semiconductor device with low off-state current. Alternatively, another object of one embodiment of the present invention is to provide a semiconductor device with low power consumption. Still alternatively, another object of one embodiment of the present invention is to provide a novel semiconductor device.

[0015]

Note that the descriptions of these objects do not disturb the existence of any other object. Note that in one embodiment of the present invention, there is no need to achieve all the objects. Other objects will be apparent from and can be derived from the description of the specification, the drawings, the claims, and the like.

[0016]

One embodiment of the present invention is a method for using a sputtering target including a polycrystalline oxide, in which a plurality of flat plate-like positively charged sputtered particles which are separated from the sputtering target are deposited on a deposition surface while repelling each other.

[0017]

Another embodiment of the present invention is a method for using a sputtering target including a polycrystalline oxide, which includes the steps of: making an ion collide with the sputtering target to separate a plurality of flat plate-like sputtered particles from the sputtering target; and positively charging the plurality of flat plate-like sputtered particles, so that the plurality of flat plate-like sputtered particles are deposited on a deposition surface while repelling each other.

[0018]

According to another embodiment of the present invention, a method for using a sputtering target including a polycrystalline oxide containing a plurality of crystal grains, in which the plurality of crystal grains each include a cleavage plane, includes the steps of: making an ion collide with the sputtering target to separate a plurality of flat plate-like sputtered particles from each cleavage plane; and positively charging the plurality of flat plate-like sputtered particles, so that the plurality of flat plate-like sputtered particles are deposited on a deposition surface while repelling each other.

[0019]

Note that when the sputtered particle has a hexagonal cylinder shape, the sputtered particles are deposited uniformly with ease.

[0020]

Another embodiment of the present invention is a method for forming an oxide film by depositing sputtered particles by any of the above-described methods.

[0021]

Note that the cleavage plane refers to a plane where atoms included in a crystal grain are bonded weakly (a surface where cleavage occur or a surface where cleavage occur easily).

[0022]

Owing to the cleavage planes in the plurality of crystal grains included in the sputtering target, when an ion collides with the sputtering target, sputtered particles can be separated from the cleavage plane of the crystal grain.

[0023]

The separated sputtered particles which are formed from part of the crystal grain in such a manner has high crystallinity. Thus, an oxide film with a high degree of crystallinity can be formed by depositing the sputtered particles.

[0024]

Note that the sputtered particle is separated from the cleavage plane and thus has a flat plate-like shape (also referred to as a pellet shape). As obvious in terms of stability, the flat plate-like sputtered particle is attached to the deposition surface with a high probability that the cleavage plane and the deposition surface are parallel to each other. Thus, a crystal portion of an oxide film to be formed is aligned along one

crystal axis. For example, in the case where a cleavage plane of a crystal grain is parallel to an *a-b* plane, an oxide film has *c*-axis alignment. That is, a normal vector of the deposition surface and the *c*-axis of the crystal portion included in the oxide film are parallel to each other. However, an *a*-axis is freely rotated on the *c*-axis; therefore, the direction of *a*-axes of a plurality of crystal portions included in the oxide film are not the same.

[0025]

In this specification, the trigonal and rhombohedral crystal systems are included in the hexagonal crystal system.

[0026]

In this specification, a term "parallel" indicates that the angle formed between two straight lines is greater than or equal to -10° and less than or equal to 10° , and accordingly also includes the case where the angle is greater than or equal to -5° and less than or equal to 5° . In addition, a term "perpendicular" indicates that the angle formed between two straight lines is greater than or equal to 80° and less than or equal to 100° , and accordingly includes the case where the angle is greater than or equal to 85° and less than or equal to 95° .

[0027]

Although sputtered particles are ideally single crystals, the crystallinity in part of the sputtered particle may be lowered due to the impact of ion collision. Thus, in some cases, a region with low crystallinity is included between crystal portions of an oxide film to be formed. For example, from an observation image obtained with a transmission electron microscope (TEM), a boundary between crystal portions is not clear. Therefore, an oxide film of one embodiment of the present invention has high electron mobility because a reduction in electron mobility due to the grain boundary is suppressed.

[0028]

Here, a cleavage plane of a crystal of an In-Ga-Zn oxide (In:Ga:Zn = 1:1:1 [atomic ratio]) is described.

[0029]

FIG. 3A illustrates the crystal structure of an In-Ga-Zn oxide viewed from a

direction parallel to the a - b plane. FIG. 3B illustrates the crystal structure after ion collision during sputtering.

[0030]

For example, cleavage of the crystal grain included in the In-Ga-Zn oxide occurs between a layer including a gallium atom and/or zinc atom and an oxygen atom, and a layer including a gallium atom and/or zinc atom, and an oxygen atom, which are illustrated in FIG. 3B. This is because oxygen atoms which have negative charges exist in the layer in a close distance from each other. In this manner, the cleavage plane is parallel to the a - b plane.

[0031]

That is, it can be seen that, when an ion collides with the surface of a sputtering target including a crystal grain of an In-Ga-Zn oxide, the crystal grain included in the In-Ga-Zn oxide is cleaved along a plane parallel to the a - b plane of the crystal, and flat plate-like sputtered particles whose top and bottom surfaces are parallel to the a - b plane are separated from the sputtering target.

[0032]

Moreover, in the crystal of the In-Ga-Zn oxide illustrated in FIG. 3A, metal atoms are arranged in a regular triangular or regular hexagonal configuration when seen from the direction perpendicular to the a - b plane; therefore, the flat plate-like crystal grain is likely to have the shape of a hexagonal cylinder whose regular hexagonal plane has internal angles of 120° .

[0033]

Note that the relative density of the sputtering target is greater than or equal to 90 %, preferably greater than or equal to 95 %, more preferably greater than or equal to 99 %. Note that the relative density of the sputtering target refers to a ratio between the density of the sputtering target and the density of a substance free of porosity having the same composition as the sputtering target.

[0034]

The polycrystalline oxide included in the sputtering target is at least an oxide containing, for example, In, M (M is Ga, Sn, Hf, Al, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, or Lu), and Zn.

[0035]

Moreover, the atomic ratio of In, *M*, and Zn contained in the polycrystalline oxide is preferably close to the stoichiometric composition ratio. When the atomic ratio of In, *M*, and Zn contained in the polycrystalline oxide becomes close to the stoichiometric composition ratio, the crystallinity of the polycrystalline oxide can be increased. Note that as described with "close", the atomic ratio and the stoichiometric composition ratio may deviate within the range of $\pm 10\%$.

[0036]

The crystal grain included in the polycrystalline oxide containing In, *M*, and Zn includes a cleavage plane between a first plane containing *M* and Zn and a second plane containing *M* and Zn.

[0037]

Described below is a method for further increasing the degree of crystallinity of an oxide film which is obtained by a method for forming a thin film by depositing sputtered particles by any of the above-described methods.

[0038]

By reducing impurities that enter the oxide film, a crystal state is prevented from being broken by the impurities and an oxide film with a high degree of crystallinity can be formed. For example, the concentration of impurities (e.g., hydrogen, water, carbon dioxide, or nitrogen) which exist in a film formation chamber may be reduced. Furthermore, the concentration of impurities in a film formation gas may be reduced. Specifically, a film formation gas whose dew point is $-80\text{ }^{\circ}\text{C}$ or lower, preferably $-100\text{ }^{\circ}\text{C}$ or lower, more preferably $-120\text{ }^{\circ}\text{C}$ or lower is used.

[0039]

When the surface where the oxide film is to be formed has minute unevenness, the oxide film has a lower degree of crystallinity. Thus, the planarity of the surface where the oxide film is to be formed is improved, whereby an oxide film with a high degree of crystallinity can be formed.

[0040]

Further, by increasing the heating temperature during the film formation, migration of a sputtered particle occurs after the sputtered particle reach the deposition

surface; therefore, an oxide film with a high degree of crystallinity can be formed. Specifically, the heating temperature during the film formation is higher than or equal to 100 °C and lower than or equal to 740 °C, preferably higher than or equal to 200 °C and lower than or equal to 500 °C. By increasing the heating temperature during the film formation, when the flat plate-like sputtered particle reaches the deposition surface, migration occurs on the deposition surface, so that a plane of the flat plate-like sputtered particle parallel to a cleavage plane is easily attached to the deposition surface.

[0041]

Moreover, by increasing the proportion of oxygen included in the film formation gas and optimizing the power used for film formation, plasma damage at the film formation can be alleviated; accordingly, an oxide film with a high degree of crystallinity can be formed. The percentage of oxygen in the film formation gas is set to be greater than or equal to 30 vol.%, preferably greater than or equal to 50 vol.%, more preferably greater than or equal to 80 vol.%, still more preferably greater than or equal to 100 vol.%.

[0042]

In addition, an oxide film with a high degree of crystallinity can be obtained by performing heat treatment after the film formation to reduce the impurity concentration in the oxide film. The heat treatment is highly effective in reducing the impurity concentration when performed in an inert atmosphere or under a reduced pressure. For the heat treatment, heat treatment in an oxidation atmosphere is preferably performed after the heat treatment in an inert atmosphere or under a reduced pressure is performed. This is in some cases due to oxygen vacancies caused in the oxide film as well as a reduction in the impurity concentration in the oxide film by the heat treatment performed in an inert atmosphere or under a reduced pressure. By performing the heat treatment in an oxidation atmosphere, oxygen vacancies in the oxide film can be reduced.

[0043]

In the above manner, an oxide film with a high degree of crystallinity can be formed.

[0044]

The oxide film with a high degree of crystallinity is preferably a *c*-axis aligned

crystalline oxide semiconductor (CAAC-OS) film.

[0045]

The CAAC-OS film is one of oxide semiconductor films including a plurality of crystal parts, and most of the crystal parts each fit inside a cube whose one side is less than 100 nm. Thus, there is a case where a crystal part included in the CAAC-OS film fits inside a cube whose one side is less than 10 nm, less than 5 nm, or less than 3 nm. The density of defect states of the CAAC-OS film is lower than that of the microcrystalline oxide semiconductor film. The CAAC-OS film is described in detail below.

[0046]

In a TEM image of the CAAC-OS film, a boundary between crystal parts, that is, a grain boundary is not clearly observed. Thus, in the CAAC-OS film, a reduction in electron mobility due to the grain boundary is less likely to occur.

[0047]

According to the TEM image of the CAAC-OS film observed in a direction substantially parallel to a sample surface (cross-sectional TEM image), metal atoms are arranged in a layered manner in the crystal parts. Each metal atom layer has a morphology reflected by a surface over which the CAAC-OS film is formed (hereinafter, a surface over which the CAAC-OS film is formed is referred to as a formation surface) or a top surface of the CAAC-OS film, and is arranged in parallel to the formation surface or the top surface of the CAAC-OS film.

[0048]

On the other hand, according to the TEM image of the CAAC-OS film observed in a direction substantially perpendicular to the sample surface (plan TEM image), metal atoms are arranged in a triangular or hexagonal configuration in the crystal parts. However, there is no regularity of arrangement of metal atoms between different crystal parts.

[0049]

From the results of the cross-sectional TEM image and the plan TEM image, alignment is found in the crystal parts in the CAAC-OS film.

[0050]

A CAAC-OS film is subjected to structural analysis with an X-ray diffraction

(XRD) apparatus. For example, when the CAAC-OS film including an InGaZnO₄ crystal is analyzed by an out-of-plane method, a peak appears frequently when the diffraction angle (2θ) is around 31°. This peak is derived from the (009) plane of the InGaZnO₄ crystal, which indicates that crystals in the CAAC-OS film have c-axis alignment, and that the c-axes are aligned in a direction substantially perpendicular to the formation surface or the top surface of the CAAC-OS film.

[0051]

On the other hand, when the CAAC-OS film is analyzed by an in-plane method in which an X-ray enters a sample in a direction substantially perpendicular to the c-axis, a peak appears frequently when 2θ is around 56°. This peak is derived from the (110) plane of the InGaZnO₄ crystal. Here, analysis (ϕ scan) is performed under conditions where the sample is rotated around a normal vector of a sample surface as an axis (ϕ axis) with 2θ fixed at around 56°. In the case where the sample is a single-crystal oxide semiconductor film of InGaZnO₄, six peaks appear. The six peaks are derived from crystal planes equivalent to the (110) plane. On the other hand, in the case of a CAAC-OS film, a peak is not clearly observed even when ϕ scan is performed with 2θ fixed at around 56°.

[0052]

According to the above results, in the CAAC-OS film having c-axis alignment, while the directions of a-axes and b-axes are different between crystal parts, the c-axes are aligned in a direction parallel to a normal vector of a formation surface or a normal vector of a top surface. Thus, each metal atom layer arranged in a layered manner observed in the cross-sectional TEM image corresponds to a plane parallel to the a-b plane of the crystal.

[0053]

Note that the crystal part is formed concurrently with deposition of the CAAC-OS film or is formed through crystallization treatment such as heat treatment. As described above, the c-axis of the crystal is aligned in a direction parallel to a normal vector of a formation surface or a normal vector of a top surface. Thus, for example, in the case where a shape of the CAAC-OS film is changed by etching or the like, the c-axis might not be necessarily parallel to a normal vector of a formation surface or a normal

vector of a top surface of the CAAC-OS film.

[0054]

Further, the degree of crystallinity in the CAAC-OS film is not necessarily uniform. For example, in the case where crystal growth leading to the CAAC-OS film occurs from the vicinity of the top surface of the film, the degree of the crystallinity in the vicinity of the top surface is higher than that in the vicinity of the formation surface in some cases. Further, when an impurity is added to the CAAC-OS film, the crystallinity in a region to which the impurity is added is changed, and the degree of crystallinity in the CAAC-OS film varies depending on regions.

[0055]

Note that when the CAAC-OS film with an InGaZnO₄ crystal is analyzed by an out-of-plane method, a peak of 2θ may also be observed at around 36°, in addition to the peak of 2θ at around 31°. The peak of 2θ at around 36° indicates that a crystal having no *c*-axis alignment is included in part of the CAAC-OS film. It is preferable that in the CAAC-OS film, a peak of 2θ appears at around 31° and a peak of 2θ do not appear at around 36°.

[0056]

In a transistor including the CAAC-OS film, change in electrical characteristics due to irradiation with visible light or ultraviolet light is small. Thus, the transistor has high reliability.

[0057]

An example of a crystal structure of the crystal portion included in the CAAC-OS film is described in detail with reference to FIGS. 4A to 4E, FIGS. 5A to 5C, FIGS. 6A to 6C, and FIGS. 7A and 7B. In FIGS. 4A to 4E, FIGS. 5A to 5C, FIGS. 6A to 6C, and FIGS. 7A and 7B, the vertical direction corresponds to the *c*-axis direction and a plane perpendicular to the *c*-axis direction corresponds to the *a-b* plane, unless otherwise specified. In the case where the expressions "an upper half" and "a lower half" are simply used, they refer to an upper half above the *a-b* plane and a lower half below the *a-b* plane (an upper half and a lower half with respect to the *a-b* plane). Moreover, in FIGS. 4A to 4E, O surrounded by a circle represents tetracoordinate O and O surrounded by a double circle represents tricoordinate O.

[0058]

FIG. 4A illustrates a structure including one hexacoordinate In atom and six tetracoordinate oxygen (hereinafter referred to as tetracoordinate O) atoms proximate to the In atom. Here, a structure including one metal atom and oxygen atoms proximate thereto is referred to as a small group. The structure in FIG. 4A is actually an octahedral structure, but is illustrated as a planar structure for easy understanding. Note that three tetracoordinate O atoms exist in each of an upper half and a lower half in FIG. 4A. In the small group illustrated in FIG. 4A, electric charge is 0 (zero).

[0059]

FIG. 4B illustrates a structure including one pentacoordinate Ga atom, three tricoordinate oxygen (hereinafter referred to as tricoordinate O) atoms proximate to the Ga atom, and two tetracoordinate O atoms proximate to the Ga atom. All the tricoordinate O atoms are on the *a-b* plane. One tetracoordinate O atom is located in each of an upper half and a lower half in FIG. 4B. An In atom can also have the structure illustrated in FIG. 4B because an In atom can have five ligands. In the small group illustrated in FIG. 4B, electric charge is 0.

[0060]

FIG. 4C illustrates a structure including one tetracoordinate Zn atom and four tetracoordinate O atoms proximate to the Zn atom. In FIG. 4C, one tetracoordinate O atom exists in an upper half and three tetracoordinate O atoms exist in a lower half. In the small group illustrated in FIG. 4C, electric charge is 0.

[0061]

FIG. 4D illustrates a structure including one hexacoordinate Sn atom and six tetracoordinate O atoms proximate to the Sn atom. In FIG. 4D, three tetracoordinate O atoms exist in each of an upper half and a lower half. In the small group illustrated in FIG. 4D, electric charge is +1.

[0062]

FIG. 4E illustrates a small group including two Zn atoms. In FIG. 4E, one tetracoordinate O atom exists in each of an upper half and a lower half. In the small group illustrated in FIG. 4E, electric charge is -1.

[0063]

Here, a plurality of small groups form a medium group, and a plurality of medium groups form a large group.

[0064]

Now, a rule of bonding between the small groups is described. The three O atoms in the upper half with respect to the hexacoordinate In atom in FIG. 4A has three proximate In atoms in the downward direction, and the three O atoms in the lower half has three proximate In atoms in the upward direction. The one O atom in the upper half with respect to the pentacoordinate Ga atom in FIG. 4B has one proximate Ga atom in the downward direction, and the one O atom in the lower half has one proximate Ga atom in the upward direction. The one O atom in the upper half with respect to the one tetracoordinate Zn atom in FIG. 4C has one proximate Zn atom in the downward direction, and the three O atoms in the lower half has three proximate Zn atoms in the upward direction. In this manner, the number of tetracoordinate O atoms above a metal atom is equal to the number of metal atoms proximate to and below the tetracoordinate O atoms; similarly, the number of tetracoordinate O atoms below a metal atom is equal to the number of metal atoms proximate to and above the tetracoordinate O atoms. Since the coordination number of the tetracoordinate O atom is 4, the sum of the number of metal atoms proximate to and below the O atom and the number of metal atoms proximate to and above the O atom is 4. Accordingly, when the sum of the number of tetracoordinate O atoms above a metal atom and the number of tetracoordinate O atoms below another metal atom is 4, the two kinds of small groups including the metal atoms can be bonded to each other. For example, in the case where the hexacoordinate metal (In or Sn) atom is bonded through three tetracoordinate O atoms in the lower half, it is bonded to the pentacoordinate metal (Ga or In) atom or the tetracoordinate metal (Zn) atom.

[0065]

A metal atom whose coordination number is 4, 5, or 6 is bonded to another metal atom through a tetracoordinate O atom in the *c*-axis direction. In addition, a medium group can also be formed in a different manner by combining a plurality of small groups so that the total electric charge of the layered structure is 0.

[0066]

FIG. 5A illustrates a model of a medium group included in a layered structure of an In-Sn-Zn oxide. FIG. 5B illustrates a large group including three medium groups.

FIG. 5C illustrates an atomic arrangement where the layered structure in FIG. 5B is observed from the *c*-axis direction.

[0067]

In FIG. 5A, a tricoordinate O atom is omitted for easy understanding, and a tetracoordinate O atom is illustrated by a circle; the number in the circle shows the number of tetracoordinate O atoms. For example, three tetracoordinate O atoms existing in each of an upper half and a lower half with respect to a Sn atom are denoted by circled 3. Similarly, one tetracoordinate O atom existing in each of an upper half and a lower half with respect to an In atom is denoted by circled 1. Moreover, one tetracoordinate O atom existing in a lower half (or an upper half) with respect to a Zn atom is denoted by circled 1, and three tetracoordinate O atoms in an upper half (or a lower half) with respect to the Zn atom is denoted by circled 3.

[0068]

In the medium group included in the layered structure of the In-Sn-Zn oxide in FIG. 5A, in the order starting from the top, a Sn atom proximate to three tetracoordinate O atoms in each of an upper half and a lower half is bonded to an In atom proximate to one tetracoordinate O atom in each of an upper half and a lower half, the In atom is bonded to a Zn atom proximate to three tetracoordinate O atoms in an upper half, the Zn atom is bonded to an In atom proximate to three tetracoordinate O atoms in each of an upper half and a lower half through one tetracoordinate O atom in a lower half with respect to the Zn atom, the In atom is bonded to a small group that includes two Zn atoms and is proximate to one tetracoordinate O atom in an upper half, and the small group is bonded to a Sn atom proximate to three tetracoordinate O atoms in each of an upper half and a lower half through one tetracoordinate O atom in a lower half with respect to the small group. A plurality of such medium groups are bonded, so that a large group is formed.

[0069]

Here, electric charge for one bond of a tricoordinate O atom and electric charge for one bond of a tetracoordinate O atom can be assumed to be -0.667 and -0.5 , respectively. For example, electric charge of a (hexacoordinate or pentacoordinate) In atom, electric charge of a (tetracoordinate) Zn atom, and electric charge of a (pentacoordinate or hexacoordinate) Sn atom are $+3$, $+2$, and $+4$, respectively.

Accordingly, electric charge in a small group including a Sn atom is +1. Therefore, electric charge of -1, which cancels +1, is needed to form a layered structure in the small group including a Sn atom. As a structure having electric charge of -1, the small group including two Zn atoms as illustrated in FIG. 4E can be given. For example, with one
5 small group including two Zn atoms, electric charge of one small group including a Sn atom is cancelled, so that the total electric charge of the layered structure can be 0.

[0070]

Specifically, when the large group illustrated in FIG. 5B is repeated, a crystal of an In-Sn-Zn oxide ($\text{In}_2\text{SnZn}_3\text{O}_8$) can be obtained. Note that a layered structure of the
10 obtained crystal of the In-Sn-Zn oxide can be expressed as a composition formula, $\text{In}_2\text{SnZnO}_6(\text{ZnO})_m$ (m is 0 or a natural number).

[0071]

The above-described rule also applies to the following oxides: an In-Sn-Ga-Zn oxide; an In-Ga-Zn oxide, an In-Al-Zn oxide; a Sn-Ga-Zn oxide; an Al-Ga-Zn oxide; a
15 Sn-Al-Zn oxide; an In-Hf-Zn oxide; an In-La-Zn oxide; an In-Ce-Zn oxide; an In-Pr-Zn oxide; an In-Nd-Zn oxide; an In-Sm-Zn oxide; an In-Eu-Zn oxide; an In-Gd-Zn oxide; an In-Tb-Zn oxide; an In-Dy-Zn oxide; an In-Ho-Zn oxide; an In-Er-Zn oxide; an In-Tm-Zn oxide; an In-Yb-Zn oxide; an In-Lu-Zn oxide; an In-Zn oxide; a Sn-Zn oxide; an Al-Zn oxide; a Zn-Mg oxide; a Sn-Mg oxide; an In-Mg oxide; an In-Ga oxide; and the like.

[0072]

For example, FIG. 6A illustrates a model of a medium group included in a layered structure of an In-Ga-Zn oxide.

[0073]

In the medium group included in the layered structure of the In-Ga-Zn oxide in
25 FIG. 6A, in the order starting from the top, an In atom proximate to three tetracoordinate O atoms in each of an upper half and a lower half is bonded to a Zn atom proximate to one tetracoordinate O atom in an upper half, the Zn atom is bonded to a Ga atom proximate to one tetracoordinate O atom in each of an upper half and a lower half through three tetracoordinate O atoms in a lower half with respect to the Zn atom, and the Ga atom is
30 bonded to an In atom proximate to three tetracoordinate O atoms in each of an upper half and a lower half through one tetracoordinate O atom in a lower half with respect to the Ga

atom. A plurality of such medium groups are bonded, so that a large group is formed.

[0074]

FIG. 6B illustrates a large group including three medium groups. Note that FIG. 6C illustrates an atomic arrangement in the case where the layered structure in FIG. 6B is observed from the *c*-axis direction.

[0075]

Here, since electric charge of a (hexacoordinate or pentacoordinate) In atom, electric charge of a (tetracoordinate) Zn atom, and electric charge of a (pentacoordinate) Ga atom are +3, +2, and +3, respectively, electric charge of a small group including any of an In atom, a Zn atom, and a Ga atom is 0. As a result, the total electric charge of a medium group having a combination of such small groups is always 0.

[0076]

In order to form the layered structure of the In-Ga-Zn oxide, a large group can be formed using not only the medium group illustrated in FIG. 6A but also a medium group in which the arrangement of the In atom, the Ga atom, and the Zn atom is different from that in FIG. 6A.

[0077]

Specifically, when the large group illustrated in FIG. 6B is repeated, a crystal of an In-Ga-Zn oxide can be obtained. Note that a layered structure of the obtained crystal of the In-Ga-Zn oxide can be expressed as a composition formula, $\text{InGaO}_3(\text{ZnO})_n$ (n is a natural number).

[0078]

In the case where $n = 1$ (InGaZnO_4), a crystal structure illustrated in FIG. 7A can be obtained, for example. Note that since a Ga atom and an In atom each have five ligands in the crystal structure in FIG. 7A as described in FIG. 4B, a structure in which Ga is replaced with In can be obtained.

[0079]

In the case where $n = 2$ ($\text{InGaZn}_2\text{O}_5$), a crystal structure illustrated in FIG. 7B can be obtained, for example. Note that since a Ga atom and an In atom each have five ligands in the crystal structure in FIG. 7B as described in FIG. 4B, a structure in which Ga is replaced with In can be obtained.

[0080]

The reason why the In-Ga-Zn oxide has a high proportion of crystals with surface structures of planes parallel to the *a-b* plane is described below.

[0081]

5 When a crystal has an equilibrium form, the area of a surface along a plane having a small surface energy becomes large. Also, cleavage of a crystal is likely to occur in a plane having a small surface energy. Calculation results of the surface energy of each plane are described below.

[0082]

10 Here, the surface energy refers to an energy obtained by subtracting the energy of a crystal structure from the energy of a surface structure and then dividing the value by a surface area.

[0083]

15 First principle calculation software, CASTEP, which is based on the density functional theory was used for the calculation, an ultrasoft type was used for pseudopotential, and the cut-off energy was 400 eV.

[0084]

20 FIGS. 8 to 11 each illustrate a crystal structure and a surface structure used for the calculation. Note that in the surface structures in FIGS. 8 to 11, a spatial portion indicates a vacuum. That is, a plane in contact with the spatial portion is a surface. Note that although there are both an upper surface and a lower surface, a lower space is omitted for easy understanding.

[0085]

25 The surface energy of a surface structure (1) in FIG. 8 is an average value of a surface energy of a (001) plane including In and O and a surface energy of a (001) plane including Ga and O. The surface energy of a surface structure (2) is an average value of a surface energy of a (001) plane including Ga and O and a surface energy of a (001) plane including Zn and O. The surface energy of a surface structure (3) is an average value of a surface energy of a (001) plane including Zn and O and a surface energy of a
30 (001) plane including In and O. The surface energy of the (001) plane including In and O, the surface energy of the (001) plane including Ga and O, and the surface energy of the (001) plane including Zn and O were calculated by simultaneously calculating the

obtained surface energies of the surface structure (1), the surface structure (2), and the surface structure (3). In this specification, planes parallel to an *a-b* plane are in some cases described for simplicity as a (001) plane. Note that in some cases, other planes (e.g., a (100) plane and a (10-1) plane) are described in a similar manner.

5 [0086]

A surface structure (4) illustrated in FIG. 9 is a (001) plane in which Ga and Zn are mixed, which exists both at an upper surface and a lower surface.

[0087]

Note that a structure illustrated in FIG. 10 and a structure illustrated in FIG. 11 are a (100) plane and a (10-1) plane, respectively. Note that the (100) plane and the (10-1) plane each include plural kinds of surface energies. Since there are all kinds of elements in the outermost surfaces of the (100) plane and the (10-1) plane, an average value of typical two surface energies was regarded here as a surface energy of each plane. In addition, two kinds of a surface structure (6) and a surface structure (7), which were
15 given as the (10-1) plane, were described as a (10-1) plane_a and a (10-1) plane_b, respectively, to distinguish between them.

[0088]

The surface energy of the surface structure (1) was 1.54 J/m².

[0089]

20 The surface energy of the surface structure (2) was 1.24 J/m².

[0090]

The surface energy of the surface structure (3) was 1.57 J/m².

[0091]

When the surface energies of the surface structure (1), the surface structure (2),
25 and the surface structure (3) were simultaneously calculated, the surface energy of the (001) plane including In and O was 1.88 J/m².

[0092]

When the surface energies of the surface structure (1), the surface structure (2), and the surface structure (3) were simultaneously calculated, the surface energy of the
30 (001) plane including Ga and O was 1.21 J/m².

[0093]

When the surface energies of the surface structure (1), the surface structure (2), and the surface structure (3) were simultaneously calculated, the surface energy of the (001) plane including Zn and O was 1.26 J/m^2 .

[0094]

5 The surface energy of the surface structure (4) was 0.35 J/m^2 .

[0095]

The surface energy of the surface structure (5) was 1.64 J/m^2 .

[0096]

The surface energy of the surface structure (6) was 1.72 J/m^2 .

10 [0097]

The surface energy of the surface structure (7) was 1.79 J/m^2 .

[0098]

The above calculation results show that the surface energy of the surface structure (4) is the smallest, i.e., a (001) plane in which Ga and Zn are mixed has the smallest surface energy when considered as a surface.

[0099]

Therefore, it can be seen that the crystal of the In-Ga-Zn oxide has high proportion of surface structures of planes parallel to the *a-b* plane.

[0100]

20 Further, one embodiment of the present invention is a transistor including the above oxide film as a channel region.

[0101]

Further, one embodiment of the present invention is a semiconductor device including the transistor.

25 [0102]

It is possible to provide a transistor which has stable electrical characteristics with the use of an oxide film with a high degree of crystallinity.

[0103]

30 In addition, it is possible to provide a highly reliable semiconductor device with the use of the transistor.

BRIEF DESCRIPTION OF DRAWINGS

[0104]

FIGS. 1A and 1B are schematic diagrams illustrating a state in which sputtered particles are separated from a sputtering target.

FIGS. 2A and 2B are schematic diagrams each illustrating a state in which sputtered particles reach a deposition surface.

FIGS. 3A and 3B illustrate a crystal structure of an oxide semiconductor of one embodiment of the present invention.

FIGS. 4A to 4E each illustrate a crystal structure of an oxide semiconductor of one embodiment of the present invention.

FIGS. 5A to 5C illustrate a crystal structure of an oxide semiconductor of one embodiment of the present invention.

FIGS. 6A to 6C illustrate a crystal structure of an oxide semiconductor of one embodiment of the present invention.

FIGS. 7A and 7B each illustrate a crystal structure of an oxide semiconductor of one embodiment of the present invention.

FIG. 8 illustrates a crystal structure and surface structures.

FIG. 9 illustrates a crystal structure and a surface structure.

FIG. 10 illustrates a crystal structure and a surface structure.

FIG. 11 illustrates a crystal structure and surface structures.

FIG. 12 is a top view which illustrates an example of a film formation apparatus.

FIGS. 13A to 13C illustrate a structure example of a film formation chamber.

FIGS. 14A to 14D each illustrate a positional relation of a sputtering target, a magnet, and a substrate holder.

FIGS. 15A and 15B are flow charts illustrating an example of a method for manufacturing a sputtering target.

FIGS. 16A to 16C are a top view and cross-sectional views illustrating an example of a transistor.

FIGS. 17A to 17C are a top view and cross-sectional views illustrating an example of a transistor;

FIGS. 18A to 18C are a top view and cross-sectional views illustrating an example of a transistor.

FIGS. 19A to 19C are a top view and cross-sectional views illustrating an

example of a transistor.

FIGS. 20A to 20C are a top view and cross-sectional views illustrating an example of a transistor.

FIGS. 21A to 21C are a top view and cross-sectional views illustrating an
5 example of a transistor.

FIGS. 22A and 22B are a circuit diagram and a cross-sectional view of a semiconductor device of one embodiment of the present invention.

FIGS. 23A and 23B are each a circuit diagram of a semiconductor device of one embodiment of the present invention.

10 FIGS. 24A and 24B are a circuit diagram and a cross-sectional view of a semiconductor device of one embodiment of the present invention.

FIG. 25 is a circuit diagram of a semiconductor device of one embodiment of the present invention.

15 FIGS. 26A to 26D are circuit diagrams, a cross-sectional view, and a graph showing electrical characteristics of a semiconductor device of one embodiment of the present invention.

FIGS. 27A to 27C are a circuit diagram, a graph showing electrical characteristics, and a cross-sectional view of a semiconductor device of one embodiment of the present invention.

20 FIGS. 28A to 28C are block diagrams illustrating a structure of a CPU of one embodiment of the present invention.

FIG. 29 is a circuit diagram of part of a pixel of a display device using an EL element of one embodiment of the present invention.

25 FIGS. 30A to 30C are a top view and a cross-sectional view, and a cross-sectional view of a light-emitting layer, of a display device using an EL element of one embodiment of the present invention.

FIGS. 31A and 31B are each a cross-sectional view of a display device using an EL element of one embodiment of the present invention.

30 FIG. 32 is a circuit diagram of a pixel of a display device using a liquid crystal element of one embodiment of the present invention.

FIGS. 33A to 33C are each a cross-sectional view of a display device using a liquid crystal element of one embodiment of the present invention.

FIGS. 34A to 34D each illustrate an electronic device of one embodiment of the present invention.

FIGS. 35A, 35B-1 and 35B-2, and 35C are diagrams for describing a discharge state when sputtering is performed using an AC power source.

5

BEST MODE FOR CARRYING OUT THE INVENTION

[0105]

Embodiments of the present invention are described in detail below with reference to the accompanying drawings. However, the present invention is not limited to the description below, and it is easily understood by those skilled in the art that modes and details thereof can be modified in various ways. Therefore, the present invention is not construed as being limited to description of the embodiments. In describing structures of the present invention with reference to the drawings, the same reference numerals are used in common for the same portions in different drawings. Note that the same hatch pattern is applied to similar parts, and the similar parts are not especially denoted by reference numerals in some cases.

15

[0106]

Note that the ordinal numbers such as "first" and "second" in this specification are used for convenience and do not denote the order of steps or the stacking order of layers. In addition, the ordinal numbers in this specification do not denote particular names which specify the present invention.

20

[0107]

[Embodiment 1]

In this embodiment, a method for using a sputtering target including a polycrystalline oxide is described.

25

[0108]

FIG. 1A is a schematic diagram illustrating a state in which an ion 1001 collides with a sputtering target 1000 to separate sputtered particles 1002 from the sputtering target 1000. Note that the sputtered particle 1002 may have the shape of a hexagonal cylinder whose hexagonal planes are parallel to an *a-b* plane. In that case, the direction perpendicular to the hexagonal planes is a *c*-axis direction (see FIG. 1B). The diameter of the plane of the sputtered particle 1002, which is parallel to the *a-b*

30

plane, is approximately greater than or equal to 1 nm and less than or equal to 30 nm or greater than or equal to 1 nm and less than or equal to 10 nm, though it differs depending on the kind of oxide. Note that an oxygen cation is used as the ion 1001. An argon cation may be used in addition to the oxygen cation. Note that a cation of another rare gas may be used instead of an argon cation.

[0109]

With the use of an oxygen cation as the ion 1001, plasma damage at the film formation can be alleviated. Thus, when the ion 1001 collides with the surface of the sputtering target 1000, a deterioration in crystallinity of the sputtering target 1000 can be suppressed or a change of the sputtering target 1000 into an amorphous state can be suppressed.

[0110]

It is preferable that the separated sputtered particles 1002 be positively charged. However, there is no particular limitation on the timing at which the sputtered particles 1002 are positively charged. Specifically, a sputtered particle 1002 is in some cases positively charged by being exposed to plasma. Alternatively, a sputtered particle 1002 is in some cases positively charged by receiving an electric charge at the collision of the ion 1001. Further alternatively, a sputtered particle 1002 is in some cases positively charged in such a manner that the ion 1001 which is an oxygen cation is bonded with a side, top, or bottom surface of the sputtered particle 1002.

[0111]

In the sputtered particle 1002, the corners of the hexagonal plane are positively charged, whereby positive charges of the hexagonal plane repel each other. Thus, flat-plate shapes of the sputtered particles 1002 can be maintained.

[0112]

It is preferable to use a direct-current (DC) power source to positively charge the corners of the hexagonal plane of the sputtered particle 1002. Note that a radio frequency (RF) power source or an alternating-current (AC) power source can also be used. Note that it is difficult to use an RF power source for a sputtering apparatus which is capable of performing deposition to a large-sized substrate. In addition, a DC power source is preferred to an AC power source from the viewpoint below.

[0113]

In the AC power source, adjacent targets alternately have a cathode potential and an anode potential. In a period A shown in FIG. 35A, a target 1 functions as a cathode and a target 2 functions as an anode as illustrated in FIG. 35B-1. In a period B shown in FIG. 35A, the target 1 functions as an anode and the target 2 functions as a cathode as illustrated in FIG. 35B-2. The total time of the period A and the period B is 20 μ sec to 50 μ sec and the period A and the period B are repeated at a constant frequency.

[0114]

In the case where the sputtered particle 1002 is positively charged, positive charges in the sputtered particle 1002 repel each other, whereby flat-plate shapes of the sputtered particles 1002 can be maintained. However, in the case where the AC power source is used, there is time during which an electric field is not applied instantaneously; therefore, some charges of the sputtered particle 1002 are lost and the structure of the sputtered particle might be broken (see FIG. 35C). Thus, a DC power source is preferred to an AC power source.

[0115]

A state in which sputtered particles are deposited on a deposition surface is described below with reference to FIGS. 2A and 2B. Note that FIG. 2A illustrates the case where film formation is performed with substrate heating, whereas FIG. 2B illustrates the case where film formation is performed without substrate heating.

[0116]

As illustrated in FIG. 2A, in the case with substrate heating, one sputtered particle 1002 moves to a region of the deposition surface 1003, where other sputtered particles 1002 have not been deposited yet, and migration of the sputtered particle 1002 occurs, whereby the sputtered particle 1002 is bonded to the side of the sputtered particles which are already deposited. In this manner, the sputtered particles 1002 are spread over the deposition surface 1003 with flat plate planes facing upward. The *c*-axes of the deposited sputtered particles 1002 are aligned in one direction perpendicular to the deposition surface 1003; accordingly, a CAAC-OS film is obtained. Moreover, an oxide film which is obtained by the deposition has a uniform thickness and a uniform crystal orientation.

[0117]

The CAAC-OS film which is obtained by such a mechanism has high crystallinity even on an amorphous surface, a surface of an amorphous insulating film, a surface of an amorphous oxide film, or the like.

[0118]

5 As illustrated in FIG. 2B, in the case without substrate heating, sputtered particles 1002 fall irregularly to a deposition surface 1003. Thus, the sputtered particles 1002 are deposited randomly also in a region where other sputtered particles 1002 are already deposited. That is, an oxide film which is obtained by the deposition has neither a uniform thickness nor a uniform crystal orientation. The oxide film
10 which is obtained in such a manner is a microcrystalline oxide film because the crystallinity of flat plate-like sputtered particles 1002 is maintained to some extent.

[0119]

Note that the deposition surface 1003 preferably has an insulating property. With the deposition surface 1003 having an insulating property, the sputtered particles
15 1002 which are deposited on the deposition surface 1003 are unlikely to lose positive charges. However, in the case where the deposition rate of the sputtered particles 1002 is less than the rate at which a positive charge is lost, the deposition surface 1003 may have conductivity.

[0120]

20 With the use of a sputtering target in the way as described above, an oxide film having a uniform thickness and a uniform crystal orientation can be formed.

[0121]

This embodiment can be implemented in appropriate combination with any of the other embodiments.

25 [0122]

[Embodiment 2]

In this embodiment, a film formation apparatus for forming the oxide film with a high degree of crystallinity described in Embodiment 1 is described.

[0123]

30 First, a structure of a film formation apparatus which allows the entry of few impurities into a film during film formation is described with reference to FIG. 12 and FIGS. 13A to 13C.

[0124]

FIG. 12 is a top view schematically illustrating a single wafer multi-chamber film formation apparatus 4000. The film formation apparatus 4000 includes an atmosphere-side substrate supply chamber 4001 including a cassette port 4101 for holding a substrate and an alignment port 4102 for performing alignment of a substrate, an atmosphere-side substrate transfer chamber 4002 through which a substrate is transferred from the atmosphere-side substrate supply chamber 4001, a load lock chamber 4003a where a substrate is carried and the pressure inside the chamber is switched from an atmospheric pressure to a reduced pressure or from a reduced pressure to an atmospheric pressure, an unload lock chamber 4003b where a substrate is carried out and the pressure inside the chamber is switched from a reduced pressure to an atmospheric pressure or from an atmospheric pressure to a reduced pressure, a transfer chamber 4004 through which a substrate is transferred in a vacuum, a substrate heating chamber 4005 where a substrate is heated, and film formation chambers 4006a, 4006b, and 4006c in each of which a target is placed for film formation.

[0125]

Note that a plurality of the cassette ports 4101 may be provided as illustrated in FIG. 12 (in FIG. 12, three cassette ports 4101 are provided).

[0126]

The atmosphere-side substrate transfer chamber 4002 is connected to the load lock chamber 4003a and the unload lock chamber 4003b, the load lock chamber 4003a and the unload lock chamber 4003b are connected to the transfer chamber 4004, and the transfer chamber 4004 is connected to the substrate heating chamber 4005 and the film formation chambers 4006a, 4006b, and 4006c.

[0127]

Gate valves 4104 are provided for connecting portions between chambers so that each chamber except the atmosphere-side substrate supply chamber 4001 and the atmosphere-side substrate transfer chamber 4002 can be independently kept under vacuum. Moreover, the atmosphere-side substrate transfer chamber 4002 and the transfer chamber 4004 each include a transfer robot 4103, with which a glass substrate can be transferred.

[0128]

Further, it is preferable that the substrate heating chamber 4005 also serve as a plasma treatment chamber. In the film formation apparatus 4000, it is possible to transfer a substrate without exposure to the air between treatment and treatment; therefore, adsorption of impurities on a substrate can be suppressed. In addition, the order of film formation, heat treatment, or the like can be freely determined. Note that the number of the transfer chambers, the number of the film formation chambers, the number of the load lock chambers, the number of the unload lock chambers, and the number of the substrate heating chambers are not limited to the above, and the numbers thereof can be set as appropriate depending on the space for placement or the process conditions.

[0129]

Next, FIG. 13A, FIG. 13B, and FIG. 13C are a cross-sectional view taken along dashed-dotted line X1-X2, a cross-sectional view taken along dashed-dotted line Y1-Y2, and a cross-sectional view taken along dashed-dotted line Y2-Y3, respectively, in the film formation apparatus 4000 illustrated in FIG. 12.

[0130]

FIG. 13A is a cross section of the substrate heating chamber 4005 and the transfer chamber 4004, and the substrate heating chamber 4005 includes a plurality of heating stages 4105 which can hold a substrate. Note that although the substrate heating chamber 4005 including the seven heating stages 4105 is illustrated in FIG. 13A, one embodiment of the present invention is not limited to such a structure. The number of heating stages 4105 may be greater than or equal to one and less than seven. Alternatively, the number of heating stages 4105 may be greater than or equal to eight. It is preferable to increase the number of the heating stages 4105 because a plurality of substrates can be subjected to heat treatment at the same time, which leads to an increase in productivity. Further, the substrate heating chamber 4005 is connected to a vacuum pump 4200 through a valve. As the vacuum pump 4200, a dry pump and a mechanical booster pump can be used, for example.

[0131]

As heating mechanism which can be used for the substrate heating chamber 4005, a resistance heater or the like may be used for heating, for example. Alternatively, heat conduction or heat radiation from a medium such as a heated gas may be used as the

heating mechanism. For example, a rapid thermal annealing (RTA) apparatus such as a gas rapid thermal annealing (GRTA) apparatus or a lamp rapid thermal annealing (LRTA) apparatus can be used. The LRTA apparatus is an apparatus for heating an object by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high-pressure sodium lamp, or a high-pressure mercury lamp. In the GRTA apparatus, heat treatment is performed using a high-temperature gas. An inert gas is used as the gas.

[0132]

Moreover, the substrate heating chamber 4005 is connected to a refiner 4301 through a mass flow controller 4300. Note that although refiner 4301 and the mass flow controller 4300 can be provided for each of a plurality of kinds of gases, only one refiner 4301 and one mass flow controller 4300 are provided for easy understanding. As the gas introduced to the substrate heating chamber 4005, a gas whose dew point is -80°C or lower, preferably -100°C or lower can be used; for example, an oxygen gas, a nitrogen gas, and a rare gas (e.g., an argon gas) are used.

[0133]

The transfer chamber 4004 includes the transfer robot 4103. The transfer robot 4103 includes a plurality of movable portions and an arm for holding a substrate and can transfer a substrate to each chamber. Further, the transfer chamber 4004 is connected to a vacuum pump 4200 and a cryopump 4201 through valves. With such a structure, evacuation can be performed using the vacuum pump 4200 when the pressure inside the transfer chamber 4004 is in the range of an atmospheric pressure to a low vacuum (approximately 0.1 Pa to several hundred Pa) and then, by switching the valves, evacuation can be performed using the cryopump 4201 when the pressure inside the transfer chamber 4004 is in the range of middle vacuum to ultra-high vacuum (0.1 Pa to $1 \times 10^{-7}\text{ Pa}$).

[0134]

Alternatively, two or more cryopumps 4201 may be connected in parallel to the transfer chamber 4004. With such a structure, even when one of the cryopumps is in regeneration, evacuation can be performed using any of the other cryopumps. Note that the above regeneration refers to treatment for discharging molecules (or atoms)

entrapped in the cryopump. When molecules (or atoms) are entrapped too much in a cryopump, the evacuation capability of the cryopump is lowered; therefore, regeneration is performed regularly.

[0135]

5 FIG. 13B is a cross section of the film formation chamber 4006b, the transfer chamber 4004, and the load lock chamber 4003a.

[0136]

Here, the details of the film formation chamber (sputtering chamber) are described with reference to FIG. 13B. The film formation chamber 4006b illustrated in
10 FIG. 13B includes a target 4106, an attachment protection plate 4107, and a substrate stage 4108. Note that here, a substrate 4109 is provided on the substrate stage 4108. Although not illustrated, the substrate stage 4108 may include a substrate holding mechanism which holds the substrate 4109, a rear heater which heats the substrate 4109 from the back surface, or the like.

15 [0137]

Note that the substrate stage 4108 is held substantially vertically to a floor during film formation and is held substantially parallel to the floor when the substrate is delivered. In FIG. 13B, the position where the substrate stage 4108 is held when the substrate is delivered is denoted by a dashed line. With such a structure, the
20 probability that dust or a particle which might be entered at the film formation is attached to the substrate 4109 can be suppressed as compared to the case where the substrate stage 4108 is held parallel to the floor. However, there is a possibility that the substrate 4109 falls when the substrate stage 4108 is held vertically (90°) to the floor; therefore, the angle of the substrate stage 4108 to the floor is preferably wider
25 than or equal to 80° and narrower than 90°.

[0138]

The attachment protection plate 4107 can suppress deposition of a particle which is sputtered from the target 4106 on a region where deposition is not needed. Moreover, the attachment protection plate 4107 is preferably processed to prevent
30 accumulated sputtered particles from being separated. For example, blasting treatment which increases surface roughness may be performed, or roughness may be formed on

the surface of the attachment protection plate 4107.

[0139]

The film formation chamber 4006b is connected to a mass flow controller 4300 through a gas heating system 4302, and the gas heating system 4302 is connected to a refiner 4301 through the mass flow controller 4300. With the gas heating system 4302, a gas to be introduced to the film formation chamber 4006b can be heated to a temperature higher than or equal to 40 °C and lower than or equal to 400 °C, preferably higher than or equal to 50 °C and lower than or equal to 200 °C. Note that although the gas heating system 4302, the mass flow controller 4300, and the refiner 4301 can be provided for each of a plurality of kinds of gases, only one gas heating system 4302, one mass flow controller 4300, and one refiner 4301 are provided for easy understanding. As the gas introduced to the film formation chamber 4006b, a gas whose dew point is -80 °C or lower, preferably -100 °C or lower can be used; for example, an oxygen gas, a nitrogen gas, and a rare gas (e.g., an argon gas) are used.

[0140]

A facing-target-type sputtering apparatus may be provided in the film formation chamber 4006b. The specific positional relation of a sputtering target, a magnet, and a substrate holder is described with reference to FIGS. 14A to 14D.

[0141]

Each of the structures illustrated in FIGS. 14A to 14D includes a first sputtering target 4032a, a second sputtering target 4032b, first cathode magnets 4033a, second cathode magnets 4033b, and a substrate holder 4035. That is, FIGS. 14A to 14D differ only in positions of the above components.

[0142]

In the structure illustrated in FIG. 14A, the first sputtering target 4032a and the second sputtering target 4032b are provided parallel to face each other. The first cathode magnet 4033a and the second cathode magnet 4033b are provided so that the same polarities face each other. Note that although the first cathode magnet 4033a and the second cathode magnet 4033b are provided so that the S-poles thereof face each other, they may be provided so that the N-poles thereof face each other. The substrate holder 4035 is provided on a lower side of a region where the first sputtering target

4032a and the second sputtering target 4032b face each other; however, the substrate holder 4035 may be provided on an upper side thereof. Alternatively, the substrate holder 4035 may be provided on the upper side and the lower side thereof. When the substrate holder 4035 is provided on the upper side and the lower side, the productivity of the oxide film can be improved. Note that although the substrate holder 4035 is provided so that the top surface thereof is perpendicular to the top surfaces of the first sputtering target 4032a and the second sputtering target 4032b, the substrate holder 4035 may be inclined. With the positional relation illustrated in FIG. 14A, the deposition rate can be increased.

[0143]

In the structure illustrated in FIG. 14B, the first sputtering target 4032a and the second sputtering target 4032b are provided parallel to face each other. The first cathode magnet 4033a and the second cathode magnet 4033b are provided so that different polarities face each other. The substrate holder 4035 is provided on a lower side of a region where the first sputtering target 4032a and the second sputtering target 4032b face each other; however, the substrate holder 4035 may be provided on an upper side thereof. Alternatively, the substrate holder 4035 may be provided on the upper side and the lower side thereof. When the substrate holder 4035 is provided on the upper side and the lower side, the productivity of the oxide film can be improved. Note that although the substrate holder 4035 is provided so that the top surface thereof is perpendicular to the top surfaces of the first sputtering target 4032a and the second sputtering target 4032b, the substrate holder 4035 may be inclined. With the positional relation illustrated in FIG. 14B, the deposition rate can be increased.

[0144]

In the structure illustrated in FIG. 14C, the first sputtering target 4032a and the second sputtering target 4032b are provided to face each other with symmetrical inclination (in an inverted V shape). The first cathode magnet 4033a and the second cathode magnet 4033b are provided so that the same polarities face each other. Note that although the first cathode magnet 4033a and the second cathode magnet 4033b are provided so that the S-poles thereof face each other, they may be provided so that the N-poles thereof face each other. The substrate holder 4035 is provided on a lower side of a region where the first sputtering target 4032a and the second sputtering target

4032b face each other (the side on which a distance between the targets is larger). With the positional relation illustrated in FIG. 14C, the deposition rate can be increased because sputtered particles efficiently fall to the substrate holder 4035.

[0145]

5 In the structure illustrated in FIG. 14D, the first sputtering target 4032a and the second sputtering target 4032b are provided to face each other with symmetrical inclination (in an inverted V shape). The first cathode magnet 4033a and the second cathode magnet 4033b are provided so that different polarities face each other. The substrate holder 4035 is provided on a lower side of a region where the first sputtering
10 target 4032a and the second sputtering target 4032b face each other (the side on which a distance between the targets is larger). With the positional relation illustrated in FIG. 14D, the deposition rate can be increased because sputtered particles efficiently fall to the substrate holder 4035.

[0146]

15 In each of the above-described structures of the facing-target-type sputtering apparatus, plasma is confined between the targets; therefore, plasma damage to a substrate can be reduced. Further, step coverage can be improved because an incident angle of a sputtered particle to the substrate can be made smaller depending on the inclination of the target.

20 [0147]

Note that a parallel plate type sputtering apparatus or an ion beam sputtering apparatus may be provided in the film formation chamber 4006b.

[0148]

25 In the case where the refiner is provided just before the gas is introduced, the length of a pipe between the refiner and the film formation chamber 4006b is less than or equal to 10 m, preferably less than or equal to 5 m, more preferably less than or equal to 1 m. When the length of the pipe is less than or equal to 10 m, less than or equal to 5m, or less than or equal to 1 m, the effect of the release of gas from the pipe can be reduced accordingly. As the pipe for the gas, a metal pipe the inside of which is covered with an
30 iron fluoride, an aluminum oxide, a chromium oxide, or the like can be used. With the above pipe, the amount of released gas containing impurities is made small and the entry of impurities into the gas can be reduced as compared with a SUS316L-EP pipe, for

example. Further, a high-performance ultra-compact metal gasket joint (UPG joint) may be used as a joint of the pipe. A structure where all the materials of the pipe are metals is preferable because the effect of the generated released gas or the external leakage can be reduced compared with a structure where resin or the like is used.

5 [0149]

The film formation chamber 4006b is connected to a turbo molecular pump 4202 and a vacuum pump 4200 through valves.

[0150]

In addition, the film formation chamber 4006b is provided with a cryotrap 4110.

10 [0151]

The cryotrap 4110 is a mechanism which can adsorb a molecule (or an atom) having a relatively high melting point, such as water. The turbo molecular pump 4202 is capable of stably evacuating a large-sized molecule (or atom), needs low frequency of maintenance, and thus enables high productivity, whereas it has a low capability in
15 evacuating hydrogen and water. Hence, the cryotrap 4110 is connected to the film formation chamber 4006b so as to have a high capability in evacuating water or the like. The temperature of a refrigerator of the cryotrap 4110 is set to be lower than or equal to 100 K, preferably lower than or equal to 80 K. In the case where the cryotrap 4110 includes a plurality of refrigerators, it is preferable to set the temperature of each
20 refrigerator at a different temperature because efficient evacuation is possible. For example, the temperatures of a first-stage refrigerator and a second-stage refrigerator may be set at lower than or equal to 100 K and lower than or equal to 20 K, respectively.

[0152]

Note that the evacuation method of the film formation chamber 4006b is not
25 limited to the above, and a structure similar to that in the evacuation method described in the transfer chamber 4004 (the evacuation method using the cryopump and the vacuum pump) may be employed. Needless to say, the evacuation method of the transfer chamber 4004 may have a structure similar to that of the film formation chamber 4006b (the evacuation method using the turbo molecular pump and the vacuum
30 pump).

[0153]

Note that in each of the above transfer chamber 4004, the substrate heating

chamber 4005, and the film formation chamber 4006b, the back pressure (total pressure) and the partial pressure of each gas molecule (atom) are preferably set as follows. In particular, the back pressure and the partial pressure of each gas molecule (atom) in the film formation chamber 4006b need to be noted because impurities might enter a film to be formed.

[0154]

In each of the above chambers, the back pressure (total pressure) is less than or equal to 1×10^{-4} Pa, preferably less than or equal to 3×10^{-5} Pa, more preferably less than or equal to 1×10^{-5} Pa. In each of the above chambers, the partial pressure of a gas molecule (atom) having a mass-to-charge ratio (m/z) of 18 is less than or equal to 3×10^{-5} Pa, preferably less than or equal to 1×10^{-5} Pa, more preferably less than or equal to 3×10^{-6} Pa. Moreover, in each of the above chambers, the partial pressure of a gas molecule (atom) having a mass-to-charge ratio (m/z) of 28 is less than or equal to 3×10^{-5} Pa, preferably less than or equal to 1×10^{-5} Pa, more preferably less than or equal to 3×10^{-6} Pa. Further, in each of the above chambers, the partial pressure of a gas molecule (atom) having a mass-to-charge ratio (m/z) of 44 is less than or equal to 3×10^{-5} Pa, preferably less than or equal to 1×10^{-5} Pa, more preferably less than or equal to 3×10^{-6} Pa.

[0155]

Note that a total pressure and a partial pressure in a vacuum chamber can be measured using a mass analyzer. For example, Qulee CGM-051, a quadrupole mass analyzer (also referred to as Q-mass) manufactured by ULVAC, Inc. may be used.

[0156]

Moreover, the above transfer chamber 4004, the substrate heating chamber 4005, and the film formation chamber 4006b preferably have a small amount of external leakage or internal leakage.

[0157]

For example, in each of the above transfer chamber 4004, the substrate heating chamber 4005, and the film formation chamber 4006b, the leakage rate is less than or equal to 3×10^{-6} Pa·m³/s, preferably less than or equal to 1×10^{-6} Pa·m³/s. The leakage rate of a gas molecule (atom) having a mass-to-charge ratio (m/z) of 18 is less than or

equal to 1×10^{-7} Pa·m³/s, preferably less than or equal to 3×10^{-8} Pa·m³/s. The leakage rate of a gas molecule (atom) having a mass-to-charge ratio (m/z) of 28 is less than or equal to 1×10^{-5} Pa·m³/s, preferably less than or equal to 1×10^{-6} Pa·m³/s. The leakage rate of a gas molecule (atom) having a mass-to-charge ratio (m/z) of 44 is less than or equal to 3×10^{-6} Pa·m³/s, preferably less than or equal to 1×10^{-6} Pa·m³/s.

[0158]

Note that a leakage rate can be derived from the total pressure and partial pressure measured using the mass analyzer.

[0159]

The leakage rate depends on external leakage and internal leakage. The external leakage refers to inflow of gas from the outside of a vacuum system through a minute hole, a sealing defect, or the like. The internal leakage is due to leakage through a partition, such as a valve, in a vacuum system or due to released gas from an internal member. Measures need to be taken from both aspects of external leakage and internal leakage in order that the leakage rate is set to be less than or equal to the above value.

[0160]

For example, an open/close portion of the film formation chamber 4006b can be sealed with a metal gasket. For the metal gasket, metal covered with an iron fluoride, an aluminum oxide, or a chromium oxide is preferably used. The metal gasket realizes higher adhesion than an O-ring, and can reduce the external leakage. Further, with the use of the metal covered with an iron fluoride, an aluminum oxide, a chromium oxide, or the like which is in the passive state, the release of gas containing impurities released from the metal gasket is suppressed, so that the internal leakage can be reduced.

[0161]

For a member of the film formation apparatus 4000, aluminum, chromium, titanium, zirconium, nickel, or vanadium, which releases a smaller amount of gas containing impurities, is used. Alternatively, for the above member, an alloy containing iron, chromium, nickel, and the like covered with the above material may be used. The alloy containing iron, chromium, nickel, and the like is rigid, resistant to heat, and suitable for processing. Here, when surface unevenness of the member is decreased by polishing or the like to reduce the surface area, the release of gas can be reduced.

[0162]

Alternatively, the above member of the film formation apparatus 4000 may be covered with an iron fluoride, an aluminum oxide, a chromium oxide, or the like.

[0163]

5 The member of the film formation apparatus 4000 is preferably formed with only metal as much as possible. For example, in the case where a viewing window formed with quartz or the like is provided, it is preferable that the surface of the viewing window be thinly covered with an iron fluoride, an aluminum oxide, a chromium oxide, or the like so as to suppress release of gas.

10 [0164]

When an adsorbate is present in the film formation chamber, the adsorbate does not affect the pressure in the film formation chamber because it is adsorbed onto an inner wall or the like; however, the adsorbate causes gas to be released when the inside of the film formation chamber is evacuated. Therefore, although there is no correlation
15 between the leakage rate and the evacuation rate, it is important that the adsorbate present in the film formation chamber be desorbed as much as possible and evacuation be performed in advance with the use of a pump with high evacuation capability. Note that the film formation chamber may be baked to promote desorption of the adsorbate. By the baking, the film formation rate of the adsorbate can be increased approximately
20 tenfold. The baking can be performed at a temperature in the range of 100 °C to 450 °C. At this time, when the adsorbate is removed while an inert gas is introduced to the film formation chamber, the film formation rate of water or the like, which is difficult to be desorbed simply by evacuation, can be further increased. Note that when the inert gas to be introduced is heated to substantially the same temperature as the baking temperature of
25 the film formation chamber, the desorption rate of the adsorbate can be further increased. Here, a rare gas is preferably used as an inert gas. Depending on the kind of a film to be formed, oxygen or the like may be used instead of an inert gas. For example, in the case of forming an oxide, the use of oxygen which is the main component of the oxide is preferable in some cases.

30 [0165]

Alternatively, treatment for evacuating the inside of the film formation chamber is preferably performed a certain period of time after heated oxygen, a heated inert gas

such as a rare gas, or the like is introduced to increase a pressure in the film formation chamber. The introduction of the heated gas can desorb the adsorbate in the film formation chamber, and the impurities present in the film formation chamber can be reduced. Note that an advantageous effect can be achieved when this treatment is repeated more than or equal to twice and less than or equal to 30 times, preferably more than or equal to 5 times and less than or equal to 15 times. Specifically, an inert gas, oxygen, or the like with a temperature higher than or equal to 40 °C and lower than or equal to 400 °C, preferably higher than or equal to 50 °C and lower than or equal to 200 °C is introduced to the film formation chamber, so that the pressure therein can be kept to be greater than or equal to 0.1 Pa and less than or equal to 10 kPa, preferably greater than or equal to 1 Pa and less than or equal to 1 kPa, more preferably greater than or equal to 5 Pa and less than or equal to 100 Pa in the time range of 1 minute to 300 minutes, preferably 5 minutes to 120 minutes. After that, the inside of the film formation chamber is evacuated in the time range of 5 minutes to 300 minutes, preferably 10 minutes to 120 minutes.

[0166]

The rate of desorption of the adsorbate can be further increased also by dummy film formation. Here, the dummy film formation refers to film formation on a dummy substrate by a sputtering method or the like, in which a film is deposited on the dummy substrate and the inner wall of the film formation chamber so that impurities in the film formation chamber and an adsorbate on the inner wall of the film formation chamber are confined in the film. For a dummy substrate, a substrate which releases a smaller amount of gas is preferably used. By performing dummy film formation, impurity concentration in a film to be formed later can be reduced. Note that the dummy film formation may be performed at the same time as the baking of the film formation chamber.

[0167]

Next, the details of the transfer chamber 4004 and the load lock chamber 4003a illustrated in FIG. 13B and the atmosphere-side substrate transfer chamber 4002 and the atmosphere-side substrate supply chamber 4001 illustrated in FIG. 13C are described. Note that FIG. 13C is a cross section of the atmosphere-side substrate transfer chamber

4002 and the atmosphere-side substrate supply chamber 4001.

[0168]

For the transfer chamber 4004 illustrated in FIG. 13B, the description of the transfer chamber 4004 illustrated in FIG. 13A can be referred to.

5 [0169]

The load lock chamber 4003a includes a substrate delivery stage 4111. When a pressure in the load lock chamber 4003a becomes an atmospheric pressure by being increased from a reduced pressure, the substrate delivery stage 4111 receives a substrate from the transfer robot 4103 provided in the atmosphere-side substrate transfer chamber 4002. After that, the load lock chamber 4003a is evacuated into vacuum so that the pressure therein becomes a reduced pressure and then the transfer robot 4103 provided in the transfer chamber 4004 receives the substrate from the substrate delivery stage 4111.

[0170]

15 Further, the load lock chamber 4003a is connected to a vacuum pump 4200 and a cryopump 4201 through valves. For a method for connecting evacuation systems such as the vacuum pump 4200 and the cryopump 4201, the description of the method for connecting the transfer chamber 4004 can be referred to, and the description thereof is omitted here. Note that the unload lock chamber 4003b illustrated in FIG. 12 can have a structure similar to that in the load lock chamber 4003a.

20 [0171]

The atmosphere-side substrate transfer chamber 4002 includes the transfer robot 4103. The transfer robot 4103 can deliver a substrate from the cassette port 4101 to the load lock chamber 4003a or deliver a substrate from the load lock chamber 4003a to the cassette port 4101. Further, a mechanism for suppressing entry of dust or a particle, such as high efficiency particulate air (HEPA) filter, may be provided above the atmosphere-side substrate transfer chamber 4002 and the atmosphere-side substrate supply chamber 4001.

[0172]

30 The atmosphere-side substrate supply chamber 4001 includes a plurality of the cassette ports 4101. The cassette port 4101 can hold a plurality of substrates.

[0173]

When an oxide film is formed with the use of the above film formation apparatus, the entry of impurities into the oxide film can be suppressed. Further, when a film in contact with the oxide film is formed with the use of the above film formation apparatus, the entry of impurities into the oxide film from the film in contact therewith can be suppressed.

[0174]

Next, a method for forming a CAAC-OS film with the use of the above film formation apparatus is described.

[0175]

In order to form the oxide film, the sputtering target described in Embodiment 1 is used.

[0176]

The surface temperature of the sputtering target is set to be lower than or equal to 100 °C, preferably lower than or equal to 50 °C, more preferably approximately room temperature (typically, 25°C). In a sputtering apparatus for a large substrate, a large sputtering target is often used. However, it is difficult to form a sputtering target for a large substrate without a juncture. In fact, a plurality of sputtering targets are arranged so that there is as little space as possible therebetween to obtain a large shape; however, a slight space is inevitably generated. When the surface temperature of the sputtering target increases, in some cases, Zn or the like is volatilized from such a slight space and the space might be expanded gradually. When the space expands, a metal of a backing plate or a metal used for adhesion might be sputtered and cause an increase in impurity concentration. Thus, it is preferable that the sputtering target be cooled sufficiently.

[0177]

Specifically, for the backing plate, a metal having high conductivity and a high heat dissipation property (specifically Cu) is used. The sputtering target can be cooled efficiently by making a sufficient amount of cooling water flow through a water channel which is formed in the backing plate.

[0178]

The oxide film is formed in an oxygen gas atmosphere with a substrate heating temperature higher than or equal to 100 °C and lower than or equal to 600 °C, preferably

higher than or equal to 150 °C and lower than or equal to 550 °C, more preferably higher than or equal to 200 °C and lower than or equal to 500 °C. The thickness of the oxide film is greater than or equal to 1 nm and less than or equal to 40 nm, preferably greater than or equal to 3 nm and less than or equal to 20 nm. As the substrate heating temperature during the film formation is higher, the impurity concentration in the obtained oxide film is lower. Further, migration of sputtered particles on a deposition surface is likely to occur; therefore, the atomic arrangement in the oxide film is ordered and the density thereof is increased, so that a CAAC-OS film with a high degree of crystallinity is formed easily. Furthermore, when the film formation is performed in an oxygen gas atmosphere, plasma damage is alleviated and a surplus atom such as a rare gas atom is not contained in the oxide film, whereby a CAAC-OS film with a high degree of crystallinity is formed easily. Note that the film formation may be performed in a mixed atmosphere including an oxygen gas and a rare gas. In that case, the percentage of an oxygen gas is set to be greater than or equal to 30 vol.%, preferably greater than or equal to 50 vol.%, more preferably greater than or equal to 80 vol.%.
[0179]

Note that in the case where the sputtering target includes Zn, plasma damage is alleviated by the film formation in an oxygen gas atmosphere; thus, an oxide film in which Zn is unlikely to be volatilized can be obtained.

[0180]

The oxide film is formed under conditions in which the film formation pressure is less than or equal to 0.8 Pa, preferably less than or equal to 0.4 Pa, and the distance between the sputtering target and a substrate is less than or equal to 100 mm, preferably less than or equal to 40 mm, more preferably less than or equal to 25 mm. When the oxide film is formed under such a condition, the frequency of the collision between a sputtered particle and another sputtered particle, a gas molecule, or an ion can be reduced. That is, depending on the film formation pressure, the distance between the sputtering target and the substrate is made shorter than the mean free path of a sputtered particle, a gas molecule, or an ion, so that the entry of impurities into the film can be reduced.

[0181]

For example, when the pressure is 0.4 Pa and the temperature is 25 °C (the

absolute temperature is 298 K), a hydrogen molecule (H_2) has a mean free path of 48.7 mm, a helium atom (He) has a mean free path of 57.9 mm, a water molecule (H_2O) has a mean free path of 31.3 mm, an ethane molecule (CH_4) has a mean free path of 13.2 mm, a neon atom (Ne) has a mean free path of 42.3 mm, a nitrogen molecule (N_2) has a mean free path of 23.2 mm, a carbon monoxide molecule (CO) has a mean free path of 16.0 mm, an oxygen molecule (O_2) has a mean free path of 26.4 mm, an argon atom (Ar) has a mean free path of 28.3 mm, a carbon dioxide molecule (CO_2) has a mean free path of 10.9 mm, a krypton atom (Kr) has a mean free path of 13.4 mm, and a xenon atom (Xe) has a mean free path of 9.6 mm. Note that doubling of the pressure halves a mean free path and doubling of the absolute temperature doubles a mean free path.

[0182]

The mean free path depends on pressure, temperature, and the diameter of a molecule (atom). In the case where pressure and temperature are constant, as the diameter of a molecule (atom) is larger, the mean free path is shorter. Note that the diameters of the molecules (atoms) are as follows: H_2 : 0.218 nm; He: 0.200 nm; H_2O : 0.272 nm; CH_4 : 0.419 nm; Ne: 0.234 nm; N_2 : 0.316 nm; CO: 0.380 nm; O_2 : 0.296 nm; Ar: 0.286 nm; CO_2 : 0.460 nm; Kr: 0.415 nm; and Xe: 0.491 nm.

[0183]

Thus, as the diameter of a molecule (atom) is larger, the mean free path is shorter and the degree of crystallinity is lowered due to the large diameter of the molecule (atom) when the molecule (atom) enters the film. For this reason, it can be said that, for example, a molecule (atom) whose diameter is larger than that of Ar is likely to behave as an impurity.

[0184]

Next, heat treatment is performed. The heat treatment is performed under a reduced pressure or in an inert atmosphere or an oxidation atmosphere. By the heat treatment, the impurity concentration in the CAAC-OS film can be reduced.

[0185]

The heat treatment is preferably performed in a manner such that after heat treatment is performed under a reduced pressure or in an inert atmosphere, the atmosphere is switched to an oxidation atmosphere with the temperature maintained and heat treatment is further performed. When the heat treatment is performed under a

reduced pressure or in an inert atmosphere, the impurity concentration in the CAAC-OS film can be reduced; however, oxygen vacancies are caused at the same time. By the heat treatment in an oxidation atmosphere, the caused oxygen vacancies can be reduced.
[0186]

5 When heat treatment is performed on the CAAC-OS film in addition to the substrate heating during the film formation, the impurity concentration in the film can be reduced.
[0187]

10 Specifically, the concentration of hydrogen in the CAAC-OS film, which is measured by secondary ion mass spectrometry (SIMS), can be set to be lower than or equal to 2×10^{20} atoms/cm³, preferably lower than or equal to 5×10^{19} atoms/cm³, more preferably lower than or equal to 1×10^{19} atoms/cm³, further preferably lower than or equal to 5×10^{18} atoms/cm³.
[0188]

15 The concentration of nitrogen in the CAAC-OS film, which is measured by SIMS, can be set to be lower than 5×10^{19} atoms/cm³, preferably lower than or equal to 5×10^{18} atoms/cm³, more preferably lower than or equal to 1×10^{18} atoms/cm³, further preferably lower than or equal to 5×10^{17} atoms/cm³.
[0189]

20 The concentration of carbon in the CAAC-OS film, which is measured by SIMS, can be set to be lower than 5×10^{19} atoms/cm³, preferably lower than or equal to 5×10^{18} atoms/cm³, more preferably lower than or equal to 1×10^{18} atoms/cm³, further preferably lower than or equal to 5×10^{17} atoms/cm³.
[0190]

25 The amount of each of the following gas molecules (atoms) released from the CAAC-OS film can be less than or equal to 1×10^{19} /cm³, preferably less than or equal to 1×10^{18} /cm³ or less, which is measured by thermal desorption spectroscopy (TDS) analysis: a gas molecule (atom) having a mass-to-charge ratio (m/z) of 2 (e.g., hydrogen molecule), a gas molecule (atom) having a mass-to-charge ratio (m/z) of 18, a gas molecule (atom) having a mass-to-charge ratio (m/z) of 28, and a gas molecule (atom) having a mass-to-charge ratio (m/z) of 44.
30

[0191]

A measurement method of the amount of released oxygen atoms, which is to be described later, is referred to for a measurement method of the release amount using TDS analysis.

5 [0192]

In the above manner, a CAAC-OS film with a high degree of crystallinity can be formed.

[0193]

10 This embodiment can be implemented in appropriate combination with any of the other embodiments.

[0194]

[Embodiment 3]

In this embodiment, a sputtering target of one embodiment of the present invention is described.

15 [0195]

A sputtering target is a sputtering target where impurity concentration is reduced. Specifically, the concentration of silicon in the sputtering target is set to be lower than 1×10^{19} atoms/cm³, preferably lower than 5×10^{18} atoms/cm³, more preferably lower than 1×10^{18} atoms/cm³. The concentration of carbon in the sputtering target is set to be lower than 1×10^{19} atoms/cm³, preferably lower than 5×10^{18} atoms/cm³, more preferably lower than 1×10^{18} atoms/cm³. The concentration of iron in the sputtering target is set to be lower than 1×10^{16} atoms/cm³, preferably lower than 5×10^{15} atoms/cm³, more preferably lower than 1×10^{15} atoms/cm³. The concentration of nickel in the sputtering target is set to be lower than 5×10^{16} atoms/cm³, preferably lower than 1×10^{16} atoms/cm³, more preferably lower than 5×10^{15} atoms/cm³, further preferably lower than 1×10^{15} atoms/cm³. It is preferable to use a highly-purified raw material in order to reduce the impurity concentration in the sputtering target.

[0196]

30 The relative density of the sputtering target is higher than or equal to 90 %, preferably higher than or equal to 95 %, more preferably higher than or equal to 99 %.

[0197]

The sputtering target includes a polycrystalline oxide containing a plurality of crystal grains, whose average grain size is less than or equal to 3 μm , preferably less than or equal to 2.5 μm , more preferably less than or equal to 2 μm .

5 [0198]

Alternatively, the sputtering target includes a polycrystalline oxide containing a plurality of crystal grains, in which the proportion of crystal grains whose grain size is greater than or equal to 0.4 μm and less than or equal to 1 μm is 8 % or more, preferably 15 % or more, more preferably 25 % or more.

10 [0199]

Note that a crystal grain size can be measured by, for example, electron backscatter diffraction (EBSD). The grain size of the crystal grain described here is calculated from a cross-sectional area, assuming that a cross section of one crystal grain is a perfect circle. The cross section of the crystal grain can be measured from a crystal grain map obtained by EBSD. Specifically, when the cross-sectional area of the crystal grain is denoted by S and the radius of the cross section of the crystal grain is denoted by r , the radius r is calculated from the relation in which $S = \pi r^2$ to obtain the grain size which can be represented by $2r$ (twice the radius r).

[0200]

20 Further, the plurality of crystal grains included in the sputtering target include cleavage planes. The cleavage plane is a plane parallel to an a - b plane, for example.

[0201]

Owing to small grain sizes of the plurality of crystal grains, when an ion collides with the sputtering target, a sputtered particle is separated from the cleavage plane. The separated sputtered particle has a flat plate-like shape whose top and bottom surfaces are parallel to the cleavage plane. Further, owing to small grain sizes of the plurality of crystal grains, a crystal is distorted and a sputtered particle is easily separated from the cleavage plane.

[0202]

30 Note that when the plurality of crystal grains included in the sputtering target are hexagonal crystals, flat plate-like sputtered particles each have the shape of a

hexagonal cylinder whose top and bottom surfaces are approximately equilateral hexagons each having interior angles of 120 °.

[0203]

Although sputtered particles are ideally single crystals, part of the sputtered
5 particles may be changed into an amorphous state due to the impact of ion collision.

[0204]

As such a polycrystalline oxide included in the sputtering target, an oxide
containing In, *M* (*M* is Ga, Sn, Hf, Al, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm,
Yb, or Lu), and Zn can be used. The oxide containing In, *M*, and Zn is also referred to
10 as In-*M*-Zn oxide.

[0205]

Moreover, the atomic ratio of In, *M*, and Zn contained in the In-*M*-Zn oxide is
preferably close to the stoichiometric composition ratio. When the atomic ratio of In,
M, and Zn contained in the In-*M*-Zn oxide becomes close to the stoichiometric
15 composition ratio, the crystallinity of the In-*M*-Zn oxide can be increased.

[0206]

In the In-*M*-Zn oxide, a cleavage plane is in many cases a plane parallel to an
a-b plane in which *M* and Zn are mixed.

[0207]

20 A method for manufacturing the above sputtering target is described with
reference to FIGS. 15A and 15B.

[0208]

FIG. 15A shows manufacture of an oxide powder containing a plurality of
metal elements to be the sputtering target. First, the oxide powder is weighed in a step
25 S101.

[0209]

Here, description is given on the case where an oxide powder containing In, *M*,
and Zn (also referred to as an In-*M*-Zn oxide powder) is obtained as the oxide powder
containing a plurality of metal elements. Specifically, an InO_{*X*} oxide powder, an MO_{*Y*}
30 oxide powder, and a ZnO_{*Z*} oxide powder are prepared as a raw material. Note that *X*, *Y*,
and *Z* are each a given positive number; for example, *X*, *Y*, and *Z* are 1.5, 1.5, and 1,
respectively. It is needless to say that the above oxide powders are examples, and oxide

powders can be selected as appropriate in order to obtain a desired composition. Note that M refers to Ga, Sn, Hf, Al, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, or Lu. Although the case where three kinds of oxide powders are used is shown as an example in this embodiment, one embodiment of the present invention is not limited thereto. For example, this embodiment may be applied to the case where four or more kinds of oxide powders are used or the case where one or two kinds of oxide powders are used.

[0210]

Next, the InO_X powder, the MO_Y powder, and the ZnO_Z powder are mixed in a predetermined mole ratio.

10 [0211]

For example, the predetermined mole ratio of the InO_X oxide powder, the MO_Y oxide powder, and the ZnO_Z oxide powder is 2:2:1, 8:4:3, 3:1:1, 1:1:1, 4:2:3, 1:1:2, 3:1:4, 1:3:2, 1:3:4, 1:3:6, 1:3:8, 1:3:10, 1:3:12, 1:6:4, 1:6:6, 1:6:8, 1:6:10, 1:6:12, 1:6:14, 1:6:16, 1:6:20, or 3:1:2. With such a mole ratio, a sputtering target including a polycrystalline oxide with high crystallinity can be obtained easily later.

15

[0212]

Next, in a step S102, an In- M -Zn oxide is obtained by performing first baking on the InO_X oxide powder, the MO_Y oxide powder, and the ZnO_Z oxide powder which are mixed in a predetermined mole ratio.

20 [0213]

Note that the first baking is performed in an inert atmosphere, an oxidation atmosphere, or under a reduced pressure at a temperature higher than or equal to 400 °C and lower than or equal to 1700 °C, preferably higher than or equal to 900 °C and lower than or equal to 1500 °C. The first baking is performed for longer than or equal to 3 minutes and shorter than or equal to 24 hours, preferably longer than or equal to 30 minutes and shorter than or equal to 17 hours, more preferably longer than or equal to 30 minutes and shorter than or equal to 5 hours, for example. When the first baking is performed under the above conditions, secondary reactions other than the main reaction can be suppressed, and the impurity concentration in the In- M -Zn oxide can be reduced. Accordingly, the crystallinity of the In- M -Zn oxide can be increased.

30

[0214]

The first baking may be performed plural times at different temperatures and/or in different atmospheres. For example, the In-*M*-Zn oxide may be first held at a first temperature in a first atmosphere and then at a second temperature in a second atmosphere. Specifically, it is preferable that the first atmosphere be an inert atmosphere or under a reduced pressure and the second atmosphere be an oxidation atmosphere. This is because oxygen vacancies are generated in the In-*M*-Zn oxide when impurities contained in the In-*M*-Zn oxide are reduced in the first atmosphere. Therefore, it is preferable that oxygen vacancies in the obtained In-*M*-Zn oxide be reduced in the second atmosphere. The impurity concentration and oxygen vacancies in the In-*M*-Zn oxide are reduced, whereby the crystallinity of the In-*M*-Zn oxide can be increased.

[0215]

Next, the In-*M*-Zn oxide powder is obtained by grinding the In-*M*-Zn oxide in a step S103.

[0216]

The In-*M*-Zn oxide has a high proportion of crystals with structures of planes parallel to the *a-b* plane. Therefore, the obtained In-*M*-Zn oxide powder includes many flat plate-like crystal grains whose top and bottom surfaces are parallel to the *a-b* plane. Moreover, the crystal of the In-*M*-Zn oxide is in many cases a hexagonal crystal; therefore, in many cases, the above flat plate-like crystal grains each have the shape of a hexagonal cylinder whose top and bottom surfaces are approximately equilateral hexagons each having interior angles of 120°.

[0217]

Next, the grain size of the obtained In-*M*-Zn oxide powder is checked in a step S104. Here, the average grain size of the In-*M*-Zn oxide powder is checked to be less than or equal to 3 μm, preferably less than or equal to 2.5 μm, more preferably less than or equal to 2 μm. Note that the step S104 may be omitted and only the In-*M*-Zn oxide powder whose grain size is less than or equal to 3 μm, preferably less than or equal to 2.5 μm, more preferably less than or equal to 2 μm may be sifted using a grain size filter. The average grain size of the In-*M*-Zn oxide powder can be certainly less than or equal to 3 μm, preferably less than or equal to 2.5 μm, more preferably less than or equal to 2

μm by sifting the In-*M*-Zn oxide powder whose grain size is less than or equal to 3 μm, preferably less than or equal to 2.5 μm, more preferably less than or equal to 2 μm.

[0218]

In the case where the average grain size of the In-*M*-Zn oxide powder exceeds
5 a predetermined size in the step S104, the procedure returns to the step S103 and the In-*M*-Zn oxide powder is ground again.

[0219]

In the above manner, the In-*M*-Zn oxide powder whose average grain size is less than or equal to 3 μm, preferably less than or equal to 2.5 μm, more preferably less
10 than or equal to 2 μm can be obtained. Note that the grain size of a crystal grain included in a sputtering target to be formed later can be reduced by obtaining the In-*M*-Zn oxide powder whose average grain size is less than or equal to 3 μm, preferably less than or equal to 2.5 μm, more preferably less than or equal to 2 μm.

[0220]

15 Next, in FIG. 15B, a sputtering target is formed using the In-*M*-Zn oxide powder obtained in the flow chart shown in FIG. 15A.

[0221]

In a step S111, the In-*M*-Zn oxide powder is made to spread over a mold and molded. Here, molding refers to making powder or the like spread over a mold to
20 obtain a uniform thickness. Specifically, the In-*M*-Zn oxide powder is introduced to the mold, and then vibration is externally applied so that the In-*M*-Zn oxide powder is molded. Alternatively, the In-*M*-Zn oxide powder is introduced to the mold, and then molding is performed using a roller or the like so as to obtain a uniform thickness. Note that in the step S111, slurry in which the In-*M*-Zn oxide powder is mixed with water, a
25 dispersant, and a binder may be molded. In that case, the slurry is poured into the mold and then molded by sucking the mold from the bottom. After that, drying treatment is performed on a molded body after the mold is sucked. The drying treatment is preferably natural drying because the molded body is less likely to be cracked. After that, the molded body is subjected to heat treatment at a temperature higher than or equal
30 to 300 °C and lower than or equal to 700 °C, so that residual moisture or the like which cannot be taken out by natural drying is removed. Note that as the filter, a filter in

which a porous resin film is attached over a woven fabric or a felt may be used.

[0222]

When the In-*M*-Zn oxide powder including many flat plate-like crystal grains whose top and bottom surfaces are parallel to the *a-b* plane is made to spread over the mold and molded, the crystal grains are arranged with the planes which are parallel to the *a-b* plane thereof facing upward. Therefore, the proportion of the surface structures of planes parallel to the *a-b* plane can be increased in such a manner that the obtained In-*M*-Zn oxide powder is made to spread over the mold and molded. Note that the mold may be formed of a metal or an oxide and the upper shape thereof is rectangular or rounded.

[0223]

Next, first pressure treatment is performed on the In-*M*-Zn oxide powder in a step S112. After that, in a step S113, second baking is performed to obtain an In-*M*-Zn oxide. The second baking is performed under conditions similar to those of the first baking. The crystallinity of the In-*M*-Zn oxide can be increased by performing the second baking.

[0224]

Note that the first pressure treatment may be performed in any manner as long as the In-*M*-Zn oxide powder can be pressed. For example, a weight which is formed of the same kind of material as the mold can be used. Alternatively, the In-*M*-Zn oxide powder may be pressed under a high pressure using compressed air. Besides, the first pressure treatment can be performed using a known technique. Note that the first pressure treatment may be performed at the same time as the second baking.

[0225]

Planarization treatment may be performed after the first pressure treatment. As the planarization treatment, chemical mechanical polishing (CMP) treatment or the like can be employed.

[0226]

The plate-like In-*M*-Zn oxide thus obtained becomes a polycrystalline oxide with high crystallinity.

[0227]

Next, the thickness of the obtained plate-like In-*M*-Zn oxide is checked in a

step S114. When the thickness of the plate-like In-*M*-Zn oxide is less than a desired thickness, the procedure returns to the step S111 and the In-*M*-Zn oxide powder is made to spread over the plate-like In-*M*-Zn oxide and molded. When the plate-like In-*M*-Zn oxide has a desired thickness in the step S114, the plate-like In-*M*-Zn oxide is used as a sputtering target. The description of steps following the step S111 when the thickness of the plate-like In-*M*-Zn oxide is less than a desired thickness is given below.

[0228]

After the step S111, in the step S112, second pressure treatment is performed on the plate-like In-*M*-Zn oxide and the In-*M*-Zn oxide powder over the plate-like In-*M*-Zn oxide. Then, in the step S113, third baking is performed, whereby a plate-like In-*M*-Zn oxide whose thickness is increased by the thickness of the In-*M*-Zn oxide powder is obtained. A plate-like In-*M*-Zn oxide with an increased thickness is obtained through crystal growth with the use of the plate-like In-*M*-Zn oxide as a seed crystal; therefore, the plate-like In-*M*-Zn oxide is a polycrystalline oxide with high crystallinity.

[0229]

Note that the third baking is performed under conditions similar to those of the second baking. The second pressure treatment is performed under conditions similar to those of the first pressure treatment. Note that the second pressure treatment may be performed at the same time as the third baking.

[0230]

The thickness of the obtained plate-like In-*M*-Zn oxide is checked again in the step S114.

[0231]

Through the above steps, the thickness of the plate-like In-*M*-Zn oxide can be gradually increased while the crystal alignment is improved.

[0232]

By repeating these steps of increasing the thickness of a plate-like In-*M*-Zn oxide *n* times (*n* is a natural number), the plate-like In-*M*-Zn oxide having a desired thickness (*t*), for example, greater than or equal to 2 mm and less than or equal to 20 mm, preferably greater than or equal to 3 mm and less than or equal to 20 mm can be obtained. The plate-like In-*M*-Zn oxide is used as a sputtering target.

[0233]

After that, planarization treatment may be performed.

[0234]

Note that fourth baking may be performed on the obtained sputtering target. The fourth baking is performed under conditions similar to those of the first baking. A sputtering target including a polycrystalline oxide with much higher crystallinity can be obtained by performing the fourth baking.

[0235]

In the above manner, the sputtering target which includes a polycrystalline oxide containing a plurality of crystal grains having cleavage planes parallel to the *a-b* plane and a small grain size can be formed.

[0236]

Note that the sputtering target formed in such a manner can have high density. When the density of the sputtering target is increased, the density of a film to be formed can also be increased. Specifically, the relative density of the sputtering target can be set to be higher than or equal to 90 %, preferably higher than or equal to 95 %, more preferably higher than or equal to 99 %.

[0237]

This embodiment can be implemented in appropriate combination with any of the other embodiments.

[0238]

[Embodiment 4]

In this embodiment, a transistor of one embodiment of the present invention is described.

[0239]

FIG. 16A is a top view of a transistor of one embodiment of the present invention. FIG. 16B is a cross-sectional view taken along dashed-dotted line A1-A2 in FIG. 16A. FIG. 16C is a cross-sectional view taken along dashed-dotted line A3-A4 in FIG. 16A. For easy understanding, a gate insulating film 112 and the like are not illustrated in FIG. 16A.

[0240]

FIG. 16B is a cross-sectional view of a transistor which includes a base

insulating film 102 over a substrate 100, a gate electrode 104 over the base insulating film 102, the gate insulating film 112 over the gate electrode 104, an oxide semiconductor film 106 which is over the gate insulating film 112 and overlaps with the gate electrode 104, a source electrode 116a and a drain electrode 116b over the oxide semiconductor film 106, and a protective insulating film 118 over the oxide semiconductor film 106, the source electrode 116a, and the drain electrode 116b. Although FIG. 16B illustrates the structure in which the base insulating film 102 is provided, the present invention is not limited thereto. For example, the base insulating film 102 may be omitted.

10 [0241]

Here, the oxide film with high crystallinity described in the above embodiments is applied to the oxide semiconductor film 106.

[0242]

The concentration of hydrogen in the oxide semiconductor film 106 is lower than or equal to 2×10^{20} atoms/cm³, preferably lower than or equal to 5×10^{19} atoms/cm³, more preferably lower than or equal to 1×10^{19} atoms/cm³, further preferably lower than or equal to 5×10^{18} atoms/cm³. This is because hydrogen in the oxide semiconductor film 106 might generate unintentional carriers. The generated carriers cause an increase in the off-state current and a change in the electrical characteristics of the transistor. Thus, by suppressing the concentration of hydrogen in the oxide semiconductor film 106 within the above-described range, an increase in the off-state current and a change in the electrical characteristics of the transistor can be suppressed.

[0243]

25 By suppressing the donor (e.g., hydrogen or oxygen vacancy) concentration in the oxide semiconductor film 106 to be extremely low, the off-state current of the transistor including the oxide semiconductor film 106 can be made extremely small. Specifically, the off-state current of the transistor with a channel length of 3 μm and a channel width of 1 μm can be lower than or equal to 1×10^{-21} A or lower than or equal to 1×10^{-25} A.

[0244]

There is no large limitation on the substrate 100. For example, a glass substrate, a ceramic substrate, a quartz substrate, or a sapphire substrate may be used as the substrate 100. Alternatively, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate made of silicon, silicon carbide, or the like, a compound semiconductor substrate made of silicon germanium or the like, a silicon-on-insulator (SOI) substrate, or the like may be used as the substrate 100. Still alternatively, any of these substrates provided with a semiconductor element may be used as the substrate 100.

[0245]

In the case of using a large glass substrate such as the fifth generation (1000 mm × 1200 mm or 1300 mm × 1500 mm); the sixth generation (1500 mm × 1800 mm); the seventh generation (1870 mm × 2200 mm); the eighth generation (2200 mm × 2500 mm); the ninth generation (2400 mm × 2800 mm); or the tenth generation (2880 mm × 3130 mm) as the substrate 100, in some cases, microfabrication is made difficult owing to shrinkage of the substrate 100, which is caused by heat treatment or the like in the manufacturing process of a semiconductor device. Therefore, in the case where the above-described large glass substrate is used as the substrate 100, a substrate whose shrinkage due to heat treatment is as less as possible is preferably used. For example, as the substrate 100, it is possible to use a large glass substrate in which the amount of shrinkage by heat treatment for one hour at 400 °C, preferably 450 °C, more preferably 500 °C is less than or equal to 10 ppm, preferably less than or equal to 5 ppm, more preferably less than or equal to 3 ppm.

[0246]

Further alternatively, a flexible substrate may be used as the substrate 100. As the method for providing a transistor over a flexible substrate, there is also a method in which a transistor is formed over a non-flexible substrate, and then, the transistor is separated from the non-flexible substrate and transferred to a flexible substrate functioning as the substrate 100. In that case, a separation layer may be provided between the non-flexible substrate and the transistor.

[0247]

The base insulating film 102 may be formed using a single layer or a stacked

layer of an insulating film containing one or more kinds of an aluminum oxide, a magnesium oxide, a silicon oxide, a silicon oxynitride, a gallium oxide, a germanium oxide, an yttrium oxide, a zirconium oxide, a lanthanum oxide, a neodymium oxide, a hafnium oxide, and a tantalum oxide.

5 [0248]

The gate electrode 104 may be formed using a single layer or a stacked layer of a simple substance, a nitride, an oxide, or an alloy containing one or more kinds of Al, Ti, Cr, Co, Ni, Cu, Y, Zr, Mo, Ag, Ta, and W.

[0249]

10 The source electrode 116a and the drain electrode 116b each may be formed using a single layer or a stacked layer of a simple substance, a nitride, an oxide, or an alloy containing one or more kinds of Al, Ti, Cr, Co, Ni, Cu, Y, Zr, Mo, Ag, Ta, and W. Note that the compositions of the source electrode 116a and the drain electrode 116b are either the same as or different from each other.

15 [0250]

The gate insulating film 112 may be formed using a single layer or a stacked layer of an insulating film containing one or more kinds of an aluminum oxide, a magnesium oxide, a silicon oxide, a silicon oxynitride, a gallium oxide, a germanium oxide, an yttrium oxide, a zirconium oxide, a lanthanum oxide, a neodymium oxide, a hafnium oxide, and a tantalum oxide.

[0251]

The protective insulating film 118 may be formed using a single layer or a stacked layer of an insulating film containing one or more kinds of an aluminum oxide, a magnesium oxide, a silicon oxide, a silicon oxynitride, a gallium oxide, a germanium oxide, an yttrium oxide, a zirconium oxide, a lanthanum oxide, a neodymium oxide, a hafnium oxide, and a tantalum oxide.

[0252]

The protective insulating film 118 may be, for example, a stacked film including a silicon oxide film as a first layer and a silicon nitride film as a second layer.

30 In that case, the silicon oxide film may be a silicon oxynitride film. It is preferable to use a silicon oxide film whose defect density is small as the silicon oxide film. Specifically, a silicon oxide film whose spin density attributed to a signal with a g factor

of 2.001 in electron spin resonance (ESR) is less than or equal to 3×10^{17} spins/cm³, preferably less than or equal to 5×10^{16} spins/cm³ is used. As the silicon nitride film, a silicon nitride film from which hydrogen and ammonia are discharged as less as possible is used. The amount of discharge of hydrogen or ammonia may be measured
5 by thermal desorption spectroscopy (TDS). Further, a silicon nitride film which does not penetrate or hardly penetrate oxygen is used as the silicon nitride film.

[0253]

The protective insulating film 118 may be, for example, a stacked film including a first silicon oxide film as a first layer, a second silicon oxide film as a
10 second layer, and a silicon nitride film as a third layer. In that case, the first and/or second silicon oxide film may be a silicon oxynitride film. It is preferable to use a silicon oxide film whose defect density is small as the first silicon oxide film. Specifically, a silicon oxide film whose spin density attributed to a signal with a g factor of 2.001 in ESR is less than or equal to 3×10^{17} spins/cm³, preferably less than or equal
15 to 5×10^{16} spins/cm³ is used. As the second silicon oxide film, a silicon oxide film having excess oxygen is used. As the silicon nitride film, a silicon nitride film from which hydrogen and ammonia are discharged as less as possible is used. Further, a silicon nitride film which does not penetrate or hardly penetrate oxygen is used as the silicon nitride film.

20 [0254]

The silicon oxide film having excess oxygen means a silicon oxide film from which oxygen can be released by heat treatment or the like. When the above definition of the silicon oxide film is applied broadly to an insulating film, an insulating film having excess oxygen means an insulating film from which oxygen is released by heat
25 treatment.

[0255]

Here, a film from which oxygen is released by heat treatment may release oxygen, the amount of which is higher than or equal to 1×10^{18} atoms/cm³, higher than or equal to 1×10^{19} atoms/cm³, or higher than or equal to 1×10^{20} atoms/cm³ in TDS
30 analysis (converted into the number of oxygen atoms).

[0256]

Here, the method of measuring the amount of released oxygen using TDS analysis is described below.

[0257]

The total amount of released gas from a measurement sample in TDS analysis is proportional to the integral value of the ion intensity of the released gas. Then, comparison with a reference sample is made, whereby the total amount of released gas can be calculated.

[0258]

For example, the number of released oxygen molecules (N_{O_2}) from a measurement sample can be calculated according to Formula 1 using the TDS results of a silicon wafer containing hydrogen at a predetermined density, which is a reference sample, and the TDS results of the measurement sample. Here, all gases having a mass number of 32 which are obtained in the TDS analysis are assumed to originate from an oxygen molecule. Note that CH_3OH , which is a gas having the mass number of 32, is not taken into consideration because it is unlikely to be present. Further, an oxygen molecule including an oxygen atom having a mass number of 17 or 18 which is an isotope of an oxygen atom is also not taken into consideration because the proportion of such a molecule in the natural world is minimal.

[0259]

[FORMULA 1]

$$N_{O_2} = \frac{N_{H_2}}{S_{H_2}} \times S_{O_2} \times \alpha$$

[0260]

Here, N_{H_2} is the value obtained by conversion of the number of hydrogen molecules desorbed from the reference sample into densities. In addition, S_{H_2} is the integral value of ion intensity in the TDS analysis of the reference sample. Here, the reference value of the reference sample is N_{H_2}/S_{H_2} . Further, S_{O_2} is the integral value of ion intensity in the TDS analysis of the measurement sample, and α is a coefficient affecting the ion intensity in the TDS analysis. Refer to Japanese Published Patent Application No. H6-275697 for details of Formula 1. The amount of released oxygen was measured with a thermal desorption spectroscopy apparatus produced by ESCO Ltd.,

EMD-WA1000S/W using a silicon wafer containing hydrogen atoms at 1×10^{16} atoms/cm² as the reference sample.

[0261]

Further, in the TDS analysis, part of oxygen is detected as an oxygen atom.

5 The ratio between oxygen molecules and oxygen atoms can be calculated from the ionization rate of the oxygen molecules. Since the above α includes the ionization rate of the oxygen molecules, the number of the released oxygen atoms can also be estimated through the evaluation of the number of the released oxygen molecules.

[0262]

10 Here, N_{O_2} is the number of the released oxygen molecules. The amount of released oxygen in terms of oxygen atoms is twice the number of the released oxygen molecules.

[0263]

Further or alternatively, the film from which oxygen is released by heat
15 treatment may contain a peroxide radical. Specifically, the spin density attributed to the peroxide radical is greater than or equal to 5×10^{17} spins/cm³. Note that the film containing a peroxide radical may have an asymmetric signal with a g factor of approximately 2.01 in ESR.

[0264]

20 The insulating film containing excess oxygen may be oxygen-excess silicon oxide (SiO_X ($X > 2$)). In the oxygen-excess silicon oxide (SiO_X ($X > 2$)), the number of oxygen atoms per unit volume is more than twice the number of silicon atoms per unit volume. The number of silicon atoms and the number of oxygen atoms per unit volume are measured by Rutherford backscattering spectrometry (RBS).

25 [0265]

At least one of the gate insulating film 112 and the protective insulating film 118 is preferably the insulating film containing excess oxygen.

[0266]

In the case where at least one of the gate insulating film 112 and the protective
30 insulating film 118 is the insulating film containing excess oxygen, oxygen vacancies in the oxide semiconductor film 106 can be reduced.

[0267]

A transistor obtained by providing a back-gate electrode 114 for the transistor illustrated in FIGS. 16A to 16C is a transistor illustrated in FIGS. 17A to 17C.

[0268]

5 FIG. 17A is a top view of a transistor of one embodiment of the present invention. FIG. 17B is a cross-sectional view taken along dashed-dotted line A1-A2 in FIG. 17A. FIG. 17C is a cross-sectional view taken along dashed-dotted line A3-A4 in FIG. 17A. For easy understanding, the gate insulating film 112 and the like are not illustrated in FIG. 17A.

10 [0269]

The threshold voltage of the transistor illustrated in FIGS. 17A to 17C can be controlled easily because the back-gate electrode 114 is provided. Further, by connecting the gate electrode 104 to the back-gate electrode 114, the on-state current of the transistor can be increased. Alternatively, by setting the back-gate electrode 114 to
15 a negative potential (potential lower than a source potential of the transistor) or the source potential, the off-state current of the transistor can be reduced.

[0270]

Next, a transistor whose structure is different from those of FIGS. 16A to 16C and FIGS. 17A to 17C is described with reference to FIGS. 18A to 18C.

20 [0271]

FIG. 18A is a top view of a transistor of one embodiment of the present invention. FIG. 18B is a cross-sectional view taken along dashed-dotted line B1-B2 in FIG. 18A. FIG. 18C is a cross-sectional view taken along dashed-dotted line B3-B4 in FIG. 18A. For easy understanding, a gate insulating film 212 and the like are not illustrated in FIG.
25 18A.

[0272]

FIG. 18B is a cross-sectional view of a transistor which includes a base insulating film 202 over a substrate 200, a gate electrode 204 over the base insulating film 202, the gate insulating film 212 over the gate electrode 204, a source electrode
30 216a and a drain electrode 216b over the gate insulating film 212, an oxide semiconductor film 206 which is over the gate insulating film 212, the source electrode 216a, and the drain electrode 216b and overlaps with the gate electrode 204, and a

protective insulating film 218 over the oxide semiconductor film 206, the source electrode 216a, and the drain electrode 216b. Although FIG. 18B illustrates the structure in which the base insulating film 202 is provided, the present invention is not limited thereto. For example, the base insulating film 202 may be omitted.

5 [0273]

For the oxide semiconductor film 206, refer to the description of the oxide semiconductor film 106.

[0274]

For the substrate 200, refer to the description of the substrate 100.

10 [0275]

For the base insulating film 202, refer to the description of the base insulating film 102.

[0276]

For the gate electrode 204, refer to the description of the gate electrode 104.

15 [0277]

For the gate insulating film 212, an insulating film similar to the gate insulating film 112 may be used.

[0278]

For the source electrode 216a and the drain electrode 216b, refer to the description of the source electrode 116a and the drain electrode 116b.

20 [0279]

For the protective insulating film 218, an insulating film similar to the protective insulating film 118 may be used.

[0280]

25 Although not illustrated in the drawing, a back-gate electrode may be provided over the protective insulating film 218 of the transistor illustrated in FIGS. 18A to 18C. For the back-gate electrode, refer to the description of the back-gate electrode 114.

[0281]

30 Next, a transistor whose structure is different from those of FIGS. 16A to 16C, FIGS. 17A to 17C, and FIGS. 18A to 18C is described with reference to FIGS. 19A to 19C.

[0282]

FIG. 19A is a top view of a transistor of one embodiment of the present invention. FIG. 19B is a cross-sectional view taken along dashed-dotted line C1-C2 in FIG. 19A. FIG. 19C is a cross-sectional view taken along dashed-dotted line C3-C4 in FIG. 19A. For easy understanding, a gate insulating film 312 and the like are not illustrated in FIG. 19A.

[0283]

FIG. 19B is a cross-sectional view of a transistor which includes a base insulating film 302 over a substrate 300, an oxide semiconductor film 306 over the base insulating film 302, a source electrode 316a and a drain electrode 316b over the oxide semiconductor film 306, the gate insulating film 312 provided over the oxide semiconductor film 306, the source electrode 316a, and the drain electrode 316b, and a gate electrode 304 which is over the gate insulating film 312 and overlaps with the oxide semiconductor film 306. Although FIG. 19B illustrates the structure in which the base insulating film 302 is provided, the present invention is not limited thereto. For example, the base insulating film 302 may be omitted.

[0284]

For the oxide semiconductor film 306, refer to the description of the oxide semiconductor film 106.

[0285]

For the substrate 300, refer to the description of the substrate 100.

[0286]

For the base insulating film 302, an insulating film similar to the protective insulating film 118 may be used. In the case of employing a stacked-layer structure in which the base insulating film 302 is an example of the protective insulating film 118, the order of stacking layers is reversed.

[0287]

The base insulating film 302 is preferably flat. Specifically, the base insulating film 302 can be made to have an average surface roughness (Ra) of 1 nm or less, 0.3 nm or less, or 0.1 nm or less.

[0288]

Note that Ra is obtained by expanding, into three dimensions, arithmetic mean surface roughness that is defined by JIS B 0601:2001 (ISO4287:1997) so as to be able to

apply to a curved surface, and can be expressed as the "average value of the absolute values of deviations from a reference surface to a designated surface" and is defined by Formula 2.

[0289]

5 [FORMULA 2]

$$Ra = \frac{1}{S_0} \int_{y_1}^{y_2} \int_{x_1}^{x_2} |f(x, y) - Z_0| dx dy$$

[0290]

Here, the designated surface is a surface that is a target of roughness measurement, and is a quadrilateral region specified by four points represented by the coordinates $(x_1, y_1, f(x_1, y_1))$, $(x_1, y_2, f(x_1, y_2))$, $(x_2, y_1, f(x_2, y_1))$, and $(x_2, y_2, f(x_2, y_2))$. In addition, S_0 represents the area of a rectangle which is obtained by projecting the designated surface on the xy plane, and Z_0 represents the height of the reference surface (the average height of the designated surface). Further, Ra can be measured with an atomic force microscope (AFM).

[0291]

The base insulating film 302 is preferably the insulating film containing excess oxygen.

[0292]

20 For the source electrode 316a and the drain electrode 316b, refer to the description of the source electrode 116a and the drain electrode 116b.

[0293]

For the gate insulating film 312, an insulating film similar to the gate insulating film 112 may be used.

25 [0294]

For the gate electrode 304, refer to the description of the gate electrode 104.

[0295]

Although not illustrated in the drawing, a back-gate electrode may be provided under the base insulating film 302 of the transistor illustrated in FIGS. 19A to 19C.

30 For the back-gate electrode, refer to the description of the back-gate electrode 114.

[0296]

Next, a transistor whose structure is different from those of FIGS. 16A to 16C,

FIGS. 17A to 17C, FIGS. 18A to 18C, and FIGS. 19A to 19C is described with reference to FIGS. 20A to 20C.

[0297]

FIG. 20A is a top view of a transistor of one embodiment of the present invention.

5 FIG. 20B is a cross-sectional view taken along dashed-dotted line D1-D2 in FIG. 20A. FIG. 20C is a cross-sectional view taken along dashed-dotted line D3-D4 in FIG. 20A. For easy understanding, a gate insulating film 412 and the like are not illustrated in FIG. 20A.

[0298]

10 FIG. 20B is a cross-sectional view of a transistor which includes a base insulating film 402 over a substrate 400, a source electrode 416a and a drain electrode 416b over the base insulating film 402, an oxide semiconductor film 406 over the base insulating film 402, the source electrode 416a, and the drain electrode 416b, the gate insulating film 412 over the oxide semiconductor film 406, and a gate electrode 404
15 which is over the gate insulating film 412 and overlaps with the oxide semiconductor film 406. Although FIG. 20B illustrates the structure in which the base insulating film 402 is provided, the present invention is not limited thereto. For example, the base insulating film 402 may be omitted.

[0299]

20 For the oxide semiconductor film 406, refer to the description of the oxide semiconductor film 106.

[0300]

For the substrate 400, refer to the description of the substrate 100.

[0301]

25 For the base insulating film 402, an insulating film similar to the base insulating film 302 may be used.

[0302]

For the source electrode 416a and the drain electrode 416b, refer to the description of the source electrode 116a and the drain electrode 116b.

30 [0303]

For the gate insulating film 412, an insulating film similar to the gate insulating film 112 may be used.

[0304]

For the gate electrode 404, refer to the description of the gate electrode 104.

[0305]

Although not illustrated in the drawing, a back-gate electrode may be provided
5 under the base insulating film 402 of the transistor illustrated in FIGS. 20A to 20C.
For the back-gate electrode, refer to the description of the back-gate electrode 114.

[0306]

Next, a transistor whose structure is different from those of FIGS. 16A to 16C,
FIGS. 17A to 17C, FIGS. 18A to 18C, FIGS. 19A to 19C, and FIGS. 20A to 20C is
10 described with reference to FIGS. 21A to 21C.

[0307]

FIG. 21A is a top view of a transistor of one embodiment of the present invention.
FIG. 21B is a cross-sectional view taken along dashed-dotted line E1-E2 in FIG. 21A.
FIG. 21C is a cross-sectional view taken along dashed-dotted line E3-E4 in FIG. 21A.
15 For easy understanding, a gate insulating film 512 and the like are not illustrated in FIG.
21A.

[0308]

FIG. 21B is a cross-sectional view of a transistor which includes a base
insulating film 502 over a substrate 500, an oxide semiconductor film 506 over the base
20 insulating film 502, the gate insulating film 512 over the oxide semiconductor film 506,
a gate electrode 504 which is over the gate insulating film 512 and overlaps with the
oxide semiconductor film 506, and an interlayer insulating film 518 over the oxide
semiconductor film 506 and the gate electrode 504. Although FIG. 21B illustrates the
structure in which the base insulating film 502 is provided, the present invention is not
25 limited thereto. For example, the base insulating film 502 may be omitted.

[0309]

In the cross-sectional view of FIG. 21B, the interlayer insulating film 518 has
openings reaching the oxide semiconductor film 506, and wirings 524a and 524b over
the interlayer insulating film 518 are in contact with the oxide semiconductor film 506
30 through the openings.

[0310]

Although the gate insulating film 512 is provided only in a region which

overlaps with the gate electrode 504 in FIG. 21B, the present invention is not limited thereto. For example, the gate insulating film 512 may be provided to cover the oxide semiconductor film 506. Further, a sidewall insulating film may be provided in contact with the sidewall of the gate electrode 504.

5 [0311]

Further, in the case where the sidewall insulating film is provided in contact with the sidewall of the gate electrode 504, it is preferable that the resistance of a region of the oxide semiconductor film 506, which overlaps with the sidewall insulating film, be lower than that of a region of the oxide semiconductor film 506, which overlaps with the gate electrode 504. For example, a region of the oxide semiconductor film 506, which does not overlap with the gate electrode 504, may contain an impurity which reduces the resistance of the oxide semiconductor film 506, or may be a region whose resistance is reduced by a defect. The region of the oxide semiconductor film 506, which overlaps with the sidewall insulating film, functions as a lightly doped drain (LDD) region because the resistance thereof is lower than that of the region which overlaps with the gate electrode 504. With the LDD region of the transistor, drain induced barrier lowering (DIBL) and hot-carrier deterioration can be suppressed. The region of the oxide semiconductor film 506, which overlaps with the sidewall insulating film, may be used as an offset region. Also with the offset region of the transistor, DIBL and hot-carrier deterioration can be suppressed

20 [0312]

For the oxide semiconductor film 506, refer to the description of the oxide semiconductor film 106.

[0313]

25 For the substrate 500, refer to the description of the substrate 100.

[0314]

For the base insulating film 502, an insulating film which is similar to the base insulating film 302 may be used.

[0315]

30 For the gate insulating film 512, an insulating film similar to the gate insulating film 112 may be used.

[0316]

For the gate electrode 504, refer to the description of the gate electrode 104.

[0317]

The interlayer insulating film 518 may be formed using a single layer or a stacked layer of an insulating film containing one or more kinds of an aluminum oxide, a magnesium oxide, a silicon oxide, a silicon oxynitride, a gallium oxide, a germanium oxide, an yttrium oxide, a zirconium oxide, a lanthanum oxide, a neodymium oxide, a hafnium oxide, and a tantalum oxide.

[0318]

The wiring 524a and the wiring 524b each may be formed using a single layer or a stacked layer of a simple substance, a nitride, an oxide, or an alloy containing one or more kinds of Al, Ti, Cr, Co, Ni, Cu, Y, Zr, Mo, Ag, Ta, and W. Note that the compositions of the wiring 524a and the wiring 524b are either the same as or different from each other.

[0319]

Although not illustrated in the drawing, a back-gate electrode may be provided under the base insulating film 502 of the transistor illustrated in FIGS. 21A to 21C. For the back-gate electrode, refer to the description of the back-gate electrode 114.

[0320]

In the transistor illustrated in FIGS. 21A to 21C, a region where the gate electrode 504 overlaps with another wiring or electrode is small, so that parasitic capacitance hardly occurs and the switching properties of the transistor can be increased. Further, the channel length of the transistor can be determined by the width of the gate electrode 504, which enables a miniaturized transistor having a short channel length to be fabricated easily.

[0321]

In each of the transistors illustrated in FIGS. 16A to 16C, FIGS. 17A to 17C, FIGS. 18A to 18C, FIGS. 19A to 19C, FIGS. 20A to 20C, and FIGS. 21A to 21C, the oxide film with high crystallinity described in the above embodiments is applied to the oxide semiconductor film. Therefore, stable electrical characteristics are provided.

[0322]

This embodiment can be implemented in appropriate combination with any of the other embodiments.

[0323]

[Embodiment 5]

In this embodiment, a logic circuit that is a semiconductor device of one embodiment of the present invention is described.

5 [0324]

FIG. 22A is a circuit diagram showing one example of a NOT circuit (inverter) using a p-channel transistor and an n-channel transistor.

[0325]

10 A transistor including, for example, silicon may be applied to a transistor Tr1a that is a p-channel transistor. However, the transistor Tr1a is not limited to the transistor including silicon. The threshold voltage of the transistor Tr1a is referred to as V_{th1a} .

[0326]

15 As a transistor Tr2a that is an n-channel transistor, the transistor described in the above embodiments may be used. The threshold voltage of the transistor Tr2a is referred to as V_{th2a} .

[0327]

20 Here, a gate of the transistor Tr1a is connected to an input terminal V_{in} and a gate of the transistor Tr2a. A source of the transistor Tr1a is electrically connected to a power source potential (VDD). A drain of the transistor Tr1a is connected to a drain of the transistor Tr2a and an output terminal V_{out} . A source of the transistor Tr2a is connected to a ground potential (GND). Further, a back gate of the transistor Tr2a is connected to a back-gate line BGL. Although the structure in which the transistor Tr2a has the back gate is described in this embodiment, the present invention is not limited thereto. For example, the transistor Tr2a may not have a back gate, and the transistor Tr1a may have a back gate.

[0328]

30 For example, the threshold voltage V_{th1a} of the transistor Tr1a is set to be greater than VDD with the potential inverted and less than 0 V ($-VDD < V_{th1a} < 0$ V), and the threshold voltage V_{th2a} of the transistor Tr2a is set to be greater than 0 V and less than VDD (0 V $< V_{th2a} < VDD$). A back gate may be used to control the threshold voltage of the transistor.

[0329]

Here, when the potential of the input terminal V_{in} is VDD, the gate voltage of the transistor Tr1a becomes 0 V, so that the transistor Tr1a is turned off, whereas the gate voltage of the transistor Tr2a becomes VDD, so that the transistor Tr2a is turned on.
5 Consequently, the output terminal V_{out} is electrically connected to GND, so that GND is supplied to the output terminal V_{out} .

[0330]

On the other hand, when the potential of the input terminal V_{in} is GND, the gate voltage of the transistor Tr1a becomes VDD, so that the transistor Tr1a is turned on,
10 whereas the gate voltage of the transistor Tr2a becomes 0 V, so that the transistor Tr2a is turned off. Consequently, the output terminal V_{out} is electrically connected to VDD, so that VDD is supplied to the output terminal V_{out} .

[0331]

As described above, in the circuit diagram shown in FIG. 22A, GND and VDD
15 are output from the output terminal V_{out} when the potential of the input terminal V_{in} is VDD and when the potential of the input terminal V_{in} is GND, respectively.

[0332]

FIG. 22B is one example of the cross-sectional view of a semiconductor device corresponding to FIG. 22A.

20 [0333]

FIG. 22B is a cross-sectional view of a semiconductor device including the transistor Tr1a including a gate electrode 654, an insulating film 902 over the transistor Tr1a, and the transistor Tr2a which is over the transistor Tr1a and includes the gate electrode 654 and the insulating film 902.

25 [0334]

The insulating film 902 may be formed using a single layer or a stacked layer of an insulating film containing one or more kinds of an aluminum oxide, a magnesium oxide, a silicon oxide, a silicon oxynitride, a gallium oxide, a germanium oxide, an yttrium oxide, a zirconium oxide, a lanthanum oxide, a neodymium oxide, a hafnium
30 oxide, and a tantalum oxide.

[0335]

In FIG. 22B, a transistor which is similar to the transistor illustrated in FIGS.

20A to 20C is applied to the transistor Tr2a. Therefore, for components of the transistor Tr2a other than the components described below, refer to the description of FIGS. 20A to 20C.

[0336]

5 The transistor Tr1a includes a semiconductor substrate 650, a channel region 656, a source region 657a, and a drain region 657b which are formed in the semiconductor substrate 650, an element separation layer 664 which fills a groove formed in the semiconductor substrate 650, a gate insulating film 662 provided over the semiconductor substrate 650, and the gate electrode 654 provided over the channel
10 region 656 with the gate insulating film 662 provided therebetween.

[0337]

 As the semiconductor substrate 650, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate made of silicon, silicon carbide, or the like, or a compound semiconductor substrate made of silicon germanium or the like may be used.

15 [0338]

 Although the structure in which the transistor Tr1a is provided in the semiconductor substrate is described in this embodiment, the present invention is not limited thereto. For example, a substrate having an insulating surface may be used instead of the semiconductor substrate, and a semiconductor film may be provided on
20 the insulating surface. As the substrate having an insulating surface, a glass substrate, a ceramic substrate, a quartz substrate, or a sapphire substrate may be used, for example.

[0339]

 The source region 657a and the drain region 657b are each a region of the semiconductor substrate 650 containing an impurity imparting p-type conductivity.

25 [0340]

 The element separation layer 664 may be formed using a single layer or a stacked layer of an insulating film containing one or more kinds of an aluminum oxide, a magnesium oxide, a silicon oxide, a silicon oxynitride, a silicon nitride oxide, a silicon nitride, a gallium oxide, a germanium oxide, an yttrium oxide, a zirconium oxide, a
30 lanthanum oxide, a neodymium oxide, a hafnium oxide, and a tantalum oxide.

[0341]

 The gate insulating film 662 may be formed using a single layer or a stacked

layer of an insulating film containing one or more kinds of an aluminum oxide, a magnesium oxide, a silicon oxide, a silicon oxynitride, a silicon nitride oxide, a silicon nitride, a gallium oxide, a germanium oxide, an yttrium oxide, a zirconium oxide, a lanthanum oxide, a neodymium oxide, a hafnium oxide, and a tantalum oxide.

5 [0342]

The gate electrode 654 may be formed using a single layer or a stacked layer of a simple substance, a nitride, an oxide, or an alloy containing one or more kinds of Al, Ti, Cr, Co, Ni, Cu, Y, Zr, Mo, Ag, Ta, and W.

[0343]

10 The gate electrode 654 functions as not only the gate electrode of the transistor Tr1a but also the gate electrode of the transistor Tr2a. Thus, the insulating film 902 functions as a gate insulating film of the transistor Tr2a.

[0344]

For a source electrode 916a and a drain electrode 916b of the transistor Tr2a, refer to the description of the source electrode 416a and the drain electrode 416b.

15

[0345]

For an oxide semiconductor film 906 of the transistor Tr2a, refer to the description of the oxide semiconductor film 406.

[0346]

20 For a gate insulating film 912 of the transistor Tr2a, refer to the description of the gate insulating film 412.

[0347]

For a gate electrode 914 of the transistor Tr2a, refer to the description of the gate electrode 404. The gate electrode 914 functions as the back-gate electrode of the transistor Tr2a.

25

[0348]

The semiconductor device illustrated in FIG. 22B includes an insulating film 690 whose top surface is level with the top surface of the gate electrode 654. The insulating film 690 is not necessarily provided.

30 [0349]

The insulating film 690 may be formed using a single layer or a stacked layer of an insulating film containing one or more kinds of an aluminum oxide, a magnesium

oxide, a silicon oxide, a silicon oxynitride, a silicon nitride oxide, a silicon nitride, a gallium oxide, a germanium oxide, an yttrium oxide, a zirconium oxide, a lanthanum oxide, a neodymium oxide, a hafnium oxide, and a tantalum oxide.

[0350]

5 An opening reaching the drain region 657b of the transistor Tr1a is provided in the insulating film 690, the insulating film 902, and the gate insulating film 662. The drain electrode 916b of the transistor Tr2a is in contact with the drain region 657b of the transistor Tr1a through the opening.

[0351]

10 In the case where the transistor described in the above embodiments is applied to the transistor Tr2a, the off-state current of the transistor Tr2a is extremely small, and thus the shoot-through current in the case where the transistor Tr2a is off is also extremely small. Accordingly, a low power consumption inverter can be achieved.

[0352]

15 A NAND circuit shown in FIG. 23A may be configured by combining the inverters shown in FIG. 22A. A circuit diagram shown in FIG. 23A includes p-channel transistors Tr1b and Tr4b and n-channel transistors Tr2b and Tr3b. Transistors each using, for example, silicon may be applied to the transistors Tr1b and Tr4b. Further, the transistors including the oxide semiconductor film, which are described in the above
20 embodiments, may be applied to the transistors Tr2b and Tr3b.

[0353]

 A NOR circuit shown in FIG. 23B may be configured by combining the inverters shown in FIG. 22A. A circuit diagram shown in FIG. 23B includes p-channel transistors Tr1c and Tr2c and n-channel transistors Tr3c and Tr4c. Transistors each
25 using, for example, silicon may be applied to the transistors Tr1c and Tr2c. Further, the transistors including the oxide semiconductor film, which are described in the above embodiments, may be applied to the transistors Tr3c and Tr4c.

[0354]

 Although examples of the logic circuit configured by an inverter using a
30 p-channel transistor and an n-channel transistor are described above, a logic circuit may be configured by an inverter using only n-channel transistors. An example thereof is shown in FIG. 24A.

[0355]

A circuit diagram shown in FIG. 24A includes a depression transistor Tr1d and an enhancement transistor Tr2d.

[0356]

5 A transistor including, for example, an oxide semiconductor film may be applied to the depression transistor Tr1d. However, the transistor Tr1d is not limited to the transistor including an oxide semiconductor film. For example, a transistor including silicon may be used as well. The threshold voltage of the transistor Tr1d is referred to as V_{th1d} . Instead of the depression transistor, a resistor with sufficiently
10 low resistance may be provided.

[0357]

As the enhancement transistor Tr2d, the transistor including the oxide semiconductor film, which is described in the above embodiments, may be used. The threshold voltage of the transistor Tr2d is referred to as V_{th2d} .

15 [0358]

The transistor including the oxide semiconductor film, which is described in the above embodiments, may be used as the transistor Tr1d. In that case, any transistor other than the transistor including the oxide semiconductor film, which is described in the above embodiments, may be used as the transistor Tr2d.

20 [0359]

Here, a gate of the transistor Tr1d is connected to an input terminal V_{in} and a gate of the transistor Tr2d. A drain of the transistor Tr1d is electrically connected to VDD. A source of the transistor Tr1d is connected to a drain of the transistor Tr2d and an output terminal V_{out} . A source of the transistor Tr2d is connected to GND.
25 Further, a back gate of the transistor Tr2d is connected to a back-gate line BGL. Although the structure in which the transistor Tr2d has the back gate is described in this embodiment, the present invention is not limited thereto. For example, the transistor Tr2d may not have a back gate, and the transistor Tr1d may have a back gate.

[0360]

30 For example, the threshold voltage V_{th1d} of the transistor Tr1d is set to be lower than 0 V ($V_{th1d} < 0$ V), so that the transistor Tr1d is on regardless of its gate voltage; that is, the transistor Tr1d functions as a resistor with sufficiently low resistance.

Further, the threshold voltage V_{th2d} of the transistor Tr2d is set to be greater than 0 V and less than VDD ($0\text{ V} < V_{th2d} < \text{VDD}$). A back gate may be used to control the threshold voltage of the transistor. Further, a resistor with sufficiently low resistance may be provided instead of the transistor Tr1d.

5 [0361]

Here, when the potential of the input terminal V_{in} is VDD, the gate voltage of the transistor Tr2d becomes VDD, so that the transistor Tr2d is turned on. Consequently, the output terminal V_{out} is electrically connected to GND, so that GND is supplied to the output terminal V_{out} .

10 [0362]

On the other hand, when the potential of the input terminal V_{in} is GND, the gate voltage of the transistor Tr2d becomes 0 V, so that the transistor Tr2d is turned off. Consequently, the output terminal V_{out} is electrically connected to VDD, so that VDD is supplied to the output terminal V_{out} . Strictly speaking, a potential whose voltage is
15 dropped from VDD by the resistance of the transistor Tr1d is output from the output terminal V_{out} ; however, such a voltage drop can be ignored because the resistance of the transistor Tr1d is sufficiently low.

[0363]

As described above, in the circuit diagram shown in FIG. 24A, GND and VDD
20 are output from the output terminal V_{out} when the potential of the input terminal V_{in} is VDD and when the potential of the input terminal V_{in} is GND, respectively.

[0364]

The transistor Tr1d and the transistor Tr2d may be formed in the same plane, which enables the inverter to be fabricated easily. In that case, at least one of the
25 transistor Tr1d and the transistor Tr2d is preferably provided with a back gate. In the case where a depression transistor is formed, the threshold voltage V_{th2d} of the transistor Tr2d may be controlled to be in the above-described range by the back gate of the transistor Tr2d, and in the case where an enhancement transistor is formed, the threshold voltage V_{th1d} of the transistor Tr1d may be controlled to be in the
30 above-described range by the back gate of the transistor Tr1d. The threshold voltages of the transistor Tr1d and the transistor Tr2d may be controlled by their respective back gates.

[0365]

Alternatively, the transistor Tr1d and the transistor Tr2d may be stacked, which leads to a reduction in the area of the inverter.

[0366]

5 FIG. 24B is one example of the cross-sectional view of a semiconductor device fabricated by stacking the transistor Tr1d and the transistor Tr2d.

[0367]

10 In FIG. 24B, refer to the description of the transistor illustrated in FIGS. 20A to 20C for the transistor Tr1d, and a transistor which is similar to the transistor illustrated in FIGS. 20A to 20C is applied to the transistor Tr2d. Therefore, for components of the transistor Tr2d other than the components described below, refer to the description of FIGS. 20A to 20C.

[0368]

15 The transistor Tr1d includes the base insulating film 402 over the substrate 400, the source electrode 416a and the drain electrode 416b over the base insulating film 402, the oxide semiconductor film 406 over the base insulating film 402, the source electrode 416a, and the drain electrode 416b, the gate insulating film 412 over the oxide semiconductor film 406, and the gate electrode 404 which is over the gate insulating film 412 and overlaps with the oxide semiconductor film 406.

20 [0369]

The gate electrode 404 functions as not only the gate electrode of the transistor Tr1d but also the gate electrode of the transistor Tr2d. Thus, an insulating film 802 functions as a gate insulating film of the transistor Tr2d.

[0370]

25 For a source electrode 816a and a drain electrode 816b of the transistor Tr2d, refer to the description of the source electrode 416a and the drain electrode 416b.

[0371]

For an oxide semiconductor film 806 of the transistor Tr2d, refer to the description of the oxide semiconductor film 406.

30 [0372]

For a gate insulating film 812 of the transistor Tr2d, refer to the description of the gate insulating film 412.

[0373]

For a gate electrode 814 of the transistor Tr2d, refer to the description of the gate electrode 404. The gate electrode 814 functions as the back-gate electrode of the transistor Tr2d.

5 [0374]

The semiconductor device illustrated in FIG. 24B includes an insulating film 420 whose top surface is level with the top surface of the gate electrode 404. The insulating film 420 is not necessarily provided.

[0375]

10 The insulating film 420 may be formed using a single layer or a stacked layer of an insulating film containing one or more kinds of an aluminum oxide, a magnesium oxide, a silicon oxide, a silicon oxynitride, a silicon nitride oxide, a silicon nitride, a gallium oxide, a germanium oxide, an yttrium oxide, a zirconium oxide, a lanthanum oxide, a neodymium oxide, a hafnium oxide, and a tantalum oxide.

15 [0376]

An opening reaching the drain electrode 416b of the transistor Tr1d is provided in the insulating film 420, the insulating film 802, the gate insulating film 412, and the oxide semiconductor film 406. The source electrode 816a of the transistor Tr2d is in contact with the drain electrode 416b of the transistor Tr1d through the opening.

20 [0377]

In the case where the transistor described in the above embodiments is applied to the transistor Tr2d, the off-state current of the transistor Tr2d is extremely small, and thus the shoot-through current in the case where the transistor Tr2d is off is also extremely small. Accordingly, a low power consumption inverter can be achieved.

25 [0378]

This embodiment can be implemented in appropriate combination with any of the other embodiments.

[0379]

[Embodiment 6]

30 In this embodiment, a static random access memory (SRAM) which is a semiconductor device including a flip-flop to which the inverters described in Embodiment 5 are applied is described.

[0380]

The SRAM, which retains data with the use of the flip-flop, does not need the refresh operation unlike a dynamic random access memory (DRAM). Therefore, power consumption in retaining data can be suppressed. In addition, since a capacitor is not used, the SRAM is suitable for application which requires high-speed operation.

[0381]

FIG. 25 is a circuit diagram of a memory cell of an SRAM of one embodiment of the present invention. FIG. 25, which shows one memory cell, may be applied to a memory cell array in which the plurality of memory cells are arranged.

[0382]

The memory cell illustrated in FIG. 25 includes a transistor Tr1e, a transistor Tr2e, a transistor Tr3e, a transistor Tr4e, a transistor Tr5e, and a transistor Tr6e. The transistor Tr1e and the transistor Tr2e are p-channel transistors, and the transistor Tr3e and the transistor Tr4e are n-channel transistors. A gate of the transistor Tr1e is electrically connected to a drain of the transistor Tr2e, a gate of the transistor Tr3e, a drain of the transistor Tr4e, and one of a source and a drain of the transistor Tr6e. A source of the transistor Tr1e is electrically connected to VDD. A drain of the transistor Tr1e is electrically connected to a gate of the transistor Tr2e, a drain of the transistor Tr3e, and one of a source and a drain of the transistor Tr5e. A source of the transistor Tr2e is electrically connected to VDD. A source of the transistor Tr3e is electrically connected to GND. A back gate of the transistor Tr3e is electrically connected to a back-gate line BGL. A source of the transistor Tr4e is electrically connected to GND. A back gate of the transistor Tr4e is electrically connected to a back-gate line BGL. A gate of the transistor Tr5e is electrically connected to a word line WL. The other of the source and the drain of the transistor Tr5e is electrically connected to a bit line BLB. A gate of the transistor Tr6e is electrically connected to the word line WL. The other of the source and the drain of the transistor Tr6e is electrically connected to a bit line BL.

[0383]

Described in this embodiment is an example in which n-channel transistors are applied to the transistors Tr5e and Tr6e. However, the transistors Tr5e and Tr6e are not limited to the n-channel transistors, and p-channel transistors may be applied thereto,

and accordingly the method of writing, retaining, and reading data described below is changed as appropriate.

[0384]

In this manner, the inverter including the transistors Tr1e and Tr3e is connected
5 to the inverter including the transistors Tr2e and Tr4e in ring connection, whereby the flip-flop is configured.

[0385]

A transistor including, for example, silicon may be applied to the p-channel transistor. However, the p-channel transistor is not limited to the transistor including
10 silicon. Further, the transistor including the oxide semiconductor film, which is described in the above embodiments, may be used as the n-channel transistor.

[0386]

In this embodiment, the transistor including the oxide semiconductor film, which is described in the above embodiments, is applied to each of the transistors Tr3e
15 and Tr4e. Since the off-state current of the transistor is extremely small, the shoot-through current is also extremely small.

[0387]

Instead of the p-channel transistors, n-channel transistors may be applied to the transistors Tr1e and Tr2e. In the case where n-channel transistors are used as the
20 transistors Tr1e and Tr2e, depression transistors may be applied thereto with reference to the description of FIGS. 24A and 24B.

[0388]

Data writing, retaining, and reading of the memory cell shown in FIG. 25 are described below.

25 [0389]

In the case where data is written, first, potentials corresponding to data 0 or data 1 are applied to the bit line BL and the bit line BLB.

[0390]

For example, in the case where data 1 is to be written, the bit line BL and the
30 bit line BLB are set to VDD and GND, respectively. Next, a potential (VH) which is greater than or equal to a potential obtained by adding VDD to the threshold voltage of the transistor Tr5e and Tr6e is applied to the word line WL.

[0391]

Next, the potential of the word line WL is changed to a potential lower than the threshold voltage of the transistor Tr5e and Tr6e, so that the data 1 written into the flip-flop is retained. In the case of an SRAM, the current flowing during a period of retaining data is only the leak current of the transistor. Therefore, by applying the transistor including the oxide semiconductor film, which is described in the above embodiments, to the transistor included in the SRAM, standby electricity for data retention can be reduced because the off-state current of the transistor is extremely small, i.e., the leak current attributed to the transistor is extremely small.

[0392]

In the case where the data is read, first, the bit line BL and the bit line BLB are set to VDD in advance. Next, VH is applied to the word line WL, so that the potential of the bit line BL remains VDD but the bit line BLB is discharged through the transistors Tr5e and Tr3e to be GND. This difference between the potential of the bit line BL and the potential of the bit line BLB is amplified by a sense amplifier (not shown); whereby the retained data 1 can be read.

[0393]

In the case where data 0 is to be written, the bit line BL and the bit line BLB are set to GND and VDD, respectively, and then, VH is applied to the word line WL. Next, the potential of the word line WL is changed to a potential lower than the threshold voltage of the transistor Tr5e and Tr6e, so that the data 0 written into the flip-flop is retained. In the case where the data is read, first, the bit line BL and the bit line BLB are set to VDD, and then, VH is applied to the word line WL, so that the potential of the bit line BLB remains VDD but the bit line BL is discharged through the transistors Tr6e and Tr4e to be GND. This difference between the potential of the bit line BL and the potential of the bit line BLB is amplified by the sense amplifier, whereby the retained data 0 can be read.

[0394]

According to this embodiment, an SRAM with low standby electricity can be provided.

[0395]

This embodiment can be implemented in appropriate combination with any of

the other embodiments.

[0396]

[Embodiment 7]

5 The off-state current of the transistor including the oxide semiconductor film, which is described in the above embodiments, can be made extremely small. That is, the transistor has such electrical characteristics in which leakage of charge through the transistor is less likely to occur.

[0397]

10 A semiconductor device including a memory element to which the transistor having such electrical characteristics and which has a greater function than a semiconductor device including a conventional memory element is described below.

[0398]

15 First, a semiconductor device is specifically described with reference to FIGS. 26A to 26D. FIG. 26A is a circuit diagram of a memory cell array of the semiconductor device. FIG. 26B is a circuit diagram of a memory cell. FIG. 26C illustrates an example of the cross-sectional structure of the memory cell shown in FIG. 26B. Further, FIG. 26D is a graph showing electrical characteristics of the memory cell shown in FIG. 26B.

[0399]

20 The memory cell array shown in FIG. 26A includes memory cells 556, bit lines 553, word lines 554, capacitor lines 555, and sense amplifiers 558.

[0400]

25 The bit lines 553 and the word lines 554 are provided in a grid pattern, and the memory cell 556 is provided per intersection of the bit line 553 and the word line 554. The bit line 553 is connected to the sense amplifier 558. The potential of the bit line 553 is read as data by the sense amplifier 558.

[0401]

30 In FIG. 26B, the memory cell 556 includes a transistor 551 and a capacitor 552. A gate of the transistor 551 is electrically connected to the word line 554, a source of the transistor 551 is electrically connected to the bit line 553, and a drain of the transistor 551 is electrically connected to one electrode of the capacitor 552. The other electrode of the capacitor 552 is electrically connected to the capacitor line 555.

[0402]

FIG. 26C illustrates an example of the cross-sectional structure of the memory cell. FIG. 26C is a cross-sectional view of a semiconductor device including the transistor 551, the wiring 524a and the wiring 524b which are connected to the transistor 551, an insulating film 520 over the transistor 551 and the wirings 524a and 524b, and the capacitor 552 over the insulating film 520.

[0403]

In FIG. 26C, the transistor illustrated in FIGS. 21A to 21C is applied to the transistor 551. Therefore, for components of the transistor 551 other than the components described below, refer to the description in the above embodiment.

[0404]

For the insulating film 520, refer to the description of the interlayer insulating film 518. A resin film made of a polyimide resin, an acrylic resin, an epoxy resin, a silicone resin, or the like may be used as the insulating film 520.

[0405]

The capacitor 552 includes an electrode 526 which is in contact with the wiring 524b, an electrode 528 which overlaps with the electrode 526, and an insulating film 522 which is provided between the electrodes 526 and 528.

[0406]

The electrode 526 may be formed using a single layer or a stacked layer of a simple substance, a nitride, an oxide, or an alloy containing one or more kinds of aluminum, titanium, chromium, cobalt, nickel, copper, yttrium, zirconium, molybdenum, silver, tantalum, and tungsten.

[0407]

The electrode 528 may be formed using a single layer or a stacked layer of a simple substance, a nitride, an oxide, or an alloy containing one or more kinds of aluminum, titanium, chromium, cobalt, nickel, copper, yttrium, zirconium, molybdenum, silver, tantalum, and tungsten.

[0408]

The insulating film 522 may be formed using a single layer or a stacked layer including an insulating film containing one or more kinds of an aluminum oxide, a magnesium oxide, a silicon oxide, a silicon oxynitride, a silicon nitride oxide, a silicon

nitride, a gallium oxide, a germanium oxide, an yttrium oxide, a zirconium oxide, a lanthanum oxide, a neodymium oxide, a hafnium oxide, and a tantalum oxide.

[0409]

Although the example in which the transistor 551 and the capacitor 552 are provided in different layers is illustrated in FIG. 26C, the present invention is not limited thereto. For example, the transistor 551 and the capacitor 552 may be provided in the same plane, which enables a memory cell having the same structure to be stacked over the memory cell. By stacking a plurality of memory cells, a large number of memory cells can be integrated in the area for one memory cell. Accordingly, the degree of integration of the semiconductor device can be increased. Note that in this specification, "A overlaps with B" means that A and B are provided such that at least part of A overlaps with at least part of B.

[0410]

The wiring 524a in FIG. 26C is electrically connected to the bit line 553 in FIG. 26B. The gate electrode 504 in FIG. 26C is electrically connected to the word line 554 in FIG. 26B. The electrode 528 in FIG. 26C is electrically connected to the capacitor line 555 in FIG. 26B.

[0411]

As shown in FIG. 26D, a voltage retained in the capacitor 552 decreases gradually due to leak through the transistor 551 as time passes. A voltage which has been charged from V_0 to V_1 decreases to V_A which is a limit for reading data 1 as a certain period of time passes. This period is referred to as a retaining period T_1 . That is, in the case of a two-level memory cell, refresh operation needs to be performed within the retaining period T_1 .

[0412]

For example, in the case where the off-state current of the transistor 551 is not sufficiently small, the amount of change of a voltage retained in the capacitor 552 with time is large, resulting in a reduction in the retaining period T_1 . Consequently, the frequency of refresh operations needs to be increased, which leads to an increase in power consumption of the semiconductor device.

[0413]

Since the off-state current of the transistor 551 is extremely small in this embodiment, the retaining period T_1 can be made extremely long. That is, the frequency of refresh operations can be reduced, which results in reduction in power consumption. For example, in the case where the transistor 551 in the memory cell has an off-state current of 1×10^{-21} A to 1×10^{-25} A, data can be retained for several days to several decades during which power is not supplied.

[0414]

As described above, according to one embodiment of the present invention, a semiconductor device with high integration degree and low power consumption can be provided.

[0415]

Next, a semiconductor device which is different from FIGS. 26A to 26D is described with reference to FIGS. 27A to 27C. FIG. 27A is a circuit diagram including a memory cell and wirings of the semiconductor device. FIG. 27B is a graph showing electrical characteristics of the memory cell shown in FIG. 27A. FIG. 27C illustrates an example of the cross-sectional structure of the memory cell shown in FIG. 27A.

[0416]

In FIG. 27A, the memory cell includes a transistor 671, a transistor 672, and a capacitor 673. A gate of the transistor 671 is electrically connected to a word line 676, and a source of the transistor 671 is electrically connected to a source line 674. A drain of the transistor 671 is electrically connected to a gate of the transistor 672 and one electrode of the capacitor 673; this connection portion is referred to as a node 679. A source of the transistor 672 is electrically connected to a source line 675, and a drain of the transistor 672 is electrically connected to a drain line 677. The other electrode of the capacitor 673 is electrically connected to a capacitor line 678.

[0417]

The semiconductor device shown in FIGS. 27A to 27C utilizes the fact that the apparent threshold voltage of the transistor 672 is changed in accordance with the potential of the node 679. For example, FIG. 27B is a graph showing a relation between the voltage V_{CL} of the capacitor line 678 and the drain current I_{d_2} flowing through the transistor 672.

[0418]

The potential of the node 679 can be controlled through the transistor 671. For example, the potential of the source line 674 is set to a power source potential VDD. In that case, when the potential of the word line 676 is set to be greater than or equal to a potential obtained by adding the power source potential VDD to the threshold voltage V_{th} of the transistor 671, the voltage of the node 679 can be HIGH. On the other hand, when the potential of the word line 676 is set to be less than or equal to the threshold voltage V_{th} of the transistor 671, the potential of the node 679 can be LOW.

[0419]

Therefore, the transistor 672 has either electrical characteristics shown by a curve $V_{CL} - I_{d_2}$ denoted by LOW or electrical characteristics shown by a curve $V_{CL} - I_{d_2}$ denoted by HIGH. That is, when the potential of the node 679 is LOW, data 0 is stored at V_{CL} of 0 V because I_{d_2} is small. Further, when the potential of the node 679 is HIGH, data 1 is stored at V_{CL} of 0 V because I_{d_2} is large. In this manner, data can be stored.

[0420]

FIG. 27C illustrates an example of the cross-sectional structure of the memory cell. FIG. 27C is a cross-sectional view of a semiconductor device including the transistor 672, an insulating film 668 over the transistor 672, the transistor 671 over the insulating film 668, an insulating film 620 over the transistor 671, and the capacitor 673 over the insulating film 620.

[0421]

For the insulating film 620, refer to the description of the protective insulating film 118. A resin film made of a polyimide resin, an acrylic resin, an epoxy resin, a silicone resin, or the like may be used as the insulating film 620.

[0422]

In FIG. 27C, the transistor illustrated in FIGS. 20A to 20C is applied to the transistor 671. Therefore, for components of the transistor 671 other than the components described below, refer to the description in the above embodiment.

[0423]

A transistor including crystalline silicon has an advantage of higher capability

of increasing the on-state characteristics over a transistor including an oxide semiconductor film, and is therefore suitable for the transistor 672 that needs high on-state characteristics.

[0424]

5 The transistor 672 includes the channel region 656 and impurity regions 657 in the semiconductor substrate 650, the element separation layer 664 which fills a groove in the semiconductor substrate 650, the gate insulating film 662 over the semiconductor substrate 650, and the gate electrode 654 over the channel region 656 with the gate insulating film 662 provided therebetween.

10 [0425]

As the semiconductor substrate 650, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate made of silicon, silicon carbide, or the like, or a compound semiconductor substrate made of silicon germanium or the like may be used.

[0426]

15 Although the structure in which the transistor 672 is provided in the semiconductor substrate is described in this embodiment, the present invention is not limited thereto. For example, a substrate having an insulating surface may be used instead of the semiconductor substrate, and a semiconductor film may be provided on the insulating surface. As the substrate having an insulating surface, a glass substrate,
20 a ceramic substrate, a quartz substrate, or a sapphire substrate may be used, for example. The transistor including the oxide semiconductor film, which is described in the above embodiments, may be applied to the transistor 672.

[0427]

25 The impurity regions 657 are each a region of the semiconductor substrate 650 containing an impurity imparting one conductivity type.

[0428]

30 The element separation layer 664 may be formed using a single layer or a stacked layer of an insulating film containing one or more kinds of an aluminum oxide, a magnesium oxide, a silicon oxide, a silicon oxynitride, a silicon nitride oxide, a silicon nitride, a gallium oxide, a germanium oxide, an yttrium oxide, a zirconium oxide, a lanthanum oxide, a neodymium oxide, a hafnium oxide, and a tantalum oxide.

[0429]

The gate insulating film 662 may be formed using a single layer or a stacked layer of an insulating film containing one or more kinds of an aluminum oxide, a magnesium oxide, a silicon oxide, a silicon oxynitride, a silicon nitride oxide, a silicon nitride, a gallium oxide, a germanium oxide, an yttrium oxide, a zirconium oxide, a lanthanum oxide, a neodymium oxide, a hafnium oxide, and a tantalum oxide.

[0430]

For the gate electrode 654, refer to the description of the gate electrode 104.

[0431]

For the insulating film 668, refer to the description of the protective insulating film 118. A resin film made of a polyimide resin, an acrylic resin, an epoxy resin, a silicone resin, or the like may be used as the insulating film 668.

[0432]

The insulating film 668 and the base insulating film 602 have an opening reaching the gate electrode 654 of the transistor 672. The drain electrode 416b of the transistor 671 is in contact with the gate electrode 654 of the transistor 672 through the opening.

[0433]

The capacitor 673 includes an electrode 626 which is in contact with the drain electrode 416b, an electrode 628 which overlaps with the electrode 626, and an insulating film 622 which is provided between the electrodes 626 and 628.

[0434]

For the electrode 626, refer to the description of the electrode 526.

[0435]

For the electrode 628, refer to the description of the electrode 528.

[0436]

The source electrode 416a in FIG. 27C is electrically connected to the source line 674 in FIG. 27A. The gate electrode 404 in FIG. 27C is electrically connected to the word line 676 in FIG. 27A. The electrode 628 in FIG. 27C is electrically connected to the capacitor line 678 in FIG. 27A.

[0437]

Although the example in which the transistor 671 and the capacitor 673 are provided in different layers is illustrated in FIG. 27C, the present invention is not limited

thereto. For example, the transistor 671 and the capacitor 673 may be provided in the same plane, which enables a memory cell having the same structure to be stacked over the memory cell. By stacking a plurality of memory cells, a large number of memory cells can be integrated in the area for one memory cell. Accordingly, the degree of integration of the semiconductor device can be increased.

[0438]

By applying the transistor including the oxide semiconductor film, which is described in the above embodiments, to the transistor 671, leak of charge accumulated in the node 679 through the transistor 671 can be suppressed because the off-state current of the transistor is extremely small. Therefore, data can be retained for a long period. Further, as compared to a flash memory, a high voltage is not needed in writing data, and accordingly power consumption can be reduced and the operation speed can be increased.

[0439]

As described above, according to one embodiment of the present invention, a semiconductor device with high integration degree and low power consumption can be provided.

[0440]

This embodiment can be implemented in appropriate combination with any of the other embodiments.

[0441]

[Embodiment 8]

A central processing unit (CPU) can be formed with the use of the transistor including the oxide semiconductor film or the semiconductor device including the memory element described in the above embodiments, for at least part of the CPU.

[0442]

FIG. 28A is a block diagram showing a specific structure of a CPU. The CPU shown in FIG. 28A includes an arithmetic logic unit (ALU) 1191, an ALU controller 1192, an instruction decoder 1193, an interrupt controller 1194, a timing controller 1195, a register 1196, a register controller 1197, a bus interface (Bus I/F) 1198, a rewritable ROM 1199, and an ROM interface (ROM I/F) 1189 over a substrate 1190. A semiconductor substrate, an SOI substrate, a glass substrate, or the like is used as the substrate 1190.

The ROM 1199 and the ROM interface 1189 may be provided over a separate chip. The CPU shown in FIG. 28A is just an example in which the structure is simplified; an actual CPU may have various structures depending on its application.

[0443]

5 An instruction input to the CPU through the bus interface 1198 is input to the instruction decoder 1193 and decoded therein, and then input to the ALU controller 1192, the interrupt controller 1194, the register controller 1197, and the timing controller 1195.

[0444]

10 The ALU controller 1192, the interrupt controller 1194, the register controller 1197, and the timing controller 1195 conduct various controls in accordance with the decoded instruction. Specifically, the ALU controller 1192 generates signals for controlling the operation of the ALU 1191. While the CPU is executing a program, the interrupt controller 1194 judges an interrupt request from an external input/output device or a peripheral circuit on the basis of its priority or a mask state, and processes the request.

15 The register controller 1197 generates an address of the register 1196, and reads/writes data from/to the register 1196 in accordance with the state of the CPU.

[0445]

20 The timing controller 1195 generates signals for controlling operation timings of the ALU 1191, the ALU controller 1192, the instruction decoder 1193, the interrupt controller 1194, and the register controller 1197. For example, the timing controller 1195 has an internal clock generator for generating an internal clock signal CLK2 based on a reference clock signal CLK1, and supplies the clock signal CLK2 to the above circuits.

[0446]

25 In the CPU shown in FIG. 28A, a memory element is provided in the register 1196. In the register 1196, the semiconductor device including the memory element described in the above embodiments can be used.

[0447]

30 In the CPU shown in FIG. 28A, the register controller 1197 selects operation of retaining data in the register 1196 in accordance with an instruction from the ALU 1191. That is, the register controller 1197 selects whether data is retained by a flip-flop or data is retained by a capacitor in the memory element included in the register 1196. When data

is retained by the flip-flop, a power source voltage is supplied to the memory element in the register 1196. When data is retained by the capacitor, the data in the capacitor is rewritten, and supply of the power source voltage to the memory element in the register 1196 can be stopped.

5 [0448]

The power supply can be stopped by a switching element provided between the memory element group and the node to which a power source potential VDD or a power source potential VSS is applied, as shown in FIG. 28B or FIG. 28C. Circuits illustrated in FIGS. 28B and 28C are described below.

10 [0449]

FIGS. 28B and 28C each illustrate an example of the structure using the transistor including the oxide semiconductor film, which is described in the above embodiments, as the switching element for controlling supply of the power source potential to the memory element.

15 [0450]

A memory device shown in FIG. 28B includes a switching element 1141 and a memory element group 1143 including a plurality of memory elements 1142. Specifically, as each of the memory elements 1142, the semiconductor device including the memory element described in the above embodiments can be used. Each of the memory elements 1142 included in the memory element group 1143 is supplied with the high-level power source potential VDD through the switching element 1141. Further, each of the memory elements 1142 included in the memory element group 1143 is supplied with the potential of a signal IN and the potential of the low-level power source potential VSS.

25 [0451]

In FIG. 28B, the transistor including the oxide semiconductor film, which is described in the above embodiments, is used as the switching element 1141. The off-state current of the transistor can be made extremely small. The switching of the transistor is controlled by a signal SigA input to a gate thereof.

30 [0452]

Although FIG. 28B shows the structure in which the switching element 1141 includes only one transistor, the present invention is not limited thereto; a plurality of

transistors may be included. In the case where the switching element 1141 includes a plurality of transistors which function as switching elements, the plurality of transistors may be connected to each other in parallel, in series, or in combination of parallel connection and series connection.

5 [0453]

In FIG. 28C, an example of a memory device in which each of the memory elements 1142 included in the memory element group 1143 is supplied with the low-level power source potential VSS through the switching element 1141 is illustrated. The supply of the low-level power source potential VSS to each of the memory elements 1142 included in the memory element group 1143 can be controlled by the switching element 1141.

[0454]

With the switching element provided between the memory element group and the node to which the power source potential VDD or the power source potential VSS is supplied, data can be retained even in the case where an operation of the CPU is temporarily stopped and the supply of the power source voltage is stopped; accordingly, power consumption can be reduced. For example, while a user of a personal computer does not input data to an input device such as a keyboard, the operation of the CPU can be stopped, whereby the power consumption can be reduced.

20 [0455]

Although the CPU is given as an example in this embodiment, the transistor can also be applied to an LSI such as a digital signal processor (DSP), a custom LSI, or a field programmable gate array (FPGA).

[0456]

25 This embodiment can be implemented in appropriate combination with any of the other embodiments.

[0457]

[Embodiment 9]

30 In this embodiment, a display device to which the transistor described in the above embodiments is applied is described.

[0458]

As a display element provided in the display device, a liquid crystal element

(also referred to as a liquid crystal display element), a light-emitting element (also referred to as a light-emitting display element), or the like can be used. The light-emitting element includes, in its category, an element whose luminance is controlled by current or voltage, specifically an inorganic electroluminescent (EL) element, an organic EL element, and the like. Furthermore, a display medium whose contrast is changed by an electric effect, such as electronic ink, can be used as the display element. In this embodiment, a display device including an EL element and a display device including a liquid crystal element are described as examples of the display device.

[0459]

The display device in this embodiment includes in its category a panel in which a display element is sealed, and a module in which an IC such as a controller or the like is mounted on the panel.

[0460]

The display device in this embodiment also refers to an image display device, a display device, or a light source (including a lighting device). The display device includes any of the following modules: a module provided with a connector such as an FPC or TCP; a module in which a printed wiring board is provided at the end of TCP; and a module in which an integrated circuit (IC) is mounted directly on a display element by a COG method.

[0461]

FIG. 29 is an example of the circuit diagram of a pixel of a display device including an EL element.

[0462]

The display device shown in FIG. 29 includes a switching element 743, a transistor 741, a capacitor 742, and a light-emitting element 719.

[0463]

A gate of the transistor 741 is electrically connected to one electrode of the switching element 743 and one electrode of the capacitor 742. A source of the transistor 741 is electrically connected to one terminal of the light-emitting element 719. A drain of the transistor 741 is electrically connected to the other electrode of the capacitor 742, to which a power source potential VDD is supplied. The other electrode of the switching element 743 is electrically connected to a signal line 744. A constant

potential is supplied to the other terminal of the light-emitting element 719. The constant potential is a ground potential GND or a potential lower than the ground potential GND.

[0464]

5 The transistor including the oxide semiconductor film, which is described in the above embodiments, is used as the transistor 741. The transistor has stable electrical characteristics. Accordingly, a display device having high display quality can be provided.

[0465]

10 A transistor is preferably used as the switching element 743, which enables the pixel area to be small, so that a display device with high resolution can be achieved. The transistor including the oxide semiconductor film, which is described in the above embodiments, may be used as the switching element 743; accordingly, the switching element 743 can be fabricated by the same process as the transistor 741, which leads to
15 an improvement in the productivity of the display device.

[0466]

FIG. 30A is a top view of a display device including an EL element. The display device including an EL element includes a substrate 100, a substrate 700, a seal material 734, a driver circuit 735, a driver circuit 736, a pixel 737, and an FPC 732.
20 The seal material 734 is provided between the substrate 100 and the substrate 700 so as to surround the pixel 737, the driver circuit 735, and the driver circuit 736. The driver circuit 735 and/or the driver circuit 736 may be provided outside the seal material 734.

[0467]

FIG. 30B is a cross-sectional view of the display device including an EL
25 element taken along dashed-dotted line M-N in FIG. 30A. The FPC 732 is connected to a wiring 733a through a terminal 731. The wiring 733a is the same layer as the gate electrode 104.

[0468]

FIG. 30B illustrates the example in which the transistor 741 and the capacitor
30 742 are provided in the same plane. With such a structure, the capacitor 742 can be fabricated in the same planes as the gate electrode, the gate insulating film, and the source (drain) electrode of the transistor 741. Such provision of the transistor 741 and

the capacitor 742 in the same plane leads to shortening of the manufacturing process of the display device and an improvement of the productivity.

[0469]

FIG. 30B illustrates the example in which the transistor illustrated in FIGS. 16A to 16C is applied to the transistor 741. Therefore, for components of the transistor 741 other than the components described below, refer to the description of the above embodiment.

[0470]

An insulating film 720 is provided over the transistor 741 and the capacitor 742.

[0471]

Here, an opening reaching the source electrode 116a of the transistor 741 is provided in the insulating film 720 and the protective insulating film 118.

[0472]

An electrode 781 is provided over the insulating film 720. The electrode 781 is in contact with the source electrode 116a of the transistor 741 through the opening provided in the insulating film 720 and the protective insulating film 118.

[0473]

Over the electrode 781, a bank 784 having an opening reaching the electrode 781 is provided.

[0474]

Over the bank 784, a light-emitting layer 782 in contact with the electrode 781 through the opening provided in the bank 784 is provided.

[0475]

An electrode 783 is provided over the light-emitting layer 782.

[0476]

A region where the electrode 781, the light-emitting layer 782, and the electrode 783 overlap with one another serves as the light-emitting element 719.

[0477]

For the insulating film 720, refer to the protective insulating film 118. A resin film made of a polyimide resin, an acrylic resin, an epoxy resin, a silicone resin, or the like may be used as the insulating film 720.

[0478]

The light-emitting layer 782 is not limited to one layer and may be a stacked layer of plural kinds of light-emitting layers. For example, a structure illustrated in FIG. 30C may be used. FIG. 30C illustrates a structure in which an intermediate layer 785a, a light-emitting layer 786a, an intermediate layer 785b, a light-emitting layer 786b, an intermediate layer 785c, a light-emitting layer 786c, and an intermediate layer 785d are stacked in this order. By using light-emitting layers whose emission colors are appropriate as the light-emitting layer 786a, the light-emitting layer 786b, and the light-emitting layer 786c, the light-emitting element 719 can be provided with high color rendering properties or high luminous efficiency.

[0479]

White light may be provided by stacking plural kinds of light-emitting layers. Although not illustrated in FIG. 30B, a structure in which white light is extracted through a coloring layer may be employed.

[0480]

Although the structure in which three light-emitting layers and four intermediate layers are provided is illustrated here, the number of light-emitting layers and the number of intermediate layers can be changed as appropriate without being limited thereto. For example, the light-emitting layer 782 may be formed with the intermediate layer 785a, the light-emitting layer 786a, the intermediate layer 785b, the light-emitting layer 786b, and the intermediate layer 785c. Alternatively, the light-emitting layer 782 may be formed with the intermediate layer 785a, the light-emitting layer 786a, the intermediate layer 785b, the light-emitting layer 786b, the light-emitting layer 786c, and the intermediate layer 785d, and the intermediate layer 785c may be omitted.

[0481]

The intermediate layer can be formed using a stacked-layer structure of a hole-injection layer, a hole-transport layer, an electron-transport layer, an electron-injection layer, or the like. Not all of these layers need to be provided in the intermediate layer; these layers may be selected as appropriate. Further, layers having the same functions may be provided to overlap with each other. Further, an electron-relay layer or the like may be added as appropriate as the intermediate layer, in addition to a carrier generation layer.

[0482]

As the electrode 781, a conductive film having visible light permeability may be used. Having visible light permeability means to have an average transmittance of 70 % or more, particularly 80 % or more in the visible light region (e.g., the range of wavelength of from 400 nm to 800 nm).

[0483]

As the electrode 781, for example, an oxide film such as an In-Zn-W oxide film, an In-Sn oxide film, an In-Zn oxide film, an In oxide film, a Zn oxide film, or an Sn oxide film may be used. Further, a slight amount of Al, Ga, Sb, F, or the like may be added to the above-described oxide film. A metal thin film having a thickness thin enough to transmit light (preferably, approximately 5 nm to 30 nm) can also be used. For example, an Ag film, a Mg film, or an Ag-Mg alloy film with a thickness of 5 nm may be used.

[0484]

Alternatively, a film on which visible light is reflected efficiently is preferably used as the electrode 781. For example, a film containing lithium, aluminum, titanium, magnesium, lanthanum, silver, silicon, or nickel may be used as the electrode 781.

[0485]

As the electrode 783, any of the films described for the electrode 781 can be used. Note that in the case where the electrode 781 has visible light permeability, it is preferable that the electrode 783 reflect visible light efficiently, and in the case where the electrode 781 reflects visible light efficiently, it is preferable that the electrode 783 have visible light permeability.

[0486]

Although the electrodes 781 and 783 are provided in accordance with the structure illustrated in FIG. 30B, the positions of the electrodes 781 and 783 may be replaced with each other. It is preferable to use a conductive film having a high work function for the electrode which functions as an anode, and a conductive film having a low work function for the electrode which functions as a cathode. However, in the case where a carrier generation layer is provided in contact with the anode, a variety of conductive films can be used for the anode regardless of their work functions.

[0487]

For the bank 784, refer to the protective insulating film 118. A resin film made of a polyimide resin, an acrylic resin, an epoxy resin, a silicone resin, or the like may be used as the bank 784.

[0488]

5 The transistor 741 connected to the light-emitting element 719 has stable electrical characteristics. Accordingly, a display device having high display quality can be provided.

[0489]

10 FIGS. 31A and 31B are examples of the cross-sectional view of a display device including an EL element, which are partly different from FIG. 30B. Specifically, the wiring connected to the FPC 732 is different in them. In FIG. 31A, the FPC 732 is connected to a wiring 733b through the terminal 731. The wiring 733b is the same layer as the source electrode 116a and the drain electrode 116b. In FIG. 31B, the FPC 732 is connected to a wiring 733c through the terminal 731. The wiring 733c is the
15 same layer as the electrode 781.

[0490]

Next, a display device including a liquid crystal element is described.

[0491]

20 FIG. 32 is a circuit diagram illustrating a configuration example of the pixel of a display device including a liquid crystal element. A pixel 750 shown in FIG. 32 includes a transistor 751, a capacitor 752, and an element (hereinafter also referred to as liquid crystal element) 753 in which a space between a pair of electrodes is filled with a liquid crystal.

[0492]

25 One of a source and a drain of the transistor 751 is electrically connected to a signal line 755, and a gate of the transistor 751 is electrically connected to a scan line 754.

[0493]

30 One electrode of the capacitor 752 is electrically connected to the other of the source and the drain of the transistor 751, and the other electrode of the capacitor 752 is electrically connected to a wiring to which a common potential is supplied.

[0494]

One electrode of the liquid crystal element 753 is electrically connected to the

other of the source and the drain of the transistor 751, and the other electrode of the liquid crystal element 753 is electrically connected to a wiring to which a common potential is supplied. The common potential supplied to the wiring electrically connected to the other electrode of the capacitor 752 may be different from that supplied to the wiring electrically connected to the other electrode of the liquid crystal element 753.

[0495]

The top view of the display device including a liquid crystal element is similar to that of the display device including an EL element. A cross-sectional view of the display device including a liquid crystal element taken along dashed-dotted line M-N in FIG. 30A is illustrated in FIG. 33A. In FIG. 33A, the FPC 732 is connected to the wiring 733a through the terminal 731. The wiring 733a is the same layer as the gate electrode 104.

[0496]

FIG. 33A illustrates the example in which the transistor 751 and the capacitor 752 are provided in the same plane. With such a structure, the capacitor 752 can be fabricated in the same planes as the gate electrode, the gate insulating film, and the source (drain) electrode of the transistor 751. Such provision of the transistor 751 and the capacitor 752 in the same plane leads to shortening of the manufacturing process of the display device and an improvement of the productivity.

[0497]

The transistor described in the above embodiments can be applied to the transistor 751. FIG. 33A illustrates an example in which the transistor illustrated in FIGS. 16A to 16C is applied to the transistor 751. Therefore, for components of the transistor 751 other than the components described below, refer to the description of the above embodiment.

[0498]

The off-state current of the transistor 751 can be made extremely small. Therefore, charge retained in the capacitor 752 is unlikely to leak, so that the voltage applied to the liquid crystal element 753 can be maintained for a long time. Accordingly, the transistor 751 can be kept off during a period in which moving images with few motions or a still image are/is displayed, whereby power for the operation of

the transistor 751 can be saved in that period; accordingly a display device with low power consumption can be provided.

[0499]

An insulating film 721 is provided over the transistor 751 and the capacitor
5 752.

[0500]

Here, an opening reaching the drain electrode 116b of the transistor 751 is provided in the insulating film 721 and the protective insulating film 118.

[0501]

10 An electrode 791 is provided over the insulating film 721. The electrode 791 is in contact with the drain electrode 116b of the transistor 751 through the opening provided in the insulating film 721 and the protective insulating film 118.

[0502]

15 An insulating film 792 which functions as an alignment film is provided over the electrode 791.

[0503]

A liquid crystal layer 793 is provided over the insulating film 792.

[0504]

20 An insulating film 794 which functions as an alignment film is provided over the liquid crystal layer 793.

[0505]

A spacer 795 is provided over the insulating film 794.

[0506]

An electrode 796 is provided over the spacer 795 and the insulating film 794.

25 [0507]

A substrate 797 is provided over the electrode 796.

[0508]

30 For the insulating film 721, refer to the protective insulating film 118. A resin film made of a polyimide resin, an acrylic resin, an epoxy resin, a silicone resin, or the like may be used as the insulating film 721.

[0509]

For the liquid crystal layer 793, a thermotropic liquid crystal, a low-molecular

liquid crystal, a high-molecular liquid crystal, a high-molecular distributed liquid crystal, a ferroelectric liquid crystal, an anti-ferroelectric liquid crystal, or the like may be used. Such a liquid crystal exhibits a cholesteric phase, a smectic phase, a cubic phase, a chiral nematic phase, an isotropic phase, or the like depending on conditions.

5 [0510]

A liquid crystal exhibiting a blue phase may be used as the liquid crystal layer 793. In that case, the insulating films 792 and 794, which function as alignment films, may be omitted.

[0511]

10 As the electrode 791, a conductive film having visible light permeability may be used.

[0512]

As the electrode 791, for example, an oxide film such as an In-Zn-W oxide film, an In-Sn oxide film, an In-Zn oxide film, an In oxide film, a Zn oxide film, or an Sn oxide film may be used. Further, a slight amount of Al, Ga, Sb, F, or the like may be added to the above-described oxide film. A metal thin film having a thickness thin enough to transmit light (preferably, approximately 5 nm to 30 nm) can also be used.

15 [0513]

Alternatively, a film on which visible light is reflected efficiently is preferably used as the electrode 791. For example, a film containing aluminum, titanium, chromium, copper, molybdenum, silver, tantalum, or tungsten may be used as the electrode 791.

20 [0514]

As the electrode 796, any of the films described for the electrode 791 can be used. Note that in the case where the electrode 791 has visible light permeability, it is preferable that the electrode 796 reflect visible light efficiently, and in the case where the electrode 791 reflects visible light efficiently, it is preferable that the electrode 796 have visible light permeability.

25 [0515]

30 Although the electrodes 791 and 796 are provided in accordance with the structure illustrated in FIG. 33A, the positions of the electrodes 791 and 796 may be replaced with each other.

[0516]

Each of the insulating films 792 and 794 may be formed using an organic compound or an inorganic compound.

[0517]

5 The spacer 795 may be formed using an organic compound or an inorganic compound. The spacer 795 can have any shape such as a column shape or spherical shape.

[0518]

10 A region where the electrode 791, the insulating film 792, the liquid crystal layer 793, the insulating film 794, and the electrode 796 overlap with one another serves as the liquid crystal element 753.

[0519]

Glass, resin, metal, or the like may be used for the substrate 797. The substrate 797 may be flexible.

15 [0520]

FIGS. 33B and 33C are examples of the cross-sectional view of a display device including a liquid crystal element, which are partly different from FIG. 33A. Specifically, the wiring connected to the FPC 732 is different in them. In FIG. 33B, the FPC 732 is connected to the wiring 733b through the terminal 731. The wiring
20 733b is the same layer as the source electrode 116a and the drain electrode 116b. In FIG. 33C, the FPC 732 is connected to the wiring 733c through the terminal 731. The wiring 733c is the same layer as the electrode 791.

[0521]

25 The transistor 751 connected to the liquid crystal element 753 has stable electrical characteristics. Accordingly, a display device having a high display quality can be provided. Further, the off-state current of the transistor 751 can be made extremely small. Accordingly, a display device with low power consumption can be provided.

[0522]

30 This embodiment can be implemented in appropriate combination with any of the other embodiments.

[0523]

[Embodiment 10]

In this embodiment, examples of an electronic device to which the semiconductor device described in the above embodiments is applied are described.

[0524]

5 FIG. 34A illustrates a portable information terminal. The portable information terminal illustrated in FIG. 34A includes a housing 9300, a button 9301, a microphone 9302, a display portion 9303, a speaker 9304, and a camera 9305, and has a function as a mobile phone. One embodiment of the present invention can be applied to an arithmetic unit, a wireless circuit, or a memory circuit in its main body. One embodiment of the present invention can also be applied to the display portion 9303.

[0525]

 FIG. 34B illustrates a display. The display illustrated in FIG. 34B includes a housing 9310 and a display portion 9311. One embodiment of the present invention can be applied to an arithmetic unit, a wireless circuit, or a memory circuit in its main body. One embodiment of the present invention can also be applied to the display portion 9311.

[0526]

 FIG. 34C illustrates a digital still camera. The digital still camera illustrated in FIG. 34C includes a housing 9320, a button 9321, a microphone 9322, and a display portion 9323. One embodiment of the present invention can be applied to an arithmetic unit, a wireless circuit, or a memory circuit in its main body. One embodiment of the present invention can also be applied to the display portion 9323.

[0527]

 FIG. 34D illustrates a foldable portable information terminal. The foldable portable information terminal illustrated in FIG. 34D includes a housing 9630, a display portion 9631a, a display portion 9631b, a hinge 9633, and an operation switch 9638. One embodiment of the present invention can be applied to an arithmetic unit, a wireless circuit, or a memory circuit in its main body. One embodiment of the present invention can also be applied to the display portion 9631a and the display portion 9631b.

30 [0528]

 Part or whole of the display portion 9631a and/or the display portion 9631b can function as a touch panel, which enables data input by touching an operation key

displayed thereon.

[0529]

With the use of the semiconductor device of one embodiment of the present invention, a high performance electronic device with low power consumption can be provided.

[0530]

This embodiment can be implemented in appropriate combination with any of the other embodiments.

10 EXPLANATION OF REFERENCE

[0531]

100: substrate, 102: base insulating film, 104: gate electrode, 106: oxide semiconductor film, 112: gate insulating film, 114: back-gate electrode, 116a: source electrode, 116b: drain electrode, 118: protective insulating film, 200: substrate, 202: base insulating film, 204: gate electrode, 206: oxide semiconductor film, 212: gate insulating film, 216a: source electrode, 216b: drain electrode, 218: protective insulating film, 300: substrate, 302: base insulating film, 304: gate electrode, 306: oxide semiconductor film, 312: gate insulating film, 316a: source electrode, 316b: drain electrode, 400: substrate, 402: base insulating film, 404: gate electrode, 406: oxide semiconductor film, 412: gate insulating film, 416a: source electrode, 416b: drain electrode, 420: insulating film, 500: substrate, 502: base insulating film, 504: gate electrode, 506: oxide semiconductor film, 512: gate insulating film, 518: interlayer insulating film, 520: insulating film, 522: insulating film, 524a: wiring, 524b: wiring, 526: electrode, 528: electrode, 551: transistor, 552: capacitor, 553: bit line, 554: word line, 555: capacitor line, 556: memory cell, 558: sense amplifier, 602: base insulating film, 620: insulating film, 622: insulating film, 626: electrode, 628: electrode, 650: semiconductor substrate, 654: gate electrode, 656: channel region, 657: impurity region, 657a: source region, 657b: drain region, 662: gate insulating film, 664: element separation layer, 668: insulating film, 671: transistor, 672: transistor, 673: capacitor, 674: source line, 675: source line, 676: word line, 677: drain line, 678: capacitor line, 679: node, 690: insulating film, 700: substrate, 719: light-emitting element, 720: insulating film, 721: insulating film, 731: terminal, 732: FPC, 733a: wiring, 733b: wiring, 733c: wiring, 734: seal material, 735: driver circuit,

736: driver circuit, 737: pixel, 741: transistor, 742: capacitor, 743: switching element,
744: signal line, 750: pixel, 751: transistor, 752: capacitor, 753: liquid crystal element,
754: scan line, 755: signal line, 781: electrode, 782: light-emitting layer, 783: electrode,
784: bank, 785a: intermediate layer, 785b: intermediate layer, 785c: intermediate layer,
5 785d: intermediate layer, 786a: light-emitting layer, 786b: light-emitting layer, 786c:
light-emitting layer, 791: electrode, 792: insulating film, 793: liquid crystal layer, 794:
insulating film, 795: spacer, 796: electrode, 797: substrate, 802: insulating film, 806:
oxide semiconductor film, 812: gate insulating film, 814: gate electrode, 816a: source
electrode, 816b: drain electrode, 902: insulating film, 906: oxide semiconductor film,
10 912: gate insulating film, 914: gate electrode, 916a: source electrode, 916b: drain
electrode, 1000: sputtering target, 1001: ion, 1002: sputtered particle, 1003: deposition
surface, 1141: switching element, 1142: memory element, 1143: memory element group,
1189: ROM interface, 1190: substrate, 1191: ALU, 1192: ALU controller, 1193:
instruction decoder, 1194: interrupt controller, 1195: timing controller, 1196: register,
15 1197: register controller, 1198: bus interface, 1199: ROM, 4000: film formation
apparatus, 4001: atmosphere-side substrate supply chamber, 4002: atmosphere-side
substrate transfer chamber, 4003a: load lock chamber, 4003b: unload lock chamber,
4004: transfer chamber, 4005: substrate heating chamber, 4006a: film formation
chamber, 4006b: film formation chamber, 4006c: film formation chamber, 4032a:
20 sputtering target, 4032b: sputtering target, 4033a: cathode magnet, 4033b: cathode
magnet, 4035: substrate holder, 4101: cassette port, 4102: alignment port, 4103: transfer
robot, 4104: gate valve, 4105: heating stage, 4106: target, 4107: attachment protection
plate, 4108: substrate stage, 4109: substrate, 4110: cryotrap, 4111: stage, 4200: vacuum
pump, 4201: cryopump, 4202: turbo molecular pump, 4300: mass flow controller, 4301:
25 refiner, 4302: gas heating system, 9304: speaker, 9300: housing, 9301: button, 9302:
microphone, 9303: display portion, 9305: camera, 9310: housing, 9311: display portion,
9320: housing, 9321: button, 9322: microphone, 9323: display portion, 9630: housing,
9631a: display portion, 9631b: display portion, 9633: hinge, 9638: operation switch,
S101: step, S102: step, S103: step, S104: step, S111: step, S112: step, S113: step, and
30 S114: step.

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filed with the Japan Patent Office on June 29, 2012, Japanese Patent Application serial No. 2012-266243 filed with the Japan Patent Office on December 5, 2012, and Japanese Patent Application serial No. 2012-273482 filed with the Japan Patent Office on December 14, 2012, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A method for using a target comprising the steps of:
separating a plurality of particles charged positively from the target by
5 subjecting the target to sputtering; and
 depositing the plurality of particles repelling each other on a deposition
surface,
 wherein the target comprises a polycrystalline oxide including crystal grains,
and
10 wherein the particles have a flat plate shape.
2. The method for using a target according to claim 1, wherein the particles
have a hexagonal cylindrical shape.
- 15 3. The method for using a target according to claim 1, wherein the particles
have crystallinity.
4. The method for using a target according to claim 1,
 wherein the plurality of particles are generated by cleavage of the crystal grains
20 included in the target.
5. A method for using a target comprising the steps of:
separating a plurality of particles from the target; and
 positively charging the plurality of particles so that the plurality of particles are
25 deposited on a deposition surface while repelling each other,
 wherein the target comprises a polycrystalline oxide including crystal grains,
and
 wherein the particles have a flat plate shape.
- 30 6. The method for using a target according to claim 5, wherein the particles
have a hexagonal cylindrical shape.

7. The method for using a target according to claim 5, wherein the particles have crystallinity.

8. The method for using a target according to claim 5,
5 wherein the plurality of particles are generated by cleavage of the crystal grains included in the target.

9. A method for forming an oxide film comprising the steps of:
separating a plurality of particles charged positively from a target by subjecting
10 the target to collision of ions; and
depositing the plurality of particles repelling each other on a deposition surface,
wherein the target includes crystal grains,
wherein the particles have a flat plate shape, and
15 wherein the plurality of particles are deposited so as to be spread on the deposition surface with flat plate planes facing upward.

10. The method for forming an oxide film according to claim 9, wherein the particles have crystallinity.

20 11. The method for forming an oxide film according to claim 9, wherein a shape of the particle is a substantially hexagonal cylinder and a *c*-axis of a crystal is aligned in a direction perpendicular to a hexagonal plane of the substantially hexagonal cylinder.

25 12. The method for forming an oxide film according to claim 9,
wherein the plurality of particles are generated by cleavage of the crystal grains included in the target.

30 13. The method for forming an oxide film according to claim 9,
wherein the deposition surface is heated during the deposition of the plurality of particles.

14. A method for forming an oxide film comprising the steps of:

separating a plurality of particles from a target by subjecting the target to collision of ions; and

5 positively charging the plurality of particles so that the plurality of particles are deposited on a deposition surface while repelling each other,

wherein the target includes crystal grains,

wherein the particles have a flat plate shape, and

10 wherein the plurality of particles are deposited so as to be spread on the deposition surface with flat plate planes facing upward.

15 15. The method for forming an oxide film according to claim 14, wherein the particles have crystallinity.

16. The method for forming an oxide film according to claim 14, wherein a shape of the particle is a substantially hexagonal cylinder and a *c*-axis of a crystal is aligned in a direction perpendicular to a hexagonal plane of the substantially hexagonal cylinder.

20 17. The method for forming an oxide film according to claim 14, wherein the plurality of particles are generated by cleavage of the crystal grains included in the target.

25 18. The method for forming an oxide film according to claim 14, wherein the deposition surface is heated during the deposition of the plurality of particles.