

The invention concerns a circuit arrangement for reversing a magnetic field.

Such circuit arrangements are employed for example in magneto-optical recording and playback equipment to reverse the direction of magnetisation in the magnetic layer of a magneto-optical recording medium.

A known magneto-optical recording medium is the magneto-optical disc, in which behind a light-transmissive layer lies a magneto-optical layer, on which information can be recorded and from which data can be read. It is first explained how the information is recorded on a magneto-optical disc.

A laser beam is focussed on the disc and heats the magneto-optical layer to a temperature in the vicinity of the Curie temperature. It is, however, usually sufficient to heat the magneto-optical layer only to approximately its compensation temperature, which is below the Curie temperature. An electromagnet is positioned behind the focal point on the disc and magnetizes the area heated by the laser beam in one direction of magnetization or the other. Since the heated area cools down to below the compensation temperature again once the laser beam is turned off, the magnetic orientation by the electromagnet is retained. It freezes in, so to speak. The individual bits are accordingly stored in domains of different direction of magnetization. One direction of magnetisation of a domain corresponds for example to a domain of logical one, while the opposed direction of magnetisation represents a logical zero.

The Kerr effect is exploited to read the information. The plane of polarisation of a linearly polarised beam

of light is rotated upon reflection at a magnetised mirror by a measurable angle. The plane of polarisation of the reflected beam of light is rotated right or left in accordance with the direction in which the mirror is magnetised. Since, however, the individual domains on the disc act like magnetised mirrors, the plane of polarisation of a scanning beam of light is rotated right or left by a measurable angle in accordance with the direction of magnetisation of the domain just scanned.

From the angle of rotation of the plane of polarisation of the beam of light reflected from the disc, an optical pick-up recognises which bit is present, is a logical ONE or a logical ZERO.

One known way of magnetising the magnet-optical layer in one direction or the other is provided by a circuit arrangement that acts as an electromagnet with a coil behind the magneto-optical disc. The coil must be large enough to allow remagnetisation of the total area covered by the optical pick-up. Depending on the type of recording-and-playback equipment, this area is either a radial or arcuate strip extending from the edge to the centre of the disc. Since the field strength must attain a minimum value over the total strip in order for the strip to be remagnetised, the cross-section of the coil is relatively extensive and its inductivity accordingly relatively high.

The coil in another known approach is secured to the optical pick-up. The coil can for example be wound around the objective lens of the pick-up. Since the coil in this version is guided together with the optical pick-up along the data tracks on the magneto-optical disc by a tracking circuit, a less extensive cross-

section and accordingly a lower inductivity suffice to generate the same minimum field strength, because it is no longer a radial or arcuate strip but only a small and circular for example area with the substantially punctiform laser spot at its centre that is remagnetised in the magneto-optical layer.

From GB-A-2184625 there is known a circuit arrangement for the rapid reversal of a magnetic field.

A series circuit consisting of a first and a second diode, a series circuit consisting of a third and a fourth diode, and a d.c voltage source are connected in parallel to each other. The common connection of the first and the second diodes is connected via a coil to the common connection of the third and fourth diodes. Each of the first to fourth diodes, which are all biassed in the reverse direction to the d.c.voltage source, is shunted by a respective controllable switch. Between the common connection point of the first and third diodes and the d.c. voltage source there is connected a fifth diode, which is biassed in the forward direction to the d.c voltage source. A capacitor is provided in parallel to the d.c.voltage source.

Although this circuit arrangement achieves a quick reversal of the magnetic field of the coil, the time for the reversal of the magnetic field can be further shortened by suitable measures.

Accordingly, the object of the invention is to provide a circuit arrangement according to the introductory part of claim 1, such that a sure and quick reversal of the magnetic field is effected.

The invention achieves this object by means of the

features of claim 1.

Fig.1 to Fig.4 show a first embodiment in various switching states

Fig.5 shows a second embodiment

Fig.6 shows an embodiment of a control circuit for controlling the controllable switch

Fig.7 shows a diagram, in which are plotted the control signals for the controllable switch as well as the current- and voltage- behaviour at the coil versus time.

The invention is now described and explained with reference to Figures 1 to 4.

In Figure 1 there are a series circuit consisting of two diodes D1 and D2, a series circuit consisting of two diodes D3 and D4, a d.c.voltage source U and a capacity C1 lying parallel to each other. The common terminal point A of the diodes D1 and D2 is connected via a coil L with common terminal B of the diodes D3 and D5. The diode D2 is bypassed by a controllable switch S1, the diode D4 is bypassed by a controllable switch S2. The common terminal A of the diodes D1 and D2, of the controllable switch S1 and the coil L is connected with the one terminal of a current sensor SF via a controllable switch S3. The common terminal B of the diodes D3 and D4, of the controllable switch S2 and the coil L is also connected with the one terminal of the current sensor SF via a controllable switch S4, the other terminal of the current sensor being connected with the common connecting point of the diodes D1 and D3, the voltage source U and the capacitor C1. The outputs A1 to A4 of a control circuit S, of which input

E is connected with the output of the current sensor SF, are connected with the control inputs of the controllable switches S1 to S4. The current sensor SF can be constructed e.g. as a threshold detector. For a better understanding the control circuit S is omitted from Figures 1 to 4.

The order of opening and closing of the controllable switches S1 to S4 by the control circuit S for reversal of the magnetic field generated by the coil L, is now explained referring to Figures 1 to 4.

In Figure 1 the controllable switches S1 and S4 are closed, while the controllable switches S2 and S3 are opened. Therefore a current I starts to flow from the positive pole of the voltage source U via the current sensor SF, the controllable switch S4, the coil L and the controllable switch S1 to the negative pole of the DC voltage source U. As soon as this fast increasing current reaches a predetermined threshold, the current sensor SF supplies a signal to the control circuit S, which now causes the controllable switch S4 to be opened. Hence the potential at the connecting point B drops sharply, until finally the diode D4 starts to conduct.

In this switching state, which is shown in Figure 2, the current I further flows in the same direction through the coil L in the loop, which is formed by the coil L, the controllable switch S1 and the diode D4.

For the reversal of the magnetic field the controllable switches S2 and S3 are closed, as shown in Figure 3, the controllable switch S1 however is opened. The voltage at the connecting point A jumps upwardly, such that the current I now flows from the positive pole of the DC

voltage source U via the current sensor SF , the controllable switch $S3$, the coil L and the controllable switch $S2$ to the negative pole of the DC voltage source U . -As soon as the current I reaches the predetermined threshold value, the current sensor SF supplies a signal to the control circuit S , which opens the controllable switch $S2$. Because the voltage at the connecting point A drops suddenly, the diode $D2$ starts to conduct.

In this switching state, shown in Figure 4, the current I further flows in the same direction through the coil L in the loop, which is formed by the coil L , the diode $D2$ and the controllable switch $S2$.

In order to reverse the direction of the magnetic field again, the controllable switch $S2$ is opened, the controllable switches $S1$ and $S4$ closed however. Now the switching state shown in Figure 1 is reached once more.

In order to reverse the direction of the magnetic field for instance cyclically, the switching processes explained with reference to Figures 1 to 4, are repeated by the control circuit S cyclically.

An essential advantage of the invention is that the voltage of the DC voltage source U can be selected very high - up to several hundred volts. Due to the high voltage a very fast reversal of the current and therefore of the magnetic field can be achieved. Despite the high voltage the circuit arrangement according to the invention consumes only little energy, because upon the reversal of the direction of current the coil L feeds the energy stored therein back to the voltage source U or to the capacitor $C1$ connected in parallel.

In Figure 5 a first embodiment of the invention is shown, that differs from the circuit arrangement of Figure 1 in that a diode D5 is provided in a connecting branch of the current sensor. This diode D5 prevents the current flowing in the wrong direction through the current sensor SF.

The embodiment shown in Figure 6, of a control circuit for controlling the controllable switches S1 to S4 will be first described and following it will be explained referring to the pulse diagram shown in Figure.7.

As mentioned already, the invention is suitable for the reversal of magnetisation of the magnetic layer of a magneto-optical recording medium.

The digital data signal DS to be recorded on a magneto-optical disc is supplied to the data input of a shift register SR, which is clocked by a clock generator G. The first output T0 of the shift register SR, at which the undelayed data signal can be derived, is connected to the first input of an AND-gate U1 and via a first inverter I1 to the first input of an AND-gate U2. The second output T1 of the shift register SR, at which the data signal delayed by one clock period can be derived, is connected to the second input of the AND-gate U2 and via an inverter I2 to the second input of the AND-gate U1. The output of the AND-gate U1 is connected to the input of an inverter I3 and via a capacitor C2 to the set-input of an RS-flip-flop F1. The output of the AND-gate U2 is connected to the input of an inverter I4 and via a capacitor C3 with the set-input of an RS-flip-flop F2. The set-inputs of both RS-flip-flops F1 and F2 lie at reference potential due to a respective circuit consisting of a resistor R1 or R2 and a diode D6 or D7.

The output of the current sensor SF is connected with the reset-input of both RS-flip-flops F1 and F2. These are derivable at the output of the inverter I3 the control signal for the controllable switch S1, at the output of the inverter I4 the control signal for the controllable switch S2, at the Q-output of the RS-flip-flop F1 the control signal for the controllable switch S3, and finally at the Q-output of the RS-flip-flop F2 the control signal for the controllable switch S4.

The differentiating member consisting of the resistor R1 and the capacitor C2 serves to shorten the pulses at the output of the AND-gate U1. Likewise the pulses at the output of the AND-gate U2 are shortened by the differentiating member consisting of the resistor R2 and the capacitor C2. The diodes D6 and D7 prevent the differentiating of the falling flanks too, if the signal at the output of both AND-gate U1 and U2 changes from "HIGH" to "LOW". The shortening of the pulses caused by both differentiating members at the outputs of both AND-gates U1 and U2 is necessary to make sure that the set-inputs of both RS-flip-flops F1 and F2 are always at "LOW", when the RS-flip-flops receive a reset-pulse from the current sensor SF.

The pulse diagram of Figure 7 shows the clock G for the shift register SR, for the undelayed data signal DS and for the data signal TS which is delayed by one clock period. The direction of the current I which flows through the coil L, is to be reversed at each flank in the data signal DS. The AND-gate U1 supplies at each rising flank of the data signal DS a pulse, which, after inversion by the inverter I3, opens the controllable switch S1 for the duration of the pulse. Because at the same time the RS-flip-flop F1 is set by the pulse at the output of the AND-gate U1, the controllable switch

S3 is closed. However as soon as the magnitude of current I through the coil L reaches the predetermined threshold value, the RS-flip-flop $F1$ will be reset by the current sensor SF and hereby the controllable switch $S3$ will be opened.

At each falling flank in the data signal DS the AND-gate $U2$ supplies a pulse, which, inverted by the inverter $I4$, opens the controllable switch $S2$ for the duration of the pulse. The controllable switch $S4$ is closed at the same time, because the RS-flip-flop $F2$ is set by the pulse at the output of the AND-gate $U2$. If the value of the current I through the coil L reaches the predetermined threshold value, the current sensor SF resets the RS-flip-flop $F2$ in order re-open the controllable switch $S4$. The voltage $U2$ at the coil L increases in pulses at each rising flank of the data signal DS , at a falling flank of the data signal DS however it takes the form of a negative pulse. The current I through the coil L changes in magnitude and direction depending on the data signal DS : At a rising flank in the data signal DS the current I , which flows through the coil L , rises quickly from the lower threshold value to the upper, while at a falling flank it falls just as quickly from the upper threshold value to the same lower threshold value. The current passing the current sensor SF changes only its magnitude in dependence on the data signal DS , its direction however remains the same. At each flank in the data signal DS the current rises quickly to the threshold set at the current sensor SF , which is a threshold detector, and then falls suddenly to the value zero.

With magneto-optical recording and playback equipment the invention offers the advantage, that data already recorded on the magneto-optical record can be directly

overwritten. Contrasted to this, with known magneto-optical recording and playback equipment the old data are first erased, before new data are recorded.

In order to achieve this the magneto-optical layer is heated up by the laser to the compensation temperature at those locations where new data are to be stored. Thus these locations are magnetised in one direction. The record is initialised, which is the term of the art for this procedure. Subsequently the direction of the magnetic field generated in the coil is again reversed.

For the recording of the new data the laser power is switched between a low and a high value depending on the bit to be stored. If at the previously erased location e.g a logic ZERO is stored, then the laser operates with the low power, in order not to reach the compensating temperature. For recording of a logic ONE however the laser heats the location to be recorded up to the compensation temperature, in order to allow re-magnetising of this location by the coil. In this complicated way data on the magneto-optical record are first erased, before the new data are subsequently recorded.

The invention is not only suited for magneto-optical equipment, but also for other magnetic recording equipment.

Claims

1. A circuit arrangement for the reversal of a magnetic field, in which a series circuit consisting of a first and a second diode (D1,D2), a series circuit consisting of a third and fourth diodes (D3,D4) and a DC voltage source (U) are connected in parallel, in which the common connection (A) of the first and second diodes (D1,D2) is connected via a coil (L) with the common connection (B) of the third and fourth diodes (D3,D4), in which the second diode (D2) is shunted by a first controllable switch (S1) and the fourth diode (D4) is shunted by a second controllable switch (S2), in which, by means of a third controllable switch (S3), the first connection point (A) of the coil (L) and, via a fourth controllable switch (S4), the other connection point (B) are connected to each other and in which all diodes (D1,D2,D3,D4), are biased in the reverse direction to the DC voltage source (U), characterised in that between the common connection point of the first and third diodes (D1,D3), and the common connection point of the third and fourth controllable switches (S3,S4), there is connected a current sensor (SF) the output of which is connected to the input (E) of a control circuit (S), the outputs (A1,A2,A3,A4) of which are connected to the control inputs of the controllable switches (S1,S2,S3,S4), and by which the switches are controllable such that in a first process step the first and the fourth controllable switches (S1,S4) are closed while the second and third controllable switches (S2,S3) are open, that in a second process step the fourth controllable switch (S4) is open, when the magnitude of the current (I) through the coil (L) exceeds a predetermined threshold value, that in a third process step for reversal of the current in the coil (L) the first controllable switch (S1) is open and the second



and third controllable switches (S2,S3) in contrast are closed, that in a fourth process step the third controllable switch (S3) is open when the magnitude of the current (I) through the coil (L) lies below the predetermined threshold value, and that for reversal of the current (I) through the coil (L) in a fifth process step the second controllable switch (S2) is open and the first and the fourth controllable switches (S1,S4) in contrast are closed.

2. A circuit arrangement according to claim 1, characterised in that for the cyclical reversal of the current (I) through the coil (L) the process steps two to five are cyclically repeated by the control circuit (S).

3. A circuit arrangement according to claim 1 or 2, characterised in that a first capacitor (C1) is connected in parallel to the DC voltage source (U).

4. A circuit arrangement according to claim 1,2 or 3, characterised in that in a connection branch of the current sensor (SF) there is connected a fifth diode (D5) which is biased in the forward direction for the DC voltage source (U).

5. A circuit arrangement according to claim 1,2,3 or 4, characterised in that a threshold value detector is provided as a current sensor (SF).

6. A circuit arrangement according to claim 1,2,3,4 or 5, characterised in that a digital signal (DS) is connected to the input of a shift register (SR), which is clocked by a clock generator (G), that the signals at the output (T0,T1) of the shift register and the output signal of the current sensor (SF) are logically combined



in a logic circuit and that at the outputs of the logic circuit there are derivable the control signals for the controllable switches (S1,S2,S3,S4).

7. A circuit arrangement according to claim 6, characterised in that the first output (T0) of the shift register (SR) is connected to the first input of a first AND-gate (U1) and via a first inverter (I1) to the first input of a second AND-gate (U2), that the second output (T1) of the shift register (SR) is connected to the second input of the second AND-gate (U2) and via a second inverter (I2) to the second input of the first AND-gate (U1), that the output of the first AND-gate (U1) is connected to the input of a third inverter (I3) and via a second capacitor (C2) to the set input of a first RS-flip-flop (F1), that the output of the second AND-gate (U2) is connected to the input of a fourth inverter (I4) and via a third capacitor (C3) to the set input of a second RS-flip-flop (F2), that the said input of the first RS-flip-flop (F1) is connected to reference potential via a parallel circuit consisting of a first resistor (R1) and a sixth diode (D6), that the said input of the second RS-flip-flop (F2) is connected to reference potential via a parallel circuit consisting of a second resistor (R2) and a seventh diode (D7), that the output of the current sensor (SF) is connected to the reset input of the first and second RS-flip-flops (F1,F2), that the output of the third inverter (I3) is connected to the control input of the first controllable switch (S1), that the output of the fourth inverter (I4) is connected to the control input of the second controllable switch (S2) that the Q-output of the first RS-flip-flop is connected to the control input of the third controllable switch (S3) and that the Q-output of the second RS-flip-flop (F2) is connected to the control input of the fourth controllable switch (S4).

