

Description

The invention relates to a video processor system for real-time processing of video samples and comprising a plurality of processor modules that have processor elements operating in time-parallel fashion and having their inputs and outputs interconnected by a crossbar switch which interfaces to further circuitry external to said processor module. The video signals supplied can be formed by component signals (R, G, B or Y, U, V), by combined signals as defined in the PAL or NTSC standard, or by unstandardized signals, such as are supplied, for example, by a VCR apparatus or a video disk. The processing result should be suitable for driving, for example, an imaging unit, such as a CRT or an LCD, or for being recorded on a magnetic tape. In the video processor system, the video signal samples should undergo diverse operations. Said operations may relate, for example, to filtering, correlating, and repositioning of information both within a video line and between video lines within a field or between fields within a frame.

The article entitled "Warp Architecture and Implementation" by M. Annaratone et al. from the "13th Annual symposium on computer architecture, June 1986, Tokyo (Japan)" discloses a Systolic array computer (Warp)" in which a row of processor units is present and each processor unit is provided with at least one arithmetic and logic processor element and at least one memory processor element, a crossbar switch, moreover, being present to which, via a buffer circuit, input signals for a processor unit and output signals from the processor elements belonging to the respective processor unit can be fed and from which input signals for the processor elements belonging to said processor unit and output signals from said processor unit can be obtained. The data which are processed in this parallel computer system in the said publication are stored with the aid of an I/O unit in a buffer and are further processed therefrom. The system therefore does not function on a real-time basis. The system is, moreover, not adapted for processing video signals specifically, it being necessary to take into account not only the presence of specific video line memory means and field memory means, but also the above-mentioned fixed relationship between the clock signals at all levels in the hierarchy and those which are necessary for sampling the video signals. The architecture of the video processor system according to the invention is, furthermore, not based specifically on a row of processor elements; the video processor modules may be connected in a series, a parallel and/or a fed-back configuration, which increases the flexibility of the system.

The object of the present invention is *inter alia* to provide an architecture for a video processor system as mentioned above which makes said system flexible and readily adaptable to the desired operations to be carried out on the video signals; precisely because the video signals have to be processed on a real-time basis, said operations will often have to be carried out in parallel.

The invention is set out in claims 1 and 2.

The fact that the signals derived in the video processor unit are suitable for driving an imaging unit implies in this case that said signals are able to drive an imaging unit directly and can also first be subjected to yet a further signal processing before driving an imaging unit, or may even first be recorded on a magnetic tape or other storage medium in order to be able to drive an imaging unit later.

The video processor system according to the invention has an architectural hierarchy in three levels, viz. video processor units, processor modules and processor elements. As a result of this, a modular generalized framework becomes possible in which a multiplicity of operations can be executed simultaneously, the fixed relationship between sampling frequency and clock frequency at all levels in the video processor system making data processing on a real-time basis possible without additional buffering. If several video processor units are present, they can be connected in a series, a parallel and/or a fed-back configuration. Each video processor unit may be provided with several, preferably three, processor modules and is preferably constructed as a separate integrated circuit. Each processor module may comprise several, for example three, arithmetic and/or logic processor elements and several, for example two, memory processor elements, whilst a gate processor element may furthermore be present in addition at the input or the output of the processor module. Each processor module is, moreover, provided with a crossbar switch which can be formed, for example, by the input circuits of the processor elements.

FURTHER ASPECTS OF THE INVENTION

In a particular embodiment, the memory capacity of the memory means in the processor elements is sufficient for storing the data relating to at least one video line in order to be able to carry out, for example, correlation operations between consecutive video lines in the system, one or more separate field memories, moreover, being present which are in communication with one or more video processor units. Each processor element has its own control element in which the program memory for the respective processor element is accommodated. Stored in said memory is a cycle of

branch-free instructions, for example a maximum of sixteen, with the aid of which operations can be carried out in the respective processor element. The crossbar switch is controlled from the program memories belonging to a processor module. If the program memory is formed by a RAM memory, this is loaded in an initiation process; with the exception of the initiation bus necessary therefore no further control bus is present in the video processor units, apart from a reset signal conductor which may, however, be assigned to the initiation bus. As a result of the individual programability, the processor elements may have mutually different program lengths which further increases the flexibility.

Conflicts may arise as a result of the nature of the crossbar switch and the programming of the various processor elements; if, for example, information which is intended for one and the same input of a processor element appears at the output of two processor elements at the same time, such a conflict is produced. An effective solution for such conflicts is given in US Patent 4,521,874 in which a buffer register is provided at each of the switch points of a crossbar switch. This solution is relatively expensive and takes up a large chip surface. In a particular embodiment, each processor module comprises as many so-called silo registers as the crossbar switch has outputs; the data is written into said silo registers in a fixed sequence but is read out in a sequence determined by the program in the program memory of the respective processor element. As a result of this, the solution is cheaper than that of the abovementioned US patent is avoided, although flexibility is to some extent lost.

In each of the program memories, a fixed cycle of instructions is always generated; the frequency with which this cycle is repeated again bears a fixed relationship to the frequency of the video signal stream. A reset signal can achieve the result that the first instructions of the respective cycles of all the program memories are generated at one and the same instant. The cyclic programs ensure, provided, of course, sufficient video processor units are present, that the desired operations can be carried out on each stream of video signals on a real-time basis. In addition, the communication between the video processor units is relatively simple because a synchronous control can already be determined during programming. Although they are in different processor modules or different video processor units, the communication between all the processor elements proceeds under the control of the said cyclic programs.

The architecture described here makes programming relatively simple, while the connected processor elements can be efficiently utilized.

The present invention further relates to an imaging system provided with means for receiving frame-sequential and line-sequential image information from a source device, a video processor system according to the invention and means for effecting the imaging of an image. The source device may in this case be formed by a video signal receiver, a video recorder or a video disk. The present invention further relates, in addition, to an image storage system provided with means for receiving frame-sequential and line sequential image information from a source device, a video processor system according to the invention and means for effecting the image storage. In principle, the same source devices can be used here as for the abovementioned imaging system.

Finally, the invention furthermore relates to the integrated circuit provided with a video processor unit as described above.

BRIEF DESCRIPTION OF THE FIGURES

The invention will now be explained in more detail with reference to the accompanying drawings, in which:

Figure 1 shows an example of a video processor system according to the invention;

Figure 2 shows an example of the structure of one single video processor unit;

Figure 3 shows a possible structure of one single processor module;

Figure 4 shows an embodiment of an arithmetic and logic processor element of a processor module;

Figure 5 shows an embodiment of a silo register in greater detail;

Figure 6 shows an embodiment of a memory processor element of a processor module;

Figure 7 shows an embodiment of a gate processor element of a processor module; and

Figure 8 shows the signals on the initiation bus for loading the program memories in the separate processor elements.

The invention is in no way restricted to the exemplary embodiment described with reference to the drawings; this preferred embodiment serves only to illustrate the invention.

DESCRIPTION OF A PREFERRED EMBODIMENT

Figure 1 gives an example of a video processor system according to the invention. Analog video signals which are formed in a known manner by a video camera, video cassette recorder, video disk player or in some other manner appear on the input 2. An A/D converter 4 converts said video signals at a sampling frequency determined by clock signals into a train of digital video signal

samples which are subsequently distributed by a demultiplexer 6 over two outputs according to a pre-determined distribution. As a result, each sub-stream of video signal samples can be processed at a lower frequency than that at which the complete stream of video signal samples is fed in so that signals can be processed which could otherwise probably not be processed as a result of an excessively high sampling frequency. Connected to the uppermost output of the demultiplexer 6 is a video processor unit 8 which executes a first operation. The results are fed via two outputs to a video processor unit 10 and, via one of these two, in addition to a video processor unit 12. The results from the video processor unit 12 are also processed in the video processor unit 10. The output of the video processor unit 10 is connected to a video processor unit 14. The latter is in this case bidirectionally in communication with a field memory 16; this is, for example, a CCD memory. Operation results appear, moreover, on two outputs of the video processor unit 14. The results from the lowermost output are fed back therefrom to the video processor unit 8, as a result of which a recursive operation becomes possible. The uppermost output of the video processor unit 14 is connected to a video processor unit 18. The lowermost output of the demultiplexer 6 is connected to a video processor unit 20 which is in communication with a field memory 20 bidirectionally. The video processor units 18 and 20 are connected to each other bidirectionally. In this manner, the two parts of the input signal can be processed in different manners, a recorelation being possible as a result of this latter mutual connection. D/A converters 24 and 26 respectively are connected to the video processor units 18 and 20 at the outputs. The output signals thereof may, for example, be used to drive a cathoderay tube (not shown). Two further sub-systems 28 and 30 provide the general control. The subsystem 28 forms a clock device in which the clock signals are generated with which the A/D converter 4, the demultiplexer 6, the video processor units 8, 10, 12, 14, 18 and 20, the field memories 16 and 22 and the D/A converters 24 and 26 are controlled so that all the operations may take place in a mutually fixed time relationship. The basic clock frequency of the subsystem 28 and, consequently, the clock signals derived therefrom for controlling the video processor system, including that for sampling the video signals fed in bear in this case, in addition, a fixed relationship to the frequency with which video lines and, consequently, the respective fields occur. The subsystem 30 forms a system control device and can, for example, execute reprogramming operations on the respective video processor units, for example for adjusting filter coefficients. The subsystems 28 and

30 are connected to each other bidirectionally. The subsystem 30 has at the same time the facility (not shown in the figure) for receiving signals from outside the system, for example, to initiate the said reprogramming. For the sake of simplicity, the further connections of the subsystems 28 and 30 are not depicted.

Fig. 2 gives an example of the structure of one single video processor unit. Such a video processor unit is realised as one single integrated circuit (chip) in CMOS technology, the processor modules surrounded by a broken line being controlled by a 27MHz clock signal. Within the video processor unit there are three processor modules 32, 34 and 36 which are directly connected to each other bidirectionally. Although this will also be advantageous with a larger number of processor modules it will not always be realisable because, as the number of processor modules increases, the number of interconnections rapidly becomes larger and a correspondingly larger chip surface is taken up. In the embodiment shown, each processor module has 5 input and 5 output channels of 12 bits each. Of these, one input and output channel in each case provides the contact with other possible video processor units or other types of unit. The chip depicted in Figure 2 further comprises 3 data gates each with a demultiplexer 38, 40 and 42 respectively, and a multiplexer 44, 46 and 48 respectively, while, finally a chip initiation control circuit 50 and a clock circuit 52 are also present. As already stated, the processor modules operate at a frequency of 27 MHz; in the clock circuit 52, this frequency, which bears a fixed relationship to the sampling frequency of the video signals, is derived from a 54 MHz clock signal fed to the chip. Said clock signal is used here to control the multiplexers and demultiplexers in the data gates and, specifically, to convert the 12-bit/27 MHz data provided by the processor modules into 6-bit/54 MHz data and, vice versa, to convert 6-bit/54 Mc/s data into 12-bit 27 MHz data to be fed to the processor modules. The contact with other possible video processor units and other types of units then proceeds via 6-bit/54MHz channels. This provision, which is obviously optional, has the advantage that the number of external connections to the chip are severely limited. The 27MHz clock signal is derived from the 54MHz clock signal in the clock circuit 52 with the aid of a scale-of-two circuit, the phase of the 27MHz clock signal being monitored by a reset signal R which is fed not only to all the processor modules on the chip, but also to the clock circuit 52. The chip initiation control circuit 50 has a clock and serial data input and a clock and serial data output connected to each processor module. Said clock and serial data, which is fed to the processor modules via the circuit 50, is indicated by IC. The

chip initiation control circuit 50 is furthermore provided, in a serpentine configuration, with an 8-bit serial chip address CA and a chip address valid signal V; the addressing of the initiation data will be dealt with below. Apart from the power connections P, 3 x 6 data input connections, 1 reset signal connection, 2 IC connections and 3 connections for the chip addressing for the initiation data are present on the chip; the chip therefore contains 43 connection pins, apart from the power connections.

DESCRIPTION OF A PROCESSOR MODULE

Figure 3 depicts the structure of one single processor module. Here this comprises three identical processor elements (MILL) 54, 56 and 58 for performing arithmetic and logic operations, two identical processor elements having a memory function 60 and 62 and an output gate processor element 64. Each of these elements is connected to an input circuit 66, 68, 70, 72, 74 and 76 respectively. These input circuits together form a crossbar switch. The MILL processor elements comprise an arithmetic and logic element (ALE) 78, 80 and 82 respectively, and a control element (CTRM) 84, 86 and 88 respectively. The memory processor elements comprise a memory element (ME) 90 and 92 respectively and a control element (CTRS) 94 and 96 respectively. The output gate processor element comprises an output data buffer 98 and a control element (CTRG) 100. The processor module input signals are fed to the crossbar switch via the five 12-bit channels 102 and the output signals from the processor elements belonging to the respective processor module via the five 12-bit channels 104. Processor module output signals are obtained from the crossbar switch via five 2-bit channels 106. Furthermore, a connection 108 is indicated for the reset signal R to the control elements 84, 86, 88, 94, 96 and 100, and also the two-wire clock and serial data (IC) connection 110 to all said control elements. It will furthermore be clear that, instead of the output gate processor element 64, an input gate processor element with the same function can also be used; for the diverse processor modules connected to each other, a buffer is present in both cases between every two processor modules. The various input circuits are controlled from the respective control elements. The distribution of the data stream over the respective processor elements, processor modules and video processor units, therefore, is controlled solely by the control elements.

Figure 4 shows to the right of the broken line the block diagram of an arithmetic and logic element (ALE) and to the left of the broken line the associated control element (CTRM). The ALE comprises two 12-bit inputs with a silo register 112, 114

respectively, the output of which silo registers is connected to shift units (SHA, SHB) 116 and 118 respectively (formed, for example, by "barrel shifters"). The output of said shift units is connected via multiplexers 120 and 122 respectively to the P and Q inputs respectively of a ALU 124. The CTRM comprises a program memory 126, an initiation circuit 128, an address multiplexer 130, a program address counter 132 and an OR gate 134. The silo registers have a memory function for 32 words, writing taking place in a fixed sequence, while reading out takes place in a sequence determined by the program memory 126. The write address is generated by a 5-bit counter belonging to the silo registers, while the read address is obtained by subtracting a relative read address (RAD) from the write address determined by the program memory. In this manner, delays are realised by the silo registers over RAD clock periods, RAD being a sign-free integer which may change every clock cycle. The silo registers can be written in and read out at the same time, but not at the same address, so that $0 < \text{RAD} \leq 31$. The 12-bit data words originating from the silo registers may be subjected to a shift operation determined by the program memory in the shift units 116 and 118. 12 logic shift operations to the right, 12 logic shift operations to the left and 12 arithmetic shift operations to the right are, for example, possible; the 6-bit shift control signals may be fed in for this purpose by the program memory. The 12-bit data words originating from the shift units are fed via multiplexers 120 and 122 to the ALU 124, which delivers the ALE output signal. The ALU 124 is controlled from the program memory and, to be specific, via the I input, and performs the usual arithmetic and logic operations. The multiplexers 120 and 122 offer the possibility of replacing a data word by a constant from the program memory 126. This 12-bit constant can then, for example, be formed by the 5 bits which are otherwise used for the RAD delay, and the 6 bits which are otherwise used as shift control signal, plus 1 additional bit. The multiplexers 120 and 122 are controlled by a 1-bit control signal from the program memory. The program memory has capacity for 16 words of 55 bits, the 4-bit addresses being fed in via the address multiplexer 130. The program length is adjustable up to 16 steps at the most by making use of the reset facility of the program address counter 132; the reset signal delivered by the program memory is fed to said counter via the OR gate 134. The program counter may also be reset by the external reset signal R. Via the chip initiation control circuit 50, initiation and reprogramming data can be received which, for each data unit, are made up of a program memory address IA and initiation data ID. Said data units are fed serially

over one wire of the IC connection, clock signals being delivered via the other wire of said connection in order to specify both the beginning and the end of the data units, and also the individual bits of said data units. In the initiation circuit 128, the serial data units are converted to parallel form and, to be specific, into a 4-bit program memory address IA and 41-bit initiation data ID. These data are fed to the program memory 126. In this process, the program memory address flows via the address multiplexer 130. When a data unit has been received by the initiation circuit 128, the multiplexer 130 is activated so that the program memory address IA originating from said initiation circuit is transmitted, while a write signal W/R is emitted at the same time so that the data ID can be written into the program memory. The addressing of the initiation data is dealt with further below. Finally, attention should also be drawn to the fact that the program memory delivers the control signal SC1 for the crossbar switch.

Figure 5 shows in more detail an embodiment of a silo register; said register comprises a silo memory 136, an address counter 138 and a subtraction circuit 140. The counter 138 delivers the consecutive write addresses for the 12-bit words fed to the silo register via the conductor 142. The write address with the relative read address RAD subtracted in the subtraction circuit 140 forms the read address for the 12-bit words to be read out of the silo register 136 via the conductor 144. Said relative read address RAD also determines the time delay between writing in and reading out the data words from the silo register.

Figure 6 shows, to the right of the broken line, the block diagram of a memory element ME and, to the left of the broken line, the associated control element CTRS. The ME comprises two 12-bit inputs A and B with a silo register 146 and 148 respectively. The input A forms an address input and the input B a data input. The output of the address silo register 146 is fed to a summing circuit 150, which makes a so-called memory pagination possible. The summing is executed on the 9 least significant bits of the output of the address silo register 146 and a 9-bit constant from the program memory 152 of the CTRS. The 9-bit memory address thus obtained is fed via an address multiplexer 154 to a data memory 156. This memory provides capacity for 512 12-bit data words which are fed thereto via a data multiplexer 158 from the data silo register 148. Said capacity is chosen in a manner such that it is possible for two memory processor elements, that is to say two data memories, per processor module to suffice to be able to store the 12-bit words of at least one video line together in the two data memories. For this purpose, the video signal sampling frequency

has to be equal to half the 27MHz clock frequency of the processor modules. The data memory 156 is also able, moreover, to fulfill the function of "search table". For this purpose, this memory may be filled via the initiation bus. The output of the data memory 156 also forms the output of a respective memory processor element. The silo registers 146 and 148 are constructed in the same manner and function in the same manner as the silo registers 112 and 114 described above with reference to Figures 4 and 5. The CTRS is in principle also made up in the same manner as the CTRM in Figure 4. Apart from the program memory 152 already mentioned, the CTRS comprises an initiation circuit 160, an address multiplexer 162, a program address counter 164 and an OR gate 166. The switches 162, 164 and 166 are identical to, and function in the same manner as, the address multiplexer 130, the program address counter 132 and the OR gate 134 in Figure 4. The program memory 152 provides capacity for 16 words of 29 bits. The initiation circuit 160 provides the loading of the program memory 152 as well as the loading of the data memory 156 which is then functioning as search table. The data units which, just as in the case of the initiation circuit 128 and Figure 4, are emitted in parallel by the circuit 160, are composed of 33-bit words IAD. To write into the program memory 152, use is made of 4 bits there for the addressing, while 29-bit words are written in and, to be specific, in the same manner as was the case for the program memory 126 in Figure 4. The addressing of the memory locations for the 29-bit words in the program memory 152 proceeds via the address multiplexer 162. To write 156 words into the data memory, 9 of the 33 bits are used for addressing the data memory 156 which proceeds via the multiplexer 154, while 12 of the 33 bits form the data words which are fed to the data memory 156 via the multiplexer 158. The control signal C' emitted via the initiation circuit 160 indicates that data words from the initiation circuit 160 should be written into the data memory 156; the multiplexers 154 and 158 are controlled with the aid of this signal. Finally, the ME also comprises a multiplexer 168 which transmits either a read-out signal from the program memory 152 or a write-in signal C for loading data words from the initiation circuit 160. This multiplexer, too, is controlled by the control signal C'. The program memory furthermore also delivers a control signal SC2 for the crossbar switch.

Figure 7 shows an embodiment of the gate processor element 64 from Figure 3. A buffer circuit 170 is present for each of the 5 input/output signals, each buffer circuit having its own control circuit CTRGi ($i = 1, \dots, 5$). The 5 buffer circuits together form the output data buffer 98 (Figure 3),

the 5 associated control circuits forming the control element (CTRG) 100 (Figure 3). The buffer circuits are formed by the silo registers SILOi (i = 1,...,5). These silo registers are identical to the silo registers 112, 114, 146 and 148 described with reference to Figures 4, 5 and 6. The control circuits are identical to, and function in the same manner as, the control element CTRM described above with reference to Figure 4. In Figure 7 only one of these control circuits is depicted in detail; this comprises a program memory 172, an initiation circuit 174, an address multiplexer 176, a program address counter 178 and an OR gate 180. The program memory 172 provides capacity for 16 words of 10 bits. These 10-bit words ID' are written into the program memory 172 after addressing with the aid of the 4 address bits IA' via the address multiplexer 176. The bits IA' and ID' are supplied in parallel by the initiation circuit 174 after having been fed bit-serially thereto. The 5 parts CTRGi and SILOi of the gate processor element have a common bit-serial bus IC and a common reset signal conductor R. The program memory in each of these 5 parts furthermore also supplies a control signal SCG for the crossbar switch.

To initiate the diverse program memories and the data memory of the processor memory elements (when these are used as search table) initiation data are sent, as already stated, via the two-wire IC bus. The initiation data comprises an indication of the start of the initiation data, address information, a data word and an indication of the end of the message. The information is transferred via a special serial data line and an associated clock line. In Figure 8, the signal-free state on the initiation bus is indicated by a low level on both the data line a and the clock line b. The start St of the initiation data is indicated by the appearance of the clock pulses; the end E of the initiation data is indicated by the disappearance of the clock pulses over at least one clock period. The header of the initiation data itself contains diverse addresses. The address at the lowest level is the memory address GA within a processor element, this is followed by the address GP of a processor element within a video processor unit and finally, at the highest level, the address GV of a video processor unit. The memory addresses GA within a processor element are fed via the multiplexers 130 (Figure 4), 154 and 162 (Figure 6) and 176 (Figure 7) to the respective memories. The address GP of the processor elements of the common processor modules within a video processor unit is compared with the addresses introduced by the hardware in the respective initiation circuits, and if the data word DW matches the memory address GA, is transmitted by the respective initiation circuit in parallel form to the respective program memory. If several

video processor units, that is to say, several chips, are present, the various chip addresses CA are introduced via a serpentine line in a first initiation phase, as a result of which each chip has become identifiable. If the entrained CA address is that for the respective chip, this is indicated with the aid of the chip address valid signal V. The serpentine line is composed of series-connected shift registers which are present in the initiation control circuit 50 of each video processor unit. In the second initiation phase, the address GV of a respective video processor unit is compared with the chip address CA introduced via the serpentine line, and in the event of matching, the data word DW is transmitted together with the addresses GA and GP as IC message by the initiation control circuit 50.

Claims

1. A video processor system for real-time processing of video samples and comprising a video processor unit consisting of a plurality of processor modules (32, 34, 36), each module comprising processor elements (54-62) operating in time-parallel fashion and having their inputs and outputs interconnected by a crossbar switch which interfaces to further circuitry external to said processor module, characterized in that said processor elements consist of at least two ALU elements (54, 56, 58) and at least one memory processor element (60, 62) with address processing capability, in that said crossbar switch comprises a first data path (104) consisting of a plurality of channels, each channel exclusively connected to a multibit wide output of a respective one of the processor elements of the processor module in question, and second data path (102), consisting of a plurality of channels having a combined width equal to at least the combined width of said first channels and representing input channels of the processor module in question, in that all processor elements of each processor module have all their inputs selectively connectable to any of said first and second data paths and having each input provided with a silo register, said silo register having time-sequential writing and random access reading capability, said crossbar being provided with either an output gate processor element (64) or an input gate processor element, with associated data buffer (98) for interfacing between any two interconnected processor modules, in that each said processor element (54-62, 64) has a local control element with a program memory accommodating a multi-instruction program cycle, (84-100), and in that said video processor system has a clock (52) for driving



the 5 associated control circuits forming the control element (CTRG) 100 (Figure 3). The buffer circuits are formed by the silo registers SILO_i ($i = 1, \dots, 5$). These silo registers are identical to the silo registers 112, 114, 146 and 148 described with reference to Figures 4, 5 and 6. The control circuits are identical to, and function in the same manner as, the control element CTRM described above with reference to Figure 4. In Figure 7 only one of these control circuits is depicted in detail; this comprises a program memory 172, an initiation circuit 174, an address multiplexer 176, a program address counter 178 and an OR gate 180. The program memory 172 provides capacity for 16 words of 10 bits. These 10-bit words ID' are written into the program memory 172 after addressing with the aid of the 4 address bits IA' via the address multiplexer 176. The bits IA' and ID' are supplied in parallel by the initiation circuit 174 after having been fed bit-serially thereto. The 5 parts CTRG_i and SILO_i of the gate processor element have a common bit-serial bus IC and a common reset signal conductor R. The program memory in each of these 5 parts furthermore also supplies a control signal SCG for the crossbar switch.

To initiate the diverse program memories and the data memory of the processor memory elements (when these are used as search table) initiation data are sent, as already stated, via the two-wire IC bus. The initiation data comprises an indication of the start of the initiation data, address information, a data word and an indication of the end of the message. The information is transferred via a special serial data line and an associated clock line. In Figure 8, the signal-free state on the initiation bus is indicated by a low level on both the data line a and the clock line b. The start St of the initiation data is indicated by the appearance of the clock pulses; the end E of the initiation data is indicated by the disappearance of the clock pulses over at least one clock period. The header of the initiation data itself contains diverse addresses. The address at the lowest level is the memory address GA within a processor element, this is followed by the address GP of a processor element within a video processor unit and finally, at the highest level, the address GV of a video processor unit. The memory addresses GA within a processor element are fed via the multiplexers 130 (Figure 4), 154 and 162 (Figure 6) and 176 (Figure 7) to the respective memories. The address GP of the processor elements of the common processor modules within a video processor unit is compared with the addresses introduced by the hardware in the respective initiation circuits, and if the data word DW matches the memory address GA, is transmitted by the respective initiation circuit in parallel form to the respective program memory. If several

video processor units, that is to say, several chips, are present, the various chip addresses CA are introduced via a serpentine line in a first initiation phase, as a result of which each chip has become identifiable. If the entrained CA address is that for the respective chip, this is indicated with the aid of the chip address valid signal V. The serpentine line is composed of series-connected shift registers which are present in the initiation control circuit 50 of each video processor unit. In the second initiation phase, the address GV of a respective video processor unit is compared with the chip address CA introduced via the serpentine line, and in the event of matching, the data word DW is transmitted together with the addresses GA and GP as IC message by the initiation control circuit 50.

Claims

1. A video processor system for real-time processing of video samples and comprising a video processor unit consisting of a plurality of processor modules (32, 34, 36), each module comprising processor elements (54-62) operating in time-parallel fashion and having their inputs and outputs interconnected by a crossbar switch which interfaces to further circuitry external to said processor module, characterized in that said processor elements consist of at least two ALU elements (54, 56, 58) and at least one memory processor element (60, 62) with address processing capability, in that said crossbar switch comprises a first data path (104) consisting of a plurality of channels, each channel exclusively connected to a multibit wide output of a respective one of the processor elements of the processor module in question, and second data path (102), consisting of a plurality of channels having a combined width equal to at least the combined width of said first channels and representing input channels of the processor module in question, in that all processor elements of each processor module have all their inputs selectively connectable to any of said first and second data paths and having each input provided with a silo register, said silo register having time-sequential writing and random access reading capability, said crossbar being provided with either an output gate processor element (64) or an input gate processor element, with associated data buffer (98) for interfacing between any two interconnected processor modules, in that each said processor element (54-62, 64) has a local control element with a program memory accommodating a multi-instruction program cycle, (84-100), and in that said video processor system has a clock (52) for driving



the video processing modules at a frequency that has a fixed relation to the recurrency of the video samples received.

2. A video processor system comprising at least two interconnected video processor units as claimed in Claim 1, that each comprise at least two video processor modules. 5
3. A video processor system as claimed in Claim 2, and comprising at least one field memory interconnected to at least one video processor unit. 10
4. A video processor system as claimed in Claim 2 or 3, each video processor unit comprising multiplex/demultiplex circuitry (38, 40, 42, 44, 46, 48) for external interfacing at a smaller bit width than the interface between the various video processor modules of the video processor unit in question. 15 20
5. A video processor system as claimed in any of Claims 1 to 4, wherein any video processor module has at least three ALU elements and at least two memory processor elements with address processing capability. 25
6. A video processor system as claimed in any one of Claims 1 to 5, wherein each processor element of a video processor module is provided with a uniform input circuit, and said input circuits collectively constitute said cross-bar switch. 30
7. A video processor system as claimed in any of Claims 1 to 6 wherein said program memories are RAMs and each video processor module has an initiation bus for loading the RAMs of its video processor modules. 35 40
8. A video processor system as claimed in Claim 7, wherein said bus is single-channel.
9. A video processor system as claimed in Claim 7 or 8, wherein said memory processor elements allow loading of their data memory via said initiation bus. 45
10. A video processor system as claimed in any of Claims 1 to 9 wherein said silo registers have time-sequential writing and random access reading capability which subtracts from the actual write address a relative read address extracted from the local program memory. 50 55
11. A video processor system as claimed in any of Claims 1 to 10, wherein the video processor

units synchronize to a sub-multiple of the central clock.

12. A video processor system as claimed in any of Claims 1 to 11, wherein a video processor module accommodates storing of a complete video frame line.

Patentansprüche

1. Videoprozessorsystem für Echtzeitverarbeitung von Videoabstastwerten, das eine Videoprozessoreinheit aus einer Anzahl Prozessormodulen (32, 34, 36) enthält, wobei jedes Modul im zeitparallelen Betrieb arbeitende Prozessorelemente (54-62) enthält, deren Eingänge und Ausgänge durch einen Kreuzschienenverteiler, der eine Schnittstelle zu weiterer, für das genannte Prozessormodul externer Beschaltung bildet, miteinander verbunden sind, dadurch gekennzeichnet, daß die genannten Prozessorelemente mindestens zwei Rechenwerkelemente (54, 56, 58) und mindestens ein Speicherprozessorelement (60, 62) mit Adreßverarbeitungsfähigkeit umfassen, daß der genannte Kreuzschienenverteiler einen ersten Datenpfad (104) aus einer Anzahl Kanäle enthält, wobei jeder Kanal ausschließlich mit einem mehrere Bit breiten Ausgang eines jeweiligen der Prozessorelemente des betreffenden Prozessormoduls verbunden ist, und einen zweiten Datenpfad (102) aus einer Anzahl Kanäle mit einer kombinierten Breite, die mindestens gleich der kombinierten Breite der genannten ersten Kanäle ist, und der Eingangskanäle des betreffenden Prozessormoduls repräsentiert, daß alle Eingänge aller Prozessorelemente jedes Prozessormoduls selektiv mit jedem der genannten ersten und zweiten Datenpfade verbunden werden können und jeder ihrer Eingänge mit einem Silo-Register versehen ist, wobei alle Silo-Register zeitsequentielle Schreibfähigkeit und Direktzugriff-Lesefähigkeit haben, wobei der Kreuzschienenverteiler entweder mit einem Ausgangsgatter-Prozessorelement (64) oder einem Eingangsgatter-Prozessorelement versehen ist, mit zugehörigem Datenpuffer (98) zur Bildung einer Schnittstelle zwischen zwei miteinander verbundenen Prozessormodulen, daß jedes der genannten Prozessorelemente (54-62, 64) ein lokales Steuerelement mit einem Programmspeicher hat, der einen Multibefehlsprogrammzyklus (84-100) aufnimmt und daß das Videoprozessorsystem einen Takt (52) zum Ansteuern der Videoprozessormodule bei einer Frequenz hat, die in einer festen Beziehung zum Auftreten der empfangenen Videoabstastwerte steht.



2. Videoprozessorsystem mit mindestens zwei miteinander verbundenen Videoprozessoreinheiten nach Anspruch 1, von denen jede mindestens zwei Videoprozessormodule umfaßt.
3. Videoprozessorsystem nach Anspruch 2 mit mindestens einem mit mindestens einer Videoprozessoreinheit verbundenen Bildspeicher.
4. Videoprozessorsystem nach Anspruch 2 oder 3, wobei jede Videoprozessoreinheit Multiplex/Demultiplex-Schaltungen (38, 40, 42, 44, 46, 48) für externe Schnittstellenbildung bei einer kleineren Bitrate als die Schnittstelle zwischen den verschiedenen Videoprozessormodulen des betreffenden Videoprozessorsystems hat.
- Videoprozessorsystem nach einem der Ansprüche 1 bis 4, wobei jedes Videoprozessormodul mindestens drei Rechenwerkelemente und mindestens zwei Speicherprozessorelemente mit Adreßverarbeitungsfähigkeit hat.
6. Videoprozessorsystem nach einem der Ansprüche 1 bis 5, wobei jedes Prozesselement eines Videoprozessormoduls mit einer gleichartigen Eingangsschaltung versehen ist und diese Eingangsschaltungen zusammen den genannten Kreuzschienenverteiler bilden.
7. Videoprozessorsystem nach einem der Ansprüche 1 bis 6, wobei die genannten Programmspeicher RAMs sind und jedes Videoprozessormodul einen Initialisierungsbus zum Laden der RAMs ihrer Videoprozessormodule hat.
8. Videoprozessorsystem nach Anspruch 7, wobei der Bus einkanalig ist.
9. Videoprozessorsystem nach Anspruch 7 oder 8, wobei die Speicherprozessorelemente ein Laden ihres Datenspeichers über den Initialisierungsbus zulassen.
10. Videoprozessorsystem nach einem der Ansprüche 1 bis 9, wobei die Silo-Register zeitsequentielle Schreibfähigkeit und Direktzugriff-Lesefähigkeit haben, wodurch von der aktuellen Schreibadresse eine dem lokalen Programmspeicher entnommene relative Leseadresse subtrahiert wird.
11. Videoprozessorsystem nach einem der Ansprüche 1 bis 10, wobei die Videoprozessoreinheiten bis auf ein Teilfaches des zentralen Taktes synchronisiert werden.

12. Videoprozessorsystem nach einem der Ansprüche 1 bis 11, wobei ein Videoprozessormodul Kapazität zur Speicherung einer vollständigen Videobildzeile hat.

Revendications

1. Système de traitement vidéo pour le traitement en temps réel d'échantillons vidéo et comprenant une unité de traitement vidéo constituée d'une pluralité de modules de traitement (32, 34, 36), chaque module comprenant des éléments de traitement (54-62) fonctionnant en parallèle dans le temps et dont les entrées et les sorties sont interconnectées par un commutateur Crossbar qui assure la liaison à d'autres circuits extérieurs au module de traitement, caractérisé en ce que les éléments de traitement constitués d'au moins deux éléments ALU (54, 56, 58) et d'au moins un élément de traitement de mémoire (60, 62) à capacité de traitement d'adresses, que le commutateur Crossbar comprend un premier trajet de données (104) constitué d'une pluralité de canaux, chaque canal étant connecté exclusivement à une sortie de largeur multibit d'un des éléments de traitement du module de traitement en question, et un second trajet de données (102) constitué d'une pluralité de canaux présentant une largeur combinée égale au moins à la largeur combinée des premiers canaux et représentant des canaux d'entrée du module de traitement en question, que tous les éléments de traitement de chaque module de traitement peuvent être connectés sélectivement par toutes leurs autres entrées à l'un quelconque des premier et second trajets de données, chacune de leurs entrées étant pourvue d'un registre-silo, le registre-silo présentant une capacité d'écriture séquentielle dans le temps et de lecture à accès aléatoire, le commutateur Crossbar étant pourvu d'un élément processeur formant porte de sortie (64) ou d'un élément processeur formant porte d'entrée, avec un tampon de données associé (98) pour assurer la liaison entre deux modules de traitement interconnectés, que chaque élément de traitement (54-62, 64) comporte un élément de commande local avec une mémoire de programme contenant un cycle de programme multi-instruction (84-100) et que le système de traitement vidéo comporte une horloge (52) destinée à activer les modules de traitement vidéo à une fréquence qui présente une relation fixe à l'égard de la récurrence des échantillons vidéo reçus.



2. Système de traitement vidéo, comprenant au moins deux unités de traitement vidéo interconnectées suivant la revendication 1, qui comprennent chacune au moins deux modules de traitement vidéo.

3. Système de traitement vidéo suivant la revendication 2, comprenant au moins une mémoire de trame interconnectée avec au moins une unité de traitement vidéo.

4. Système de traitement vidéo suivant la revendication 2 ou 3, chaque unité de traitement vidéo comprenant un circuit multiplex/démultiplex (38, 40, 42, 44, 46, 48) pour assurer la liaison externe à une largeur de bits plus étroite que la liaison entre les divers modules de traitement vidéo de l'unité de traitement vidéo en question.

5. Système de traitement vidéo suivant l'une quelconque des revendications 1 à 4, dans lequel tout module de traitement vidéo comporte au moins trois éléments ALU et au moins deux éléments de traitement de mémoire à capacité de traitement d'adresse.

6. Système de traitement vidéo suivant l'une quelconque des revendications 1 à 5, dans lequel chaque élément de traitement d'un module de traitement vidéo est pourvu d'un circuit d'entrée uniforme et les circuits d'entrée constituent collectivement le commutateur Crossbar.

7. Système de traitement vidéo suivant l'une quelconque des revendications 1 à 6, dans lequel les mémoires de programme sont des mémoires RAM et chaque module de traitement vidéo comporte un bus d'amorçage pour charger les RAM de ces modules de traitement vidéo.

8. Système de traitement vidéo suivant la revendication 7, dans lequel le bus est monocanal.

9. Système de traitement vidéo suivant la revendication 7 ou 8, dans lequel les éléments de traitement vidéo permettent le chargement de leurs mémoires de données via le bus d'amorçage.

10. Système de traitement vidéo suivant l'une quelconque des revendications 1 à 9, dans lequel les registres-silo présentent une capacité d'écriture séquentielle dans le temps et de lecture à accès aléatoire qui soustrait de l'adresse d'écriture réelle une adresse de lec-

ture relative de la mémoire de programme locale.

11. Système de traitement vidéo suivant l'une quelconque des revendications 1 à 10, dans lequel les unités de traitement vidéo se synchronisent sur un sous-multiple de l'horloge centrale.

12. Système de traitement vidéo suivant l'une quelconque des revendications 1 à 11, dans lequel le module de traitement vidéo accepte le stockage d'une ligne d'image vidéo complète.

5

10

15

20

25

30

35

40

45

50

55