

A B S T R A C T

A semiconductor memory device according to an embodiment includes: a row decoder and a memory cell array including a first block. The first block includes: a first region (CEL), a second region (WLHU) adjacent to the first region (CEL) in the first direction (Y-direction), and a third region (CNCT) configured to connect the first region (CEL) and the second region (WLHU). The memory cell array further includes: a first insulating layer (730) buried in a first trench (DY) between the first region (CEL) and the second region (WLHU) and in contact with the third region (CNCT); a first contact plug (CP12) provided in the first insulating layer (730) and electrically connected to the row decoder; and a first interconnect (IC1) configured to connect a selection gate line (SGD) and the first contact plug (CP12).