DICING TAPE THERMAL MANAGEMENT BY WAFER FRAME SUPPORT RING COOLING DURING PLASMA DICING

BACKGROUND

1) FIELD

[0001] Embodiments of the present invention pertain to the field of semiconductor processing and, in particular, to methods of dicing semiconductor wafers, each wafer having a plurality of integrated circuits thereon.

2) DESCRIPTION OF RELATED ART

[0002] In semiconductor wafer processing, integrated circuits are formed on a wafer (also referred to as a substrate) composed of silicon or other semiconductor material. In general, layers of various materials which are either semiconducting, conducting or insulating are utilized to form the integrated circuits. These materials are doped, deposited and etched using various well-known processes to form integrated circuits. Each wafer is processed to form a large number of individual regions containing integrated circuits known as dies.

[0003] Following the integrated circuit formation process, the wafer is "diced" to separate the individual die from one another for packaging or for use in an unpackaged form within larger circuits. The two main techniques that are used for wafer dicing are scribing and sawing. With scribing, a diamond tipped scribe is moved across the wafer surface along pre-formed scribe lines. These scribe lines extend along the spaces between the dies. These spaces are commonly referred to as “streets.” The diamond scribe forms shallow scratches in the wafer surface along the streets. Upon the application of pressure, such as with a roller, the wafer separates along the scribe lines. The breaks in the wafer follow the crystal lattice structure of the wafer substrate. Scribing can be used for wafers that are about 10 mils (thousandths of an inch) or less in thickness. For thicker wafers, sawing is presently the preferred method for dicing.

[0004] With sawing, a diamond tipped saw rotating at high revolutions per minute contacts the wafer surface and saws the wafer along the streets. The wafer is mounted on a supporting member such as an adhesive film stretched across a film frame and the saw is repeatedly applied to both the vertical and horizontal streets. One problem with either scribing or sawing is that chips and gouges can form along the severed edges of the dies. In addition, cracks can form and propagate from the edges of the dies into the substrate and render the

integrated circuit inoperative. Chipping and cracking are particularly a problem with scribing because only one side of a square or rectangular die can be scribed in the <110>direction of the crystalline structure. Consequently, cleaving of the other side of the die results in a jagged separation line. Because of chipping and cracking, additional spacing is required between the dies on the wafer to prevent damage to the integrated circuits, e.g., the chips and cracks are maintained at a distance from the actual integrated circuits. As a result of the spacing requirements, not as many dies can be formed on a standard sized wafer and wafer real estate that could otherwise be used for circuitry is wasted. The use of a saw exacerbates the waste of real estate on a semiconductor wafer. The blade of the saw is approximate 15 microns thick. As such, to insure that cracking and other damage surrounding the cut made by the saw does not harm the integrated circuits, three to five hundred microns often must separate the circuitry of each of the dies. Furthermore, after cutting, each die requires substantial cleaning to remove particles and other contaminants that result from the sawing process.

[0005] Plasma dicing has also been used, but may have limitations as well. For example, one limitation hampering implementation of plasma dicing may be cost. A standard lithography operation for patterning resist may render implementation cost prohibitive. Another limitation possibly hampering implementation of plasma dicing is that plasma processing of commonly encountered metals (e.g., copper) in dicing along streets can create production issues or throughput limits.

SUMMARY

[0006] Embodiments of the present invention include methods of dicing semiconductor wafers, each wafer having a plurality of integrated circuits thereon.

[0007] In an embodiment, a method of dicing a semiconductor wafer having a plurality of integrated circuits involves introducing a substrate supported by a substrate carrier into a plasma etch chamber. The substrate has a patterned mask thereon covering integrated circuits and exposing streets of the substrate. The substrate carrier has a backside. The method also involves supporting at least a portion of the backside of the substrate carrier on a chuck of the plasma etch chamber. The method also involves cooling substantially all of the backside of the substrate carrier, the cooling involving cooling at least a first portion of the backside of the substrate carrier by the chuck. The method also involves plasma etching the substrate through the streets to singulate the integrated circuits while performing the cooling substantially all of the backside of the substrate carrier.

[0008] In another embodiment, a plasma etch chamber includes a plasma source disposed in

an upper region of the plasma etch chamber. A cooling chuck is disposed below the plasma source, the cooling chuck for supporting a first portion of a substrate carrier. A cooling concentric ring surrounds the cooling chuck, the cooling concentric ring for supporting a second portion of the substrate carrier. Together, the cooling chuck and the cooling concentric ring are together for cooling substantially all of a backside of the substrate carrier.

[0009] In another embodiment, a plasma etch chamber includes a plasma source disposed in an upper region of the plasma etch chamber. A cooling chuck is disposed below the plasma source, the cooling chuck for supporting and cooling substantially all of a backside of a substrate carrier.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure 1 illustrates a top plan of a semiconductor wafer to be diced, in accordance with an embodiment of the present invention.

[0011] Figure 2 illustrates a top plan of a semiconductor wafer to be diced that has a dicing mask formed thereon, in accordance with an embodiment of the present invention.

[0012] Figure 3 illustrates a plan view of a substrate carrier suitable for supporting a wafer during a singulation process, in accordance with an embodiment of the present invention.

[0013] Figure 4 illustrates (a) a substrate carrier supported by a cooling enlarged chuck or (b) by a cooling concentric chuck ring and cooling chuck pairing, in accordance with an embodiment of the present invention.

[0014] Figure 5 illustrates the substrate carrier of Figure 3 with an overlying actively-cooled shadow ring or a plasma thermal shield, or both, and with an underlying cooling concentric chuck ring or cooling enlarged chuck, in accordance with another embodiment of the present invention.

[0015] Figure 6 illustrates an angled view of an actively-cooled shadow ring for heat dissipation in a plasma chamber with relative positioning to an etch cathode shown and relative sizing to a wafer support shown, in accordance with an embodiment of the present invention.

[0016] Figure 7 illustrates an enlarged view of the plasma exposed coupler of the support apparatus of Figure 6, in accordance with an embodiment of the present invention.

[0017] Figure 8 illustrates an enlarged view of the bellows feed-through of the support apparatus of Figure 6, in accordance with an embodiment of the present invention.

[0018] Figure 9 illustrates an angled top view and angled bottom view of a plasma thermal shield, in accordance with an embodiment of the present invention.

[0019] Figure 10 illustrates an enlarged angled cross-sectional view of the plasma thermal
shield of Figure 9 as positioned on a top surface of a shadow ring, in accordance with an embodiment of the present invention.

[0020] Figure 11 illustrates a cross-sectional view of an etch reactor, in accordance with an embodiment of the present invention.

[0021] Figure 12 is a Flowchart representing operations in a method of dicing a semiconductor wafer including a plurality of integrated circuits, in accordance with an embodiment of the present invention.

[0022] Figure 13A illustrates a cross-sectional view of a semiconductor wafer including a plurality of integrated circuits during performing of a method of dicing the semiconductor wafer, corresponding to operation 1202 of the Flowchart of Figure 12, in accordance with an embodiment of the present invention.

[0023] Figure 13B illustrates a cross-sectional view of a semiconductor wafer including a plurality of integrated circuits during performing of a method of dicing the semiconductor wafer, corresponding to operation 1204 of the Flowchart of Figure 12, in accordance with an embodiment of the present invention.

[0024] Figure 13C illustrates a cross-sectional view of a semiconductor wafer including a plurality of integrated circuits during performing of a method of dicing the semiconductor wafer, corresponding to operation 1210 of the Flowchart of Figure 12, in accordance with an embodiment of the present invention.

[0025] Figure 14 illustrates the effects of using a laser pulse in the femtosecond range versus longer pulse times, in accordance with an embodiment of the present invention.

[0026] Figure 15 illustrates compaction on a semiconductor wafer achieved by using narrower streets versus conventional dicing which may be limited to a minimum width, in accordance with an embodiment of the present invention.

[0027] Figure 16 illustrates freeform integrated circuit arrangement allowing denser packing and, hence, more die per wafer versus grid alignment approaches, in accordance with an embodiment of the present invention.

[0028] Figure 17 illustrates a block diagram of a tool layout for laser and plasma dicing of wafers or substrates, in accordance with an embodiment of the present invention.

[0029] Figure 18 illustrates a block diagram of an exemplary computer system, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0030] Methods of and apparatuses for dicing semiconductor wafers, each wafer having a plurality of integrated circuits thereon, are described. In the following description, numerous specific details are set forth, such as substrate carriers for thin wafers, scribing and plasma etching conditions and material regimes, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known aspects, such as integrated circuit fabrication, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

[0031] One or more embodiments described herein are directed to dicing tape thermal management via wafer frame support ring cooling during plasma dicing. One or more embodiments are directed to a hybrid laser scribing and plasma etching die singulation process.

[0032] To provide context, during plasma dicing of a wafer mounted on a tape frame, thermal management against dicing tape thermal damage or degradation can be critical to ensure successful plasma etch processing. Over-heating during plasma processing may lead to dicing tape cracking, burning or distortion, or lead to other issues such as adhesion degradation between the dicing tape and supporting frame. Such issues can result in failure of the etch process or catastrophic wafer damage. Current practice involves cooling of the wafer or substrate on a supporting chuck housed in a plasma etch chamber. The cooling is achieved by maintaining the chuck temperature at or below zero degrees Celsius, e.g., such as at a temperature of approximately -10°C.

[0033] In the case of a substrate or wafer on a carrier, the portion of the carrier supporting the wafer or substrate sits on the cooling chuck. However, the portion of the dicing tape between the wafer or substrate edge and the tape frame (as well as the tape frame) rests on a concentric support ring that is not cooled. Accordingly, heat radiation from a plasma is typically blocked by adding a shield ring above the wafer or substrate and covers the frame and the exposed dicing tape between the wafer edge and the frame. Such a shield ring, however, may not on its own be sufficient to protect the exposed portion of the carrier or dicing tape from thermal damage or degradation. Additionally, diverse types of carrier or dicing tapes of

differing durability may be subjected to a variety of etch processes for singulation. Accordingly, one or more embodiments described herein provide a broad and robust approach for protecting dicing or carrier tape during plasma etching for wafer or substrate singulation.

[0034] One or more embodiments described herein address thermal management by removing a heat load from the dicing or carrier tape and frame of a substrate carrier. In an embodiment, the heat load is removed from the substrate or wafer carrier backside. In one specific embodiment, the typical size of the supporting wafer chuck is maintained and a cooling concentric support ring is used in combination with the chuck. The cooling temperature of the support ring may not necessarily be as low as that of the chuck, e.g., may be approximately in the range of 0 to -10 degrees Celsius. In another specific embodiment, the chuck is enlarged to a diameter suitable for supporting the wafer, tape and the frame. The enlarged chuck is cooled, including in regions supporting the carrier frame and the portions of the dicing tape between the wafer and the frame. Thus, more generally, one or more embodiments described herein are directed to backside cooling of a substrate carrier frame and tape by a cooling concentric chuck ring or a cooling enlarged chuck.

[0035] In an exemplary application, and to provide further context, a wafer or substrate die singulation process involves placing a thinned wafer or substrate on a flexible polymer tape with an adhesive. The flexible polymer tape is then attached to a supportive tape frame ring. In some aspects, the only rigid form for reliable pick and place motion of singulated die is the tape frame. However, the radial location of the tape frame is typically outside of the normal range of a chuck such as is used in a plasma etch chamber. Additionally, the tape and tape frame pairing should typically not be exposed to temperatures that exceed the allowable temperature of the tape and adhesive. Addressing one or more of the above issues, in accordance with one or more embodiments described herein, the overall design of a chuck or chuck and concentric ring pairing provides backside cooling of the entire region a wafer or substrate carrier.

[0036] In an aspect of the present disclosure, a hybrid wafer or substrate dicing process involving an initial laser scribe and subsequent plasma etch may be implemented for die singulation. The laser scribe process may be used to cleanly remove a mask layer, organic and inorganic dielectric layers, and device layers. The laser etch process may then be terminated upon exposure of, or partial etch of, the wafer or substrate. The plasma etch portion of the dicing process may then be employed to etch through the bulk of the wafer or substrate, such as through bulk single crystalline silicon, to yield die or chip singulation or dicing. In one embodiment, a cooling concentric chuck ring or cooling enlarged chuck is implemented during

the etch portion of the dicing process. In an embodiment, the wafer or substrate is supported a substrate carrier having a tape frame during the singulation process, including during the etch portion of the singulation process.

[0037] In accordance with an embodiment of the present invention, described herein are one

or more apparatuses for, and methods of, cooling a tape frame and exposed tape region of a substrate carrier during plasma etch in a singulation process. For example, an apparatus may be used to support and cool the film frame used to hold a thin silicon wafer on a tape supported by the frame. The manufacturing processes related to integrated circuit (IC) packaging may require that a thinned silicon wafer be supported and mounted on a film such as a die attach film. In one embodiment, a die attach film is also supported by a substrate carrier and is used to adhere a thin silicon wafer to the substrate carrier.

[0038] To provide further context, conventional wafer dicing approaches include diamond saw cutting based on a purely mechanical separation, initial laser scribing and subsequent diamond saw dicing, or nanosecond or picosecond laser dicing. For thin wafer or substrate singulation, such as 50 microns thick bulk silicon singulation, the conventional approaches have yielded only poor process quality. Some of the challenges that may be faced when singulating die from thin wafers or substrates may include microcrack formation or delamination between different layers, chipping of inorganic dielectric layers, retention of strict kerf width control, or precise ablation depth control. Embodiments of the present invention include a hybrid laser scribing and plasma etching die singulation approach that may be useful for overcoming one or more of the above challenges.

[0039] In accordance with an embodiment of the present invention, a combination of laser scribing and plasma etching is used to dice a semiconductor wafer into individualized or singulated integrated circuits. In one embodiment, femtosecond-based laser scribing is used as an essentially, if not totally, non-thermal process. For example, the femtosecond-based laser scribing may be localized with no or negligible heat damage zone. In an embodiment, approaches herein are used to singulated integrated circuits having ultra-low k films. With convention dicing, saws may need to be slowed down to accommodate such low k films. Furthermore, semiconductor wafers are now often thinned prior to dicing. As such, in an embodiment, a combination of mask patterning and partial wafer scribing with a femtosecond-based laser, followed by a plasma etch process, is now practical. In one embodiment, direct writing with laser can eliminate need for a lithography patterning operation of a photo-resist

layer and can be implemented with very little cost. In one embodiment, through-via type silicon etching is used to complete the dicing process in a plasma etching environment.

[0040] Thus, in an aspect of the present invention, a combination of laser scribing and plasma etching may be used to dice a semiconductor wafer into singulated integrated circuits. Figure 1 illustrates a top plan of a semiconductor wafer to be diced, in accordance with an embodiment of the present invention. Figure 2 illustrates a top plan of a semiconductor wafer to be diced that has a
dicing mask formed thereon, in accordance with an embodiment of the present invention.

[0041] Referring to Figure 1, a semiconductor wafer 100 has a plurality of regions 102 that include integrated circuits. The regions 102 are separated by vertical streets 104 and horizontal streets 106. The streets 104 and 106 are areas of semiconductor wafer that do not contain integrated circuits and are designed as locations along which the wafer will be diced. Some embodiments of the present invention involve the use of a combination laser scribe and plasma etch technique to cut trenches through the semiconductor wafer along the streets such that the dies are separated into individual chips or die. Since both a laser scribe and a plasma etch process are crystal structure orientation independent, the crystal structure of the semiconductor wafer to be diced may be immaterial to achieving a vertical trench through the wafer.

[0042] Referring to Figure 2, the semiconductor wafer 100 has a mask 200 deposited upon the semiconductor wafer 100. In one embodiment, the mask is deposited in a conventional manner to achieve an approximately 4-10 micron thick layer. The mask 200 and a portion of the semiconductor wafer 100 are, in one embodiment, patterned with a laser scribing process to define the locations (e.g., gaps 202 and 204) along the streets 104 and 106 where the semiconductor wafer 100 will be diced. The integrated circuit regions of the semiconductor wafer 100 are covered and protected by the mask 200. The regions 206 of the mask 200 are positioned such that during a subsequent etching process, the integrated circuits are not degraded by the etch process. Horizontal gaps 204 and vertical gaps 202 are formed between the regions 206 to define the areas that will be etched during the etching process to finally dice the semiconductor wafer 100. In accordance with an embodiment of the present invention, a cooling concentric chuck ring or cooling enlarged chuck is implemented during the etch portion of the dicing process.

[0043] As mentioned briefly above, a substrate for dicing is supported by a substrate carrier during the plasma etching portion of a die singulation process, e.g., of a hybrid laser ablation and plasma etching singulation scheme. For example, Figure 3 illustrates a plan view

of a substrate carrier suitable for supporting a wafer during a singulation process, in accordance with an embodiment of the present invention.

[0044] Referring to Figure 3, a substrate carrier 300 includes a layer of backing tape 302 surrounded by a tape ring or frame 304. A wafer or substrate 306 is supported by the backing tape 302 of the substrate carrier 300. In one embodiment, the wafer or substrate 306 is attached to the backing tape 302 by a die attach film. In one embodiment, the tape ring 304 is composed of stainless steel.

[0045] In an embodiment, a singulation process can be accommodated in a system sized to receive a substrate carrier such as the substrate carrier 300. In one such embodiment, a system such as system 1700, described in greater detail below, can accommodate a wafer frame without impact on the system footprint that is otherwise sized to accommodate a substrate or wafer not supported by a substrate carrier. In one embodiment, such a processing system is sized to accommodate 300 millimeter-in-diameter wafers or substrates. The same system can accommodate a wafer carrier approximately 380 millimeters in width by 380 millimeters in length, as depicted in Figure 3. However, it is to be appreciated that systems may be designed to handle 450 millimeter wafers or substrate or, more particularly, 450 millimeter wafer or substrate carriers.

[0046] In an aspect of the present invention, one or more embodiments are directed to a cooling concentric chuck ring or cooling enlarged chuck. In one such embodiment, a substrate carrier is cooled by the cooling concentric chuck ring or cooling enlarged chuck during a plasma etching process. In an example, Figure 4 illustrates (a) a substrate carrier supported by a cooling enlarged chuck or (b) by a cooling concentric chuck ring and cooling chuck pairing, in accordance with an embodiment of the present invention.

[0047] Referring to the left-hand side of Figure 4, a wafer/wafer carrier pairing 400 is coupled with a wafer shield ring 402. The wafer/wafer carrier pairing 400 includes a substrate (wafer) 410 supported by a wafer or substrate carrier 404. The wafer or substrate carrier 404 includes a tape frame 406 that supports a carrier or dicing tape 408. In one embodiment, the carrier or dicing tape 408 is affixed to an overlying tape frame 406, as is depicted in Figure 4. In one embodiment, the wafer shield ring 402 includes an annular ring 412 with a central opening 414, as is shown cross-sectionally in Figure 4.

[0048] Referring to the right-hand-side of Figure 4, in pathway (a), the wafer/wafer carrier pairing 400 and wafer shield ring 402 assembly are seated on a cooling enlarged chuck 420. In pathway (b), the wafer/wafer carrier pairing 400 and wafer shield ring 402 assembly are seated on a cooling concentric chuck ring 424 and cooling chuck 422 pairing.

[0049] In either case (a) or (b), in accordance with an embodiment of the present invention, substantially all of the backside of the wafer or substrate carrier 404 is cooled during plasma processing. In one such embodiment, the wafer or substrate carrier 404 includes outer tape frame 406 and supporting dicing tape 408, and cooling substantially all of the backside of the substrate carrier involves cooling the tape frame 406 and the wafer or substrate 410. In a specific such embodiment, referring to pathway (b) of Figure 4, the dicing tape 408 is disposed between the tape frame 406 and the cooling concentric chuck ring 424 surrounding the cooling chuck 422. The dicing tape 408 is further disposed between the substrate 410 and the cooling chuck 422. In another specific embodiment, referring to pathway (a) of Figure 4, the dicing tape 408 is disposed between the tape frame 406 and the enlarged cooling chuck 420, and also between the substrate 410 and the enlarged cooling chuck 420. In both cases, in an embodiment, a portion of the front side of the wafer or substrate carrier 404 and, possibly, an outermost portion of the substrate 410 is protected by the wafer shield ring (or shadow ring) 402.

[0050] With reference again to Figure 4, and as will be described in greater detail below, in accordance with an embodiment of the present invention, a method of dicing a semiconductor wafer having a plurality of integrated circuits involves introducing a substrate supported by a substrate carrier into a plasma etch chamber. The substrate has a patterned mask thereon covering integrated circuits and exposing streets of the substrate. The substrate carrier has a backside. At least a portion of the backside of the substrate carrier is supported on a chuck (e.g., chuck 420 or chuck 422) of the plasma etch chamber. Substantially all of the backside of the substrate carrier is cooled, the cooling involving cooling at least a first portion of the backside of the substrate carrier by the chuck. The substrate is plasma etched through the streets to singulate the integrated circuits while cooling substantially all of the backside of the substrate carrier.

[0051] With reference again to pathway (a) of Figure 4, in an embodiment, the cooling chuck 420 is an enlarged cooling chuck (as compared to a normal processing chuck used for supporting wafers or substrates directly instead of supporting wafer or substrate carriers) has a supporting area at least as large as the backside of the wafer or substrate carrier 404. As such, cooling substantially all of the backside of the wafer or substrate carrier 404 involves cooling substantially all of the backside of the wafer or substrate carrier 404 only with the cooling chuck 420. In one such embodiment, during plasma processing (such as plasma etching), the enlarged cooling chuck 420 is maintained at a temperature at least as low as approximately -10 degrees Celsius.

[0052] With reference again to pathway (b) of Figure 4, in an embodiment, the cooling concentric ring 424 and the cooling chuck 422 together provide a supporting area at least as large as the backside of the wafer or substrate carrier 404. As such, cooling substantially all of the backside of the wafer or substrate carrier 404 involves cooling substantially all of the backside of the wafer or substrate carrier 404 with the combination of the cooling concentric ring 424 and the cooling chuck 422. That is, the cooling chuck 422 cools a first, inner, portion of the wafer or substrate carrier 404, and the cooling concentric ring 424 cools a second, outer, portion of the wafer or substrate carrier 404. In one such embodiment, during plasma processing (such as plasma etching), the chuck cooling 422 is maintained at a temperature at least as low as approximately -10 degrees Celsius, and the cooling concentric chuck ring 424 is maintained at a temperature approximately in the range of 0 to -10 degrees Celsius.

[0053] With reference again to both pathways (a) and (b) of Figure 4, in an embodiment, cooling of the enlarged cooling chuck 420 or the cooling concentric ring 424 and the cooling chuck 422 pairing is provided by a heat transfer fluid loop. In one such embodiment, the heat transfer fluid loop is thermally coupled to a heat sink (e.g., a chiller) to remove heat from the chuck of the chuck/concentric ring pairing. The heat transfer liquid may be any employed in the art, for example a perfluoropolyether known under the trade names of Fluorinert (3M, Inc.) or Galden (Solvey Solexis, Inc), e.g., Galden HT135 for operation in the range of 0°C-20°C.

[0054] More generally, it is to be appreciated that during plasma etching processes, the temperature of wafer is typically controlled by the electrostatic-check. The wafer shield ring acts as a thermal barrier to the frame and tape pairing. However, depending on the specific tape and etching process recipe (particularly process time) employed in a given application, the wafer shield ring may be not sufficient to block the heat from transfer to the frame and tape beneath it. In such a case, the tape and/or frame can become over-heated as to either cause tape damage or delamination of tape from frame or reduction of adhesion between tape and frame. Such damage of tape between the frame and wafer can cause the failure of the etch process and lead to wafer damage. The delamination of tape from the frame is another critical dicing failure. The reduction of adhesion between tape and frame can, for example, cause tape to peel off from the frame during tape expansion operation used for die pick. Accordingly, in one or more embodiments described herein, temperature control is applied on the support ring such that the support ring is maintained below zero (0°C), the temperature of which can be the same (or slightly higher) as that of the surrounded chuck. In another embodiment, the chuck diameter is extended in order to enable holding and cooling of the entire wafer-on-tape-frame

assembly. In either case, in an embodiment, cooling of the tape and frame during etch processing is implemented in order to avoid potential tape damage/degradation.

[0055] In another aspect of the present invention, one or more embodiments described herein are directed to an actively-cooled shadow ring for heat dissipation in a plasma etch chamber. Embodiments may include plasmas and plasma based processes, thermal management, active cooling, and heat dissipation. One or more embodiments described herein are directed to a plasma thermal shield for heat dissipation in a plasma chamber. Embodiments may include plasmas and plasma based processes, thermal management, shielding of plasma generated species, and heat dissipation. Applications for either of the actively-cooled shadow ring or the plasma thermal shield, or both, may include die singulation but other high power etch processes or differentiated etch chemistries may benefit from embodiments described herein. The plasma thermal shield may be used on its own as an inexpensive, passive component, or it may be combined with an actively-cooled shadow ring as a thermal shield to modify plasma conditions. In the latter case, the plasma thermal shield is effectively used as a dopant source in a plasma etch process. In accordance with an embodiment of the present invention, a cooling concentric chuck ring or cooling enlarged chuck is implemented along with an actively-cooled shadow ring or a plasma thermal shield, or both, during a plasma etch process.

[0056] For example, in an embodiment, the assembly including a wafer or substrate on the substrate carrier is subjected to a plasma etch reactor without affecting (e.g., etching) the film frame (e.g., tape ring 304) and the film (e.g., backing tape 302). In one such embodiment, an actively-cooled shadow ring or a plasma thermal shield, or both, are implemented during the etch portion of the dicing process. In an example, Figure 5 illustrates the substrate carrier of Figure 3 with an overlying actively-cooled shadow ring or a plasma thermal shield, or both, and with an underlying cooling concentric chuck ring or cooling enlarged chuck, in accordance with an embodiment of the present invention.

[0057] Referring to Figure 5, the substrate carrier 300, including the layer of backing tape 302 and tape ring or frame 304 is covered, in a top view perspective, by an actively-cooled shadow ring or a plasma thermal shield, or both, (all options represented as 500 in Figure 5). The actively-cooled shadow ring or a plasma thermal shield, or both, 500 includes a ring portion 502 and inner opening 504. In one embodiment, a portion of the supported wafer or substrate 306 is also covered by the actively-cooled shadow ring or a plasma thermal shield, or both, 500 (specifically, portion 506 of the actively-cooled shadow ring or a plasma thermal shield, or both, 500 covers a portion of the wafer or substrate 506). In a specific such

embodiment, the portion 506 of the actively-cooled shadow ring or a plasma thermal shield, or both, 500 covers approximately 1 – 1.5 mm of the outer most portion of the wafer or substrate 306. The portion covered may be referred to as the exclusion region of the wafer or substrate 306 since this area is effectively shielded from a plasma process. In one embodiment, the substrate carrier is supported on a cooling concentric chuck ring or cooling enlarged chuck (not shown), while covered with the actively-cooled shadow ring or a plasma thermal shield, or both.

[0058] In a first such aspect, an exemplary actively-cooled shadow ring for heat dissipation in

a plasma chamber, which may be used as described with, or may be modified to accommodate, a cooling concentric chuck ring or cooling enlarged chuck, is now described in greater detail. In an embodiment, an actively-cooled shadow ring can be implemented to reduce a temperature of a process kit shadow ring during processing of a wafer supported by a wafer carrier. By reducing the temperature of a shadow ring, damage or burning of a die singulation tape that otherwise occurs at elevated temperatures may be mitigated. For example, a damaged or burned die singulation tape normally leads to the wafer or substrate as not being recoverable. Furthermore, the attached tape can become damaged when the tape frame reaches an elevated temperature. Although described herein in the context of tape and frame protection during etch processing for die singulation, use of an actively-cooled shadow ring can provide other process benefits can include an increase in throughput. For example, temperature reduction may otherwise be achieved by easing of process conditions such as RF power reduction, but this requires an increase in process time which is detrimental to throughput.

[0059] Figure 6 illustrates an angled view of an actively-cooled shadow ring for heat dissipation in a plasma chamber with relative positioning to an etch cathode shown and relative sizing to a wafer carrier shown, in accordance with an embodiment of the present invention.

[0060] Referring to Figure 6, a support apparatus 600 for a plasma chamber includes a cathode 602 positioned below an actively-cooled shadow ring 604. A wafer or substrate support 300 with a tape 302 and frame 304 and supporting a wafer of substrate 306 is shown above the actively-cooled shadow ring 604 for sizing perspective. Such a wafer or substrate support can be as described above with respect to Figure 3. In use, the wafer or substrate support/carrier 300 is actually positioned between the actively-cooled shadow ring 604 and the cathode 602. The support apparatus 600 may also include a motorized assembly 614 and a casing 616, which is also depicted in Figure 6. In an embodiment, the support cathode is or includes a cooling concentric chuck ring/chuck pairing or a cooling enlarged chuck.

[0061] Referring again to Figure 6, the actively-cooled shadow ring 604 is fed with coolant gas or liquid by a bellows feed-through 606 which feeds into a plasma exposed coupler 608. In an embodiment, the actively-cooled shadow ring 604 is raised or lowered relative to a fixed cathode by three vertical posts 610 which can be raised for introduction of the substrate or wafer carrier 300 to the cathode 602 and then lowered to clamp the substrate or wafer carrier 300 into position. The three vertical posts 610 attach the actively-cooled shadow ring 604 to a circular ring 605 below. The circular ring 605 is connected to the motorized assembly 614 and provides the vertical motion and
positioning of the actively-cooled shadow ring 604.

[0062] The substrate or wafer carrier 300 may rest on a plurality of pads that sit between the actively-cooled shadow ring 604 and the cathode 602. For illustrative purposes, one such pad 612 is depicted. However, it is to be appreciated that the pad 612 is actually below or underneath the actively-cooled shadow ring 604, and that more than one pad is typically used, such as four pads. In an embodiment, the actively-cooled shadow ring 604 is composed of aluminum with a hard anodized surface or a ceramic coating. In an embodiment, the actively-cooled shadow ring 604 is sized to entirely cover, from a top-down perspective, the tape frame 304, the tape 302, and the outer most region of the substrate 306 during plasma processing, as was described in association with Figure 5. In one specific such embodiment, the leading edge of the shadow ring to the wafer is approximately 0.050 inches high.

[0063] Figure 7 illustrates an enlarged view of the plasma exposed coupler 608 of the support apparatus 600 of Figure 6, in accordance with an embodiment of the present invention. Referring to Figure 7, the terminating end of the bellows feed-through is depicted as coupled to the plasma exposed coupler 608. A pair of fluid connections 720, such as a supply and return line pair, is shown as entering/exiting the actively-cooled shadow ring 604. The plasma exposed coupler 608 is depicted as essentially transparent in order to reveal the pair of fluid connections 720 for illustrative purposes. In an embodiment, the pair of fluid connections 720 provides an entrance/exit to an internal fluid channel that circulates through the actively-cooled shadow ring 604. In one such embodiment, the pair of fluid connections 720 enables continual flow of a cooling fluid or gas through the actively-cooled shadow ring during plasma processing. In a specific embodiment, the cooling channels travel essentially the entire mid-circumference of the body of an annular actively-cooled shadow ring.

[0064] In an embodiment, the ability to enable such continual flow can provide superior temperature control of the shadow ring which enables temperature control (e.g., reduced temperature exposure) of the tape frame and tape of a substrate carrier clamped to the actively-

cooled shadow ring 604. This protection of the tape frame and tape is in addition to the protection provided by physically blocking the plasma from reaching the tape frame and tape of the substrate or wafer carrier. The fluid-channeled shadow ring, referred to herein as actively-cooled shadow ring 604, is distinguished from passively cooled shadow rings that may merely be cooled by contact with a heat sink or a cooled chamber wall.

[0065] Referring again to Figure 7, in an embodiment, the plasma exposed coupler 608 is a fixed-length connection between the actively-cooled shadow ring 604 above and the bellows feed-through 606 below. The coupling provided is intended to be exposed to a plasma process and to allow the bellows feed-through 606 to be positioned away from the plasma process. In one such embodiment, the coupling is a vacuum connection between the bellows feed-through 606 and the actively-cooled shadow ring 604.

[0066] Figure 8 illustrates an enlarged view of the bellows feed-through 606 of the support apparatus 600 of Figure 6, in accordance with an embodiment of the present invention. Referring to Figure 8, the bellow feed-through 606 is shown having an outer bellows 830 with an inner sleeve 832. A connection 834 is provided for coupling to a chamber body. The lower opening of the bellows feed-through 606 can accommodate supply and return lines for the coolant used to cool actively-cooled shadow ring 604. In one embodiment, the outer bellows 830 is metallic, the inner sleeve 832 is a stainless steel protective sleeve to accommodate hoses for supply and return lines, the sizing of connection 834 is an NW40 connection.

[0067] In an embodiment, the bellows feed-through 606 allows vertical motion of the actively-cooled shadow ring 604, which is in vacuum. This motion is provided by a motorized assembly which provides the necessary vertical positioning. The bellows feed-through must have allowance for this range of motion. In one embodiment, the bellows feed-through 606 has a vacuum connection at either end, e.g., a vacuum centering o-ring seal at one end and an o-ring seal on the other end. In one embodiment, the inner portion of the bellows feed-through 606 has a protective shield to allow fluid lines to pass-through without compromising the convolutions. Together, the bellows feed-through 606 and the plasma exposed coupler 608 provide a path for the supply and return lines for a coolant fluid. The coolant fluid may be passed through a fluid chiller (not depicted) after exiting and/or before entering the actively-cooled shadow ring 604.

[0068] In an embodiment, the actively-cooled shadow ring 604 is capable of dissipating a large quantity of plasma heat and in a short period of time. In one such embodiment, the actively-cooled shadow ring 604 is designed to be capable of reducing a shadow ring from temperatures greater than 260 degrees Celsius to less than 120 degrees Celsius on a continuous

processing basis. In an embodiment, with a vacuum-to-atmosphere connection available, an internal plasma-exposed component could be cooled and/or vertically-moved in a chamber.

[0069] Thus, in an embodiment, an actively-cooled shadow ring assembly includes the following major components: a bellows feed-through, a plasma-exposed coupling, a fluid-channeled shadow ring, fluid supply and return lines, and a fluid chiller. The actively-cooled shadow ring may also have a plasma shield as a plasma protective cover over the actively-cooled shadow ring, such as described in association with Figures 9 and 10 below. The actively-cooled shadow ring has an internal fluid channel to allow a chilled fluid to flow and remove plasma-induced heat. With respect to sizing, an actively-cooled shadow ring may have an increased thickness on the order of about $1/8^{th}$ of an inch relative to a conventional shadow ring in order to accommodate the cooling channels. In an embodiment, the fluid channel is designed such that it removes this heat before the actively-cooled shadow ring develops a temperature that will damage the tape or greatly elevate the temperature of the tape frame of a wafer or substrate carrier. In one embodiment, the fluid itself is non-RF conductive so as not to draw RF power away from the plasma or RF power to the chiller. In one embodiment, the actively-cooled shadow ring is capable of withstanding high RF power and not suffer plasma erosion. The supply and return fluid lines are connected to the actively-cooled shadow ring and run inside the plasma-exposed coupler and bellows feed-through. In one embodiment, the fluid lines are non-RF conductive and are capable of handling fluid temperatures below 0 degrees Celsius. In one embodiment, an associated chiller is capable of supplying a fluid below 0 degrees Celsius and with enough volume capacity to quickly dissipate the plasma heat developed.

[0070] In an embodiment, an actively-cooled shadow ring assembly is designed such that no fluid leaks or spills can be introduced into a process chamber housing the assembly. The actively-cooled shadow ring is removable for assembly and servicing. Components or kits may be grouped as: (1) an NW40 sized bellows with inner shield which includes a vacuum feed-through and inner shield for fluid lines, (2) a plasma-exposed coupler which can be a swap kit part, if necessary, (3) an actively-cooled shadow ring with an aluminum-core and anodized or ceramic coating, (4) low temperature fluid lines including a one-piece fluid connection line. Additional hardware may include a secondary chiller specifically designed for the actively-cooled shadow ring.

[0071] In a second such aspect, an exemplary plasma thermal shield for heat dissipation in a plasma chamber, which may be used as described with, or may be modified to accommodate, a cooling concentric chuck ring or cooling enlarged chuck, is now described in

greater detail. The plasma thermal shield can be used with a standard shadow ring as an inexpensive, passive component for thermal protection of substrate carrier that is plasma etched using a conventional shadow ring. On the other hand, the plasma thermal shield may be used together with the above described actively-cooled shadow ring.

[0072] As an example Figure 9 illustrates an angled top view and angled bottom view of a plasma thermal shield, in accordance with an embodiment of the present invention.

[0073] Referring to the top view of Figure 9, a plasma thermal shield 900 is an annular ring

with an inner opening 901. In an embodiment, the plasma thermal shield 900 is sized and shaped to be compatible with, e.g., by nesting upon a top surface of, a shadow ring included in a plasma processing chamber. For example, in one such embodiment, the surface of the plasma thermal shield 900 shown in the top view is the surface exposed to a plasma during processing. The surface of the top view includes a first upper surface region 902 which is raised above a second upper surface region 904. The first and second upper surfaces 902 and 904, respectively, are coupled by a sloping region 906.

[0074] Referring to the bottom view of Figure 9, the plasma thermal shield 900 has a bottom surface that is not exposed to a plasma during processing. The surface of the bottom view includes a first lower surface region 912 which is below a second lower surface region 914. The first and second lower surfaces 912 and 914, respectively, are coupled by a sloping region 916. In general, from a high level view, in an embodiment, the bottom surface of the plasma thermal shield 900 reciprocates the general topography of the upper surface. However, as described in association with Figure 10, some regions of the bottom surface of the plasma thermal shield 900 may be removed for heat dissipating applications.

[0075] Figure 10 illustrates an enlarged angled cross-sectional view of the plasma thermal shield 900 of Figure 9 as positioned on a top surface of a shadow ring 1000, in accordance with an embodiment of the present invention.

[0076] Referring to Figure 10, the plasma thermal shield 900 is nested on an upper surface of a shadow ring 1000 (which, in an embodiment, is an actively-cooled shadow ring as described in association with Figures 6-8). The upper surface portions 902, 904 and 906 are as described above with respect to Figure 9. However, in the enlarged view of Figure 10, it can be seen that the bottom surface portions 912, 914 and 916 of the plasma thermal shield 900 have recessed portions therein. In the particular example shown in Figure 10, a first gap or cavity 1052 is formed between regions 914 and 916 of the bottom surface, and a second gap or cavity 1052 is formed between regions 912 and 916 of the bottom surface. The effect is to leave

remaining three protruding portions or contact features 1050 that raise a majority of the bottom surface of the plasma thermal shield 900 off of the top surface of the shadow ring 1000. In an embodiment, the three protruding portions or contact features 1050 run the entire annular length to provide nesting support for the plasma thermal shield 900 when nested on the upper surface of the shadow ring 1000.

[0077] In an embodiment, the three protruding portions or contact features 1050 raise the majority of the bottom surface of the plasma thermal shield 900 off of the top surface of the shadow ring 1000 by a height of approximately $1/16^{th}$ of an inch. Thus, first and second gaps or cavities 1052 have a height of approximately $1/16^{th}$ of an inch. In one such embodiment, the thinned regions of surfaces 914 and 912 have a remaining thickness of approximately $1/16^{th}$ of an inch. It is to be appreciated, however, that the size of the gaps or cavities 1052 (as a height dimension) provide a trade-off between distancing heat from an underlying shadow ring versus having sufficient material in the plasma thermal shield for absorbing heat. Thus, the height of the gaps can be varied by application. Furthermore, the extent and locations of the recessed portions between protruding or contact portions 1050 are subject to the same trade-off. In one embodiment, an amount of surface area of the bottom surface of the plasma thermal shield 900 that is recessed is approximately in the range of 85 - 92 %. In an embodiment, the plasma thermal shield 900 is composed of a material such as, but not limited to, alumina (Al_2O_3), yttria (Y_2O_3), silicon nitride (SiN) or silicon carbide (SiC). In one embodiment, the plasma thermal shield 900 is composed of a process sensitive material and can act as a source of dopant for a plasma process. In an embodiment, the plasma thermal shield 900 can be viewed as an external device used to prevent contact of an underlying shadow ring with a hot surface or to act as a heat deflector for the underlying shadow ring.

[0078] In an embodiment, the plasma thermal shield 900 and the shadow ring 1000 are installed as two separate components. In one embodiment, both the shadow ring 1000 surface and the plasma thermal shield 900 barrier are composed of alumina, where the plasma thermal shield 900 provides heat dissipation away from the surface of the shadow ring 1000 even though the materials are the same. In an embodiment, the plasma thermal shield 900 blocks heat transfer to the shadow ring 1000 which is in contact with a tape frame of a substrate or wafer carrier. In an embodiment, with respect to power distribution, an open area of tape from the carrier may be positioned below the thinnest section of the shadow ring 1000. The consequential lowest mass region of the shadow ring 1000 is may be the highest in temperature. Accordingly, in an embodiment, the plasma thermal shield 900 is designed to

have greater mass and smaller gap in this region relative to the remainder of the plasma thermal shield 900, i.e., greater proportional mass is added to the tape region of the carrier.

[0079] Thus, in an embodiment, a plasma thermal shield is cross-sectionally a shell of ceramic located on top of an existing shadow ring. In one embodiment, the material of the plasma thermal shield is the same material as the shadow ring and covers the entire top surface of the shadow ring. The top surface of the plasma thermal shield may or may not be conformal to the shadow ring below. In one embodiment, the top surface of a plasma thermal shield is a continuous surface and the underside has removed areas of material to reduce conduction to the shadow ring. In an embodiment, the contact points between a plasma thermal shield and shadow ring are related to prohibiting plasma into removed areas as well as installation alignment. It is to be appreciated that the removed area cannot be so great as to create a significant plasma in the removed areas. In the plasma environment, the heat generated by the plasma is transferred to the plasma thermal shield. The plasma thermal shield increase in temperature heats up and radiates the heat to the shadow ring below. However, the shadow ring is heated only by radiated energy from the plasma thermal shield and not by direct plasma contact.

[0080] In an embodiment, a plasma thermal shield is a single passive part. The shape and material of the plasma thermal shield can be modified for different process conditions. In an embodiment, the plasma thermal shield can be used to reduce the temperature of a shadow ring by a factor in the range of 100 – 120 degrees Celsius. The plasma thermal shield may also be used as a differentiated material cover for process chemistry modification, essentially providing a dopant source to the plasma process.

[0081] In an embodiment, a plasma thermal shield is used together with an actively-cooled shadow ring. Thus, possible assemblies described herein for protecting a substrate or wafer carrier during plasma processing include an actively-cooled shadow ring, a shadow ring having a plasma thermal shield thereon, or an actively-cooled shadow ring having a plasma thermal shield thereon. In all three scenarios, from a plan view perspective, a protective annular ring with exposing inner region is provided for plasma processing of the carrier. In an embodiment, a cooling concentric chuck ring or cooling enlarged chuck is implemented in conjunction with one of the above three scenarios.

[0082] In an aspect of the present invention, an etch reactor is configured to accommodate etching of a thin wafer or substrate supported by a substrate carrier. For example, Figure 11 illustrates a cross-sectional view of an etch reactor, in accordance with an embodiment of the present invention.

[0083] Referring to Figure 11, an etch reactor 1100 includes a chamber 1102. An end effector 1104 is included for transferring a substrate carrier 1106 to and from chamber 1102. An inductively coupled plasma (ICP) source 1108 is positioned in an upper portion of the chamber 1102. The chamber 1102 is further equipped with a throttle valve 1110 and a turbo molecular pump 1112. The etch reactor 1100 also includes a cathode assembly 1114 (e.g., an assembly including an etch cathode or etch electrode). In one such embodiment, the cathode assembly 1114 includes a cooling concentric chuck ring and chuck pairing or includes a cooling enlarged chuck.

[0084] A shadow ring assembly 1115 is included above the region accommodating the substrate or wafer carrier 1106. In an embodiment, the shadow ring assembly 1115 includes a tape frame lift. In an embodiment, the shadow ring assembly 1115 is one of an actively-cooled shadow ring, a shadow ring having a plasma thermal shield thereon, or an actively-cooled shadow ring having a plasma thermal shield thereon. A shadow ring actuator 1118 may be included for moving the shadow ring. In one such embodiment, the shadow ring actuator 1118 moves a single lift hoop that is coupled to a tape frame lift and a shadow ring. Other actuators, such as actuator 1116 may also be included.

[0085] In an embodiment, the end effector 1104 is a robot blade sized for handling a substrate carrier. In one such embodiment, the robotic end effector 1104 supports a film frame assembly (e.g., substrate carrier 300) during transfer to and from an etch reactor under sub-atmospheric pressure (vacuum). The end effector 1104 includes features to support the substrate carrier in the X-Y-Z axis with gravity-assist. The end effector 1104 also includes a feature to calibrate and center the end effector with respect to circular features of a processing tool (e.g., an etch cathode center, or a center of a circular silicon wafer).

[0086] In one embodiment, an etch electrode of the cathode assembly 1114 is configured to allow RF and thermal coupling with the substrate carrier to enable plasma etching. In one such embodiment, the cathode assembly includes a cooling enlarged chuck. However, in an embodiment, the etch electrode only contacts a backing tape portion of a substrate carrier and not the frame of the substrate carrier. In one such embodiment, the cathode assembly includes a cooling concentric chuck ring surrounding the etch electrode or chuck (which may also be cooled).

[0087] In an embodiment, the shadow ring 1115 includes a protective annular ring, a lift hoop, and three supporting pins coupled between the lift hoop and the protective annular ring, as described in association with Figure 6. The lift hoop is disposed in a processing volume radially outwards of a supporting assembly. The lift hoop is mounted on shaft in a

substantially horizontal orientation. The shaft is driven by an actuator to move the lift hoop vertically in the processing volume. The three supporting pins extend upward from the lift hoop and position the protective annular ring above the supporting assembly. The three supporting pins may fixedly attach the protective annular ring to the lift hoop. The protective annular ring moves vertically with the lift hoop in the processing volume so that the protective annular ring can be positioned at a desired distance above a substrate and/or an exterior substrate handling device (such as a substrate carrier) can enter the processing volume between the protective annular ring and the supporting assembly to transfer the substrate. The three supporting pins may be positioned to allow the substrate carrier to be transferred in and out of a processing chamber between the supporting pins.

[0088] In another aspect, Figure 12 is a Flowchart 1200 representing operations in a method of dicing a semiconductor wafer including a plurality of integrated circuits, in accordance with an embodiment of the present invention. Figures 13A-13C illustrate cross-sectional views of a semiconductor wafer including a plurality of integrated circuits during performing of a method of dicing the semiconductor wafer, corresponding to operations of Flowchart 1200, in accordance with an embodiment of the present invention.

[0089] Referring to optional operation 1202 of Flowchart 1200, and corresponding Figure 13A, a mask 1302 is formed above a semiconductor wafer or substrate 1304. The mask 1302 is composed of a layer covering and protecting integrated circuits 1306 formed on the surface of semiconductor wafer 1304. The mask 1302 also covers intervening streets 1307 formed between each of the integrated circuits 1306. The semiconductor wafer or substrate 1304 is supported by a substrate carrier 1314.

[0090] In an embodiment, the substrate carrier 1314 includes a layer of backing tape, a portion of which is depicted as 1314 in Figure 13A, surrounded by a tape ring or frame (not shown). In one such embodiment, the semiconductor wafer or substrate 1304 is disposed on a die attach film 1316 disposed on the substrate carrier 1314, as is depicted in Figure 13A.

[0091] In accordance with an embodiment of the present invention, forming the mask 1302 includes forming a layer such as, but not limited to, a photo-resist layer or an I-line patterning layer. For example, a polymer layer such as a photo-resist layer may be composed of a material otherwise suitable for use in a lithographic process. In one embodiment, the photo-resist layer is composed of a positive photo-resist material such as, but not limited to, a 248 nanometer (nm) resist, a 193 nm resist, a 157 nm resist, an extreme ultra-violet (EUV) resist, or a phenolic resin matrix with a diazonaphthoquinone sensitizer. In another embodiment, the

photo-resist layer is composed of a negative photo-resist material such as, but not limited to, poly-cis-isoprene and poly-vinyl-cinnamate.

[0092] In another embodiment, the mask 1302 is a water-soluble mask layer. In an embodiment, the water-soluble mask layer is readily dissolvable in an aqueous media. For example, in one embodiment, the water-soluble mask layer is composed of a material that is soluble in one or more of an alkaline solution, an acidic solution, or in deionized water. In an embodiment, the water-soluble mask layer maintains its water solubility upon exposure to a heating process, such as heating approximately in the range of 50 – 160 degrees Celsius. For example, in one embodiment, the water-soluble mask layer is soluble in aqueous solutions following exposure to chamber conditions used in a laser and plasma etch singulation process. In one embodiment, the water-soluble mask layer is composed of a material such as, but not limited to, polyvinyl alcohol, polyacrylic acid, dextran, polymethacrylic acid, polyethylene imine, or polyethylene oxide. In a specific embodiment, the water-soluble mask layer has an etch rate in an aqueous solution approximately in the range of 1 – 15 microns per minute and, more particularly, approximately 1.3 microns per minute.

[0093] In another embodiment, the mask 1302 is a UV-curable mask layer. In an embodiment, the mask layer has a susceptibility to UV light that reduces an adhesiveness of the UV-curable layer by at least approximately 80%. In one such embodiment, the UV layer is composed of polyvinyl chloride or an acrylic-based material. In an embodiment, the UV-curable layer is composed of a material or stack of materials with an adhesive property that weakens upon exposure to UV light. In an embodiment, the UV-curable adhesive film is sensitive to approximately 365nm UV light. In one such embodiment, this sensitivity enables use of LED light to perform a cure.

[0094] In an embodiment, the semiconductor wafer or substrate 1304 is composed of a material suitable to withstand a fabrication process and upon which semiconductor processing layers may suitably be disposed. For example, in one embodiment, semiconductor wafer or substrate 1304 is composed of a group IV-based material such as, but not limited to, crystalline silicon, germanium or silicon/germanium. In a specific embodiment, providing semiconductor wafer 1304 includes providing a monocrystalline silicon substrate. In a particular embodiment, the monocrystalline silicon substrate is doped with impurity atoms. In another embodiment, semiconductor wafer or substrate 1304 is composed of a III-V material such as, e.g., a III-V material substrate used in the fabrication of light emitting diodes (LEDs).

[0095] In an embodiment, the semiconductor wafer or substrate 1304 has a thickness of approximately 300 microns or less. For example, in one embodiment, a bulk single-crystalline

silicon substrate is thinned from the backside prior to being affixed to the die attach film 1316. The thinning may be performed by a backside grind process. In one embodiment, the bulk single-crystalline silicon substrate is thinned to a thickness approximately in the range of 50 – 300 microns. It is important to note that, in an embodiment, the thinning is performed prior to a laser ablation and plasma etch dicing process. In an embodiment, the die attach film 1316 (or any suitable substitute capable of bonding a thinned or thin wafer or substrate to the substrate carrier 1314) has a thickness of approximately 20 microns.

[0096] In an embodiment, the semiconductor wafer or substrate 1304 has disposed thereon or therein, as a portion of the integrated circuits 1306, an array of semiconductor devices. Examples of such semiconductor devices include, but are not limited to, memory devices or complimentary metal-oxide-semiconductor (CMOS) transistors fabricated in a silicon substrate and encased in a dielectric layer. A plurality of metal interconnects may be formed above the devices or transistors, and in surrounding dielectric layers, and may be used to electrically couple the devices or transistors to form the integrated circuits 1306. Materials making up the streets 1307 may be similar to or the same as those materials used to form the integrated circuits 1306. For example, streets 1307 may be composed of layers of dielectric materials, semiconductor materials, and metallization. In one embodiment, one or more of the streets 1307 includes test devices similar to the actual devices of the integrated circuits 1306.

[0097] Referring to optional operation 1204 of Flowchart 1200, and corresponding Figure 13B, the mask 1302 is patterned with a laser scribing process to provide a patterned mask 1308 with gaps 1310, exposing regions of the semiconductor wafer or substrate 1304 between the integrated circuits 1306. In one such embodiment, the laser scribing process is a femtosecond-based laser scribing process. The laser scribing process is used to remove the material of the streets 1307 originally formed between the integrated circuits 1306. In accordance with an embodiment of the present invention, patterning the mask 1302 with the laser scribing process includes forming trenches 1312 partially into the regions of the semiconductor wafer 1304 between the integrated circuits 1306, as is depicted in Figure 13B.

[0098] In an embodiment, patterning the mask 1302 with the laser scribing process includes using a laser having a pulse width in the femtosecond range. Specifically, a laser with a wavelength in the visible spectrum plus the ultra-violet (UV) and infra-red (IR) ranges (totaling a broadband optical spectrum) may be used to provide a femtosecond-based laser, i.e., a laser with a pulse width on the order of the femtosecond (10^{-15} seconds). In one embodiment, ablation is not, or is essentially not, wavelength dependent and is thus suitable for

complex films such as films of the mask 1302, the streets 1307 and, possibly, a portion of the semiconductor wafer or substrate 1304.

[0099] Figure 14 illustrates the effects of using a laser pulse in the femtosecond range versus longer frequencies, in accordance with an embodiment of the present invention. Referring to Figure 14, by using a laser with a pulse width in the femtosecond range heat damage issues are mitigated or eliminated (e.g., minimal to no damage 1402C with femtosecond processing of a via 1400C) versus longer pulse widths (e.g., damage 1402B with picosecond processing of a via 1400B and significant damage 1402A with nanosecond processing of a via 1400A). The elimination or mitigation of damage during formation of via 1400C may be due to a lack of low energy recoupling (as is seen for picosecond-based laser ablation) or thermal equilibrium (as is seen for nanosecond-based laser ablation), as depicted in Figure 14.

[00100] Laser parameters selection, such as pulse width, may be critical to developing a successful laser scribing and dicing process that minimizes chipping, microcracks and delamination in order to achieve clean laser scribe cuts. The cleaner the laser scribe cut, the smoother an etch process that may be performed for ultimate die singulation. In semiconductor device wafers, many functional layers of different material types (e.g., conductors, insulators, semiconductors) and thicknesses are typically disposed thereon. Such materials may include, but are not limited to, organic materials such as polymers, metals, or inorganic dielectrics such as silicon dioxide and silicon nitride.

[00101] By contrast, if non-optimal laser parameters are selected, in a stacked structure that involves, e.g., two or more of an inorganic dielectric, an organic dielectric, a semiconductor, or a metal, a laser ablation process may cause delamination issues. For example, a laser penetrate through high bandgap energy dielectrics (such as silicon dioxide with an approximately of 9eV bandgap) without measurable absorption. However, the laser energy may be absorbed in an underlying metal or silicon layer, causing significant vaporization of the metal or silicon layers. The vaporization may generate high pressures to lift-off the overlying silicon dioxide dielectric layer and potentially causing severe interlayer delamination and microcracking. In an embodiment, while picoseconds-based laser irradiation processes lead to microcracking and delaminating in complex stacks, femtosecond-based laser irradiation processes have been demonstrated to not lead to microcracking or delamination of the same material stacks.

[00102] In order to be able to directly ablate dielectric layers, ionization of the dielectric materials may need to occur such that they behave similar to a conductive material by strongly

absorbing photons. The absorption may block a majority of the laser energy from penetrating through to underlying silicon or metal layers before ultimate ablation of the dielectric layer. In an embodiment, ionization of inorganic dielectrics is feasible when the laser intensity is sufficiently high to initiate photon-ionization and impact ionization in the inorganic dielectric materials.

[00103] In accordance with an embodiment of the present invention, suitable femtosecond-based laser processes are characterized by a high peak intensity (irradiance) that usually leads to nonlinear interactions in various materials. In one such embodiment, the femtosecond laser sources have a pulse width approximately in the range of 10 femtoseconds to 500 femtoseconds, although preferably in the range of 100 femtoseconds to 400 femtoseconds. In one embodiment, the femtosecond laser sources have a wavelength approximately in the range of 1570 nanometers to 200 nanometers, although preferably in the range of 540 nanometers to 250 nanometers. In one embodiment, the laser and corresponding optical system provide a focal spot at the work surface approximately in the range of 3 microns to 15 microns, though preferably approximately in the range of 5 microns to 10 microns.

[00104] The spacial beam profile at the work surface may be a single mode (Gaussian) or have a shaped top-hat profile. In an embodiment, the laser source has a pulse repetition rate approximately in the range of 200 kHz to 10 MHz, although preferably approximately in the range of 500kHz to 5MHz. In an embodiment, the laser source delivers pulse energy at the work surface approximately in the range of 0.5 uJ to 100 uJ, although preferably approximately in the range of 1uJ to 5uJ. In an embodiment, the laser scribing process runs along a work piece surface at a speed approximately in the range of 500mm/sec to 5m/sec, although preferably approximately in the range of 600mm/sec to 2m/sec.

[00105] The scribing process may be run in single pass only, or in multiple passes, but, in an embodiment, preferably 1-2 passes. In one embodiment, the scribing depth in the work piece is approximately in the range of 5 microns to 50 microns deep, preferably approximately in the range of 10 microns to 20 microns deep. The laser may be applied either in a train of single pulses at a given pulse repetition rate or a train of pulse bursts. In an embodiment, the kerf width of the laser beam generated is approximately in the range of 2 microns to 15 microns, although in silicon wafer scribing/dicing preferably approximately in the range of 6 microns to 10 microns, measured at the device/silicon interface.

[00106] Laser parameters may be selected with benefits and advantages such as providing sufficiently high laser intensity to achieve ionization of inorganic dielectrics (e.g., silicon dioxide) and to minimize delamination and chipping caused by underlayer damage prior

to direct ablation of inorganic dielectrics. Also, parameters may be selected to provide meaningful process throughput for industrial applications with precisely controlled ablation width (e.g., kerf width) and depth. As described above, a femtosecond-based laser is far more suitable to providing such advantages, as compared with picosecond-based and nanosecond-based laser ablation processes. However, even in the spectrum of femtosecond-based laser ablation, certain wavelengths may provide better performance than others. For example, in one embodiment, a femtosecond-based laser process having a wavelength closer to or in the UV range provides a cleaner ablation process than a femtosecond-based laser process having a wavelength closer to or in the IR range. In a specific such embodiment, a femtosecond-based laser process suitable for semiconductor wafer or substrate scribing is based on a laser having a wavelength of approximately less than or equal to 540 nanometers. In a particular such embodiment, pulses of approximately less than or equal to 400 femtoseconds of the laser having the wavelength of approximately less than or equal to 540 nanometers are used. However, in an alternative embodiment, dual laser wavelengths (e.g., a combination of an IR laser and a UV laser) are used.

[00107] Referring to optional operation 1206 of Flowchart 1200, a portion of the substrate is covered with a protective cover, e.g., to protect a tape and tape frame of the substrate carrier 1314 during plasma etching. In one embodiment, the protective cover is a shadow ring that leaves exposed a portion of, but not all of, the semiconductor wafer or substrate 1304, as described above in association with Figure 5.

[00108] Referring to operation 1208 of Flowchart 1200, the tape frame of the substrate carrier 1314 is supported by a cooling concentric chuck ring and chuck pairing or a cooling enlarged chuck. In one such embodiment, a cooling concentric chuck ring and chuck pairing or a cooling enlarged chuck such as described above in association with Figure 4 is used to support the tape frame of the substrate carrier 1314 below a shadow mask. In one embodiment, the shadow mask is a low contact shadow mask. In one embodiment, the cooling is achieved from below the substrate and tape frame by flowing a coolant through the cooling concentric chuck ring and chuck pairing or a cooling enlarged chuck.

[00109] Referring again to operations 1206 and 1208, in accordance with an optional embodiment of the present invention, a portion of the substrate carrier 1314 is covered with an actively-cooled shadow ring or a plasma thermal shield, or both, in preparation for an etch portion of the dicing process. In one embodiment, the actively-cooled shadow ring or a plasma thermal shield, or both, is included in a plasma etching chamber.

[00110] Referring to operation 1210 of Flowchart 1200, and corresponding Figure 13C, the semiconductor wafer or substrate 1304 is then etched through the gaps 1310 in the patterned mask 1308 to singulate the integrated circuits 1306. In accordance with an embodiment of the present invention, etching the semiconductor wafer 1304 includes etching to extend the trenches 1312 formed with the laser scribing process and to ultimately etch entirely through semiconductor wafer or substrate 1304, as depicted in Figure 13C.

[00111] In an embodiment, etching the semiconductor wafer or substrate 1304 includes using a plasma etching process. In one embodiment, a through-silicon via type etch process is used. For example, in a specific embodiment, the etch rate of the material of semiconductor wafer or substrate 1304 is greater than 25 microns per minute. An ultra-high-density plasma source may be used for the plasma etching portion of the die singulation process. An example of a process chamber suitable to perform such a plasma etch process is the Applied Centura® Silvia™ Etch system available from Applied Materials of Sunnyvale, CA, USA. The Applied Centura® Silvia™ Etch system combines the capacitive and inductive RF coupling ,which gives much more independent control of the ion density and ion energy than was possible with the capacitive coupling only, even with the improvements provided by magnetic enhancement. The combination enables effective decoupling of the ion density from ion energy, so as to achieve relatively high density plasmas without the high, potentially damaging, DC bias levels, even at very low pressures. An exceptionally wide process window results. However, any plasma etch chamber capable of etching silicon may be used. In an exemplary embodiment, a deep silicon etch is used to etch a single crystalline silicon substrate or wafer 1304 at an etch rate greater than approximately 40% of conventional silicon etch rates while maintaining essentially precise profile control and virtually scallop-free sidewalls. In a specific embodiment, a through-silicon via type etch process is used. The etch process is based on a plasma generated from a reactive gas, which generally a fluorine-based gas such as SF_6, C_4F_8, CHF_3, XeF_2, or any other reactant gas capable of etching silicon at a relatively fast etch rate. In one embodiment, however, a Bosch process is used which involves formation of a scalloped profile.

[00112] In an embodiment, singulation may further include patterning of die attach film 1316. In one embodiment, die attach film 1316 is patterned by a technique such as, but not limited to, laser ablation, dry (plasma) etching or wet etching. In an embodiment, the die attach film 1316 is patterned in sequence following the laser scribe and plasma etch portions of the singulation process to provide die attach film portions 1318, as depicted in Figure 13C. In an embodiment, the patterned mask 1308 is removed after the laser scribe and plasma etch

portions of the singulation process, as is also depicted in Figure 13C. The patterned mask 1308 may be removed prior to, during, or following patterning of the die attach film 1316. In an embodiment, the semiconductor wafer or substrate 1304 is etched while supported by the substrate carrier 1314. In an embodiment, the die attach film 1316 is also patterned while disposed on the substrate carrier 1314.

[00113] Accordingly, referring again to Flowchart 1200 and Figures 13A-13C, wafer dicing may be preformed by initial laser ablation through a mask, through wafer streets (including metallization), and partially into a silicon substrate. The laser pulse width may be selected in the femtosecond range. Die singulation may then be completed by subsequent through-silicon deep plasma etching. In one embodiment, a cooling concentric chuck ring and chuck pairing or a cooling enlarged chuck is implemented during the etch portion of the dicing process. In one same or different embodiment, an actively-cooled shadow ring or a plasma thermal shield, or both, are implemented during the etch portion of the dicing process. Additionally, removal of exposed portions of the die attach film is performed to provide singulated integrated circuits, each having a portion of a die attach film thereon. The individual integrated circuits, including die attach film portions may then be removed from the substrate carrier 1314, as depicted in Figure 13C. In an embodiment, the singulated integrated circuits are removed from the substrate carrier 1314 for packaging. In one such embodiment, the patterned die attach film 1318 is retained on the backside of each integrated circuit and included in the final packaging. However, in another embodiment, the patterned die attach film 1314 is removed during or subsequent to the singulation process.

[00114] Referring again to Figures 13A-13C, the plurality of integrated circuits 1306 may be separated by streets 1307 having a width of approximately 10 microns or smaller. The use of a laser scribing approach (such as a femtosecond-based laser scribing approach) may enable such compaction in a layout of integrated circuits, at least in part due to the tight profile control of the laser. For example, Figure 15 illustrates compaction on a semiconductor wafer or substrate achieved by using narrower streets versus conventional dicing which may be limited to a minimum width, in accordance with an embodiment of the present invention.

[00115] Referring to Figure 15, compaction on a semiconductor wafer is achieved by using narrower streets (e.g., widths of approximately 10 microns or smaller in layout 1502) versus conventional dicing which may be limited to a minimum width (e.g., widths of approximately 70 microns or larger in layout 1500). It is to be understood, however, that it may not always be desirable to reduce the street width to less than 10 microns even if otherwise enabled by a femtosecond-based laser scribing process. For example, some applications may

require a street width of at least 40 microns in order to fabricate dummy or test devices in the streets separating the integrated circuits.

[00116] Referring again to Figures 13A-13C, the plurality of integrated circuits 1306 may be arranged on semiconductor wafer or substrate 1304 in a non-restricted layout. For example, Figure 16 illustrates a freeform integrated circuit arrangement allowing denser packing. The denser packing may provide for more die per wafer versus grid alignment approaches, in accordance with an embodiment of the present invention. Referring to Figure 16, a freeform layout (e.g., a non-restricted layout on semiconductor wafer or substrate 1602) allows denser packing and hence more die per wafer versus grid alignment approaches (e.g., a restricted layout on semiconductor wafer or substrate 1600). In an embodiment, the speed of the laser ablation and plasma etch singulation process is independent of die size, layout or the number of streets.

[00117] A single process tool may be configured to perform many or all of the operations in a hybrid laser ablation and plasma etch singulation process. For example, Figure 17 illustrates a block diagram of a tool layout for laser and plasma dicing of wafers or substrates, in accordance with an embodiment of the present invention.

[00118] Referring to Figure 17, a process tool 1700 includes a factory interface 1702 (FI) having a plurality of load locks 1704 coupled therewith. A cluster tool 1706 is coupled with the factory interface 1702. The cluster tool 1706 includes one or more plasma etch chambers, such as plasma etch chamber 1708. A laser scribe apparatus 1710 is also coupled to the factory interface 1702. The overall footprint of the process tool 1700 may be, in one embodiment, approximately 3500 millimeters (3.5 meters) by approximately 3800 millimeters (3.8 meters), as depicted in Figure 17.

[00119] In an embodiment, the laser scribe apparatus 1710 houses a femtosecond-based laser. The femtosecond-based laser may be suitable for performing a laser ablation portion of a hybrid laser and etch singulation process, such as the laser abalation processes described above. In one embodiment, a moveable stage is also included in laser scribe apparatus 1700, the moveable stage configured for moving a wafer or substrate (or a carrier thereof) relative to the femtosecond-based laser. In a specific embodiment, the femtosecond-based laser is also moveable. The overall footprint of the laser scribe apparatus 1710 may be, in one embodiment, approximately 2240 millimeters by approximately 1270 millimeters, as depicted in Figure 17.

[00120] In an embodiment, the one or more plasma etch chambers 1708 is configured etching a wafer or substrate through the gaps in a patterned mask to singulate a plurality of integrated circuits. In one such embodiment, the one or more plasma etch chambers 1708 is

configured to perform a deep silicon etch process. In a specific embodiment, the one or more plasma etch chambers 1708 is an Applied Centura® Silvia™ Etch system, available from Applied Materials of Sunnyvale, CA, USA. The etch chamber may be specifically designed for a deep silicon etch used to create singulate integrated circuits housed on or in single crystalline silicon substrates or wafers. In an embodiment, a high-density plasma source is included in the plasma etch chamber 1708 to facilitate high silicon etch rates. In an embodiment, more than one etch chamber is included in the cluster tool 1706 portion of process tool 1700 to enable high manufacturing throughput of the singulation or dicing process. In accordance with an embodiment of the present invention, one or more of the etch chambers is equipped with a cooling concentric chuck ring and chuck pairing or a cooling enlarged chuck assembly. In one same or different embodiment, one or more of the etch chambers is equipped with an actively-cooled shadow ring or a plasma thermal shield, or both.

[00121] The factory interface 1702 may be a suitable atmospheric port to interface between an outside manufacturing facility with laser scribe apparatus 1710 and cluster tool 1706. The factory interface 1702 may include robots with arms or blades for transferring wafers (or carriers thereof) from storage units (such as front opening unified pods) into either cluster tool 1706 or laser scribe apparatus 1710, or both.

[00122] Cluster tool 1706 may include other chambers suitable for performing functions in a method of singulation. For example, in one embodiment, in place of an additional etch chamber, a deposition chamber 1712 is included. The deposition chamber 1712 may be configured for mask deposition on or above a device layer of a wafer or substrate prior to laser scribing of the wafer or substrate. In one such embodiment, the deposition chamber 1712 is suitable for depositing a water soluble mask layer. In another embodiment, in place of an additional etch chamber, a wet/dry station 1714 is included. The wet/dry station may be suitable for cleaning residues and fragments, or for removing a water soluble mask, subsequent to a laser scribe and plasma etch singulation process of a substrate or wafer. In an embodiment, a metrology station is also included as a component of process tool 1700.

[00123] Embodiments of the present invention may be provided as a computer program product, or software, that may include a machine-readable medium having stored thereon instructions, which may be used to program a computer system (or other electronic devices) to perform a process according to embodiments of the present invention. In one embodiment, the computer system is coupled with process tool 1700 described in association with Figure 17 or with etch chamber 1100 described in association with Figure 11. A machine-readable medium includes any mechanism for storing or transmitting information in a form readable by a

machine (e.g., a computer). For example, a machine-readable (e.g., computer-readable) medium includes a machine (e.g., a computer) readable storage medium (e.g., read only memory ("ROM"), random access memory ("RAM"), magnetic disk storage media, optical storage media, flash memory devices, etc.), a machine (e.g., computer) readable transmission medium (electrical, optical, acoustical or other form of propagated signals (e.g., infrared signals, digital signals, etc.)), etc.

[00124] Figure 18 illustrates a diagrammatic representation of a machine in the exemplary form of a computer system 1800 within which a set of instructions, for causing the machine to perform any one or more of the methodologies described herein, may be executed. In alternative embodiments, the machine may be connected (e.g., networked) to other machines in a Local Area Network (LAN), an intranet, an extranet, or the Internet. The machine may operate in the capacity of a server or a client machine in a client-server network environment, or as a peer machine in a peer-to-peer (or distributed) network environment. The machine may be a personal computer (PC), a tablet PC, a set-top box (STB), a Personal Digital Assistant (PDA), a cellular telephone, a web appliance, a server, a network router, switch or bridge, or any machine capable of executing a set of instructions (sequential or otherwise) that specify actions to be taken by that machine. Further, while only a single machine is illustrated, the term "machine" shall also be taken to include any collection of machines (e.g., computers) that individually or jointly execute a set (or multiple sets) of instructions to perform any one or more of the methodologies described herein.

[00125] The exemplary computer system 1800 includes a processor 1802, a main memory 1804 (e.g., read-only memory (ROM), flash memory, dynamic random access memory (DRAM) such as synchronous DRAM (SDRAM) or Rambus DRAM (RDRAM), etc.), a static memory 1806 (e.g., flash memory, static random access memory (SRAM), etc.), and a secondary memory 1818 (e.g., a data storage device), which communicate with each other via a bus 1830.

[00126] Processor 1802 represents one or more general-purpose processing devices such as a microprocessor, central processing unit, or the like. More particularly, the processor 1802 may be a complex instruction set computing (CISC) microprocessor, reduced instruction set computing (RISC) microprocessor, very long instruction word (VLIW) microprocessor, processor implementing other instruction sets, or processors implementing a combination of instruction sets. Processor 1802 may also be one or more special-purpose processing devices such as an application specific integrated circuit (ASIC), a field programmable gate array

(FPGA), a digital signal processor (DSP), network processor, or the like. Processor 1802 is configured to execute the processing logic 1826 for performing the operations described herein.

[00127] The computer system 1800 may further include a network interface device 1808. The computer system 1800 also may include a video display unit 1810 (e.g., a liquid crystal display (LCD), a light emitting diode display (LED), or a cathode ray tube (CRT)), an alphanumeric input device 1812 (e.g., a keyboard), a cursor control device 1814 (e.g., a mouse), and a signal generation device 1816 (e.g., a speaker).

[00128] The secondary memory 1818 may include a machine-accessible storage medium (or more specifically a computer-readable storage medium) 1832 on which is stored one or more sets of instructions (e.g., software 1822) embodying any one or more of the methodologies or functions described herein. The software 1822 may also reside, completely or at least partially, within the main memory 1804 and/or within the processor 1802 during execution thereof by the computer system 1800, the main memory 1804 and the processor 1802 also constituting machine-readable storage media. The software 1822 may further be transmitted or received over a network 1820 via the network interface device 1808.

[00129] While the machine-accessible storage medium 1832 is shown in an exemplary embodiment to be a single medium, the term "machine-readable storage medium" should be taken to include a single medium or multiple media (e.g., a centralized or distributed database, and/or associated caches and servers) that store the one or more sets of instructions. The term "machine-readable storage medium" shall also be taken to include any medium that is capable of storing or encoding a set of instructions for execution by the machine and that cause the machine to perform any one or more of the methodologies of the present invention. The term "machine-readable storage medium" shall accordingly be taken to include, but not be limited to, solid-state memories, and optical and magnetic media.

[00130] In accordance with an embodiment of the present invention, a machine-accessible storage medium has instructions stored thereon which cause a data processing system to perform a method of dicing a semiconductor wafer having a plurality of integrated circuits. The method involves introducing a substrate supported by a substrate carrier into a plasma etch chamber. The substrate has a patterned mask thereon covering integrated circuits and exposing streets of the substrate. The substrate carrier has a backside. The method also involves supporting at least a portion of the backside of the substrate carrier on a chuck of the plasma etch chamber. The method also involves cooling substantially all of the backside of the substrate carrier, the cooling involving cooling at least a first portion of the backside of the substrate carrier by the chuck. The method also involves plasma etching the substrate through

the streets to singulate the integrated circuits while performing the cooling substantially all of the backside of the substrate carrier.

[00131] Thus, methods of and apparatuses for dicing semiconductor wafers, each wafer having a plurality of integrated circuits, have been disclosed.

CLAIMS

1. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising: introducing a substrate supported by a substrate carrier into a plasma etch chamber, the substrate having a patterned mask thereon covering integrated circuits and exposing streets of the substrate, and the substrate carrier having a backside, wherein the substrate carrier comprises an outer tape frame and supporting dicing tape, and wherein the outer tape frame is thermally conductive; supporting at least a portion of the backside of the substrate carrier on a chuck of the plasma etch chamber; cooling substantially all of the backside of the substrate carrier, the cooling comprising cooling at least a first portion of the backside of the substrate carrier by the chuck, wherein cooling substantially all of the backside of the substrate carrier comprises cooling the tape frame and the substrate; and plasma etching the substrate through the streets to singulate the integrated circuits while performing the cooling substantially all of the backside of the substrate carrier; and wherein cooling substantially all of the backside of the substrate carrier, further comprises cooling the tape frame of the backside of the substrate carrier with a cooling concentric chuck ring surrounding the chuck.

2. The method of claim 1, wherein, during the plasma etching, the chuck is maintained at a temperature at least as low as approximately -10 degrees Celsius, and the cooling concentric chuck ring is maintained at a temperature approximately in the range of 0 to -10 degrees Celsius.

3. The method of claim 1, wherein the chuck has a supporting area at least as large as the backside of the substrate carrier, and wherein cooling substantially all of the backside of the substrate carrier comprises cooling substantially all of the backside of the substrate carrier with the chuck.

4. The method of claim 3, wherein, during the plasma etching, the chuck is maintained at a temperature at least as low as approximately -10 degrees Celsius.

5. The method of claim 1, wherein the dicing tape is disposed between the tape frame and a cooling concentric chuck ring surrounding the chuck, and between the substrate and the chuck.

6. The method of claim 1, wherein the dicing tape is disposed between the tape frame and the chuck, and between the substrate and the chuck.

7. The method of claim 1, wherein, during the plasma etching, a portion of a front side of the substrate carrier is protected by a shadow ring.

8. The method of claim 1, further comprising: forming the patterned mask with a laser scribing process.

9. A plasma etch chamber, comprising: a plasma source disposed in an upper region of the plasma etch chamber; a cooling chuck disposed below the plasma source, the cooling chuck for supporting a first portion of a substrate carrier; and a cooling concentric ring surrounding the cooling chuck, the cooling concentric ring for supporting a second portion of the substrate carrier, wherein, together, the cooling chuck and the cooling concentric ring are for cooling substantially all of a backside of the substrate carrier; further comprising a cooling concentric ring surrounding the cooling chuck, the cooling concentric ring supporting the tape frame, wherein, together, the cooling chuck and the cooling concentric ring are for cooling substantially all of a backside of the substrate carrier.

10. The plasma etch chamber of claim 9, wherein the cooling chuck is configured to be maintained at a temperature at least as low as approximately -10 degrees Celsius during plasma processing, and the cooling concentric chuck ring is configured to be maintained at a temperature approximately in the range of 0 to -10 degrees Celsius during plasma processing.

11. The plasma etch chamber of claim 9, further comprising: a shadow ring assembly configured to be positioned between the chuck and the plasma source during plasma processing.

12. The plasma etch chamber of claim 9, wherein the plasma etch chamber is housed in a cluster processing tool.

13. The plasma etch chamber of claim 9, wherein the cooling concentric ring and the cooling chuck together comprise a supporting area at least as large as the backside of the substrate carrier, the substrate carrier having an outer tape frame.

14. A plasma etch chamber, comprising: a plasma source disposed in an upper region of the plasma etch chamber; and a cooling chuck disposed below the plasma source, the cooling chuck for supporting and cooling substantially all of a backside of a substrate carrier, wherein the cooling chuck comprises a supporting area at least as large as the backside of the substrate carrier, the substrate carrier having an outer tape frame.

15. The plasma etch chamber of claim 14, wherein the cooling chuck is configured to be maintained at a temperature at least as low as approximately -10 degrees Celsius during plasma processing.

16. The plasma etch chamber of claim 14, further comprising: a shadow ring assembly configured to be positioned between the chuck and the plasma source during plasma processing.

17. The plasma etch chamber of claim 14, wherein the plasma etch chamber is housed in a cluster processing tool.