CLAIMS

1. An adaptive voltage modulation circuit, comprising: a supply voltage droop detection and mitigation circuit comprising: a detection circuit configured to generate a droop detection signal in an active state in response to a supply voltage provided to a load circuit being less than a droop threshold voltage; and a clock adjustment circuit configured to adjust a load clock signal provided to the load circuit in response to the droop detection signal; a supply voltage adjust circuit comprising: a counter circuit configured to increment a count in response to each cycle of a reference clock signal in which the droop detection signal is in an active state; a voltage adjust-up circuit configured to generate a voltage adjust-up signal in an active state in response to the count being greater than an adjust-up threshold value; and a voltage adjust-down circuit configured to generate a voltage adjust-down signal in an active state in response to the count being less than an adjust-down threshold value at an end of a defined period as measured by the reference clock signal; and a supply voltage controller circuit configured to: increase the supply voltage provided to the load circuit in response to the voltage adjust-up signal being in an active state; and decrease the supply voltage provided to the load circuit in response to the voltage adjust-down signal being in an active state.

2. The adaptive voltage modulation circuit of claim 1, wherein: the voltage adjust-up circuit is further configured to generate the voltage adjust-up signal in an inactive state in response to the count being less than the adjust-up threshold value at the end of the defined period; and the voltage adjust-down circuit is further configured to generate the voltage adjust-down signal in an inactive state in response to the count being greater than the adjust-down threshold value at the end of the defined period.

3. The adaptive voltage modulation circuit of claim 1, wherein: the voltage adjust-up circuit is further configured to generate the voltage adjust-up signal in an inactive state in response to an acknowledgement signal of the supply voltage controller circuit indicating that the supply voltage has been adjusted up; and the voltage adjust-down circuit is further configured to generate the voltage adjust-down signal in an inactive state in response to an acknowledgement signal of the supply voltage controller circuit indicating that the supply voltage has been adjusted down.

4. The adaptive voltage modulation circuit of claim 3, wherein the counter circuit is configured to reset the count to an initial count value in response to the acknowledgement signal of the supply voltage controller circuit indicating that the supply voltage has been adjusted up.

5. The adaptive voltage modulation circuit of claim 3, wherein the counter circuit is configured to reset the count to an initial count value in response to the acknowledgement signal of the supply voltage controller circuit indicating that the supply voltage has been adjusted down.

6. The adaptive voltage modulation circuit of claim 1, wherein the counter circuit is configured to reset the count to an initial count value in response to the end of the defined period.

7. The adaptive voltage modulation circuit of claim 1, wherein the counter circuit is further configured to: increment an adjust-up count in response to each cycle of the reference clock signal during an adjust-up period in which the droop detection signal is in an active state; and increment an adjust-down count in response to each cycle of the reference clock signal during an adjust-down period in which the droop detection signal is in an active state.

8. The adaptive voltage modulation circuit of claim 7, wherein the counter circuit comprises: a first input node; a second input node; a first output node; and a second output node; the counter circuit configured to: receive the droop detection signal on the first input node of the counter circuit; receive the reference clock signal on the second input node of the counter circuit; provide an up count signal indicating the adjust-up count on the first output node of the counter circuit; and provide a down count signal indicating the adjust-down count on the second output node of the counter circuit.

9. The adaptive voltage modulation circuit of claim 8, wherein the supply voltage adjust circuit further comprises: an adjust-up register comprising an output node and configured to: store the adjust-up threshold value; and provide the adjust-up threshold value on the output node of the adjust-up register; and an adjust-down register comprising an output node and configured to: store the adjust-down threshold value; and provide the adjust-down threshold value on the output node of the adjust-down register.

10. The adaptive voltage modulation circuit of claim 9, wherein: the voltage adjust-up circuit comprises: a first input node electrically coupled to the first output node of the counter circuit; a second input node electrically coupled to the output node of the adjust-up register; and an output node electrically coupled to a first input node of the supply voltage controller circuit; the voltage adjust-up circuit configured to provide the voltage adjust-up signal on the output node of the voltage adjust-up circuit; and the voltage adjust-down circuit comprises: a first input node electrically coupled to the second output node of the counter circuit; a second input node electrically coupled to the output node of the adjust-down register; and an output node electrically coupled to a second input node of the supply voltage controller circuit; the voltage

adjust-down circuit configured to provide the voltage adjust-down signal on the output node of the voltage adjust-down circuit.

11. The adaptive voltage modulation circuit of claim 1, wherein the supply voltage droop detection and mitigation circuit further comprises a droop threshold register comprising an output node and configured to: store a digital threshold signal that is a digital representation of the droop threshold voltage; and provide the digital threshold signal on the output node of the droop threshold register.

12. The adaptive voltage modulation circuit of claim 11, wherein the supply voltage droop detection and mitigation circuit further comprises: a digital-to-analog converter (DAC) comprising: an input node electrically coupled to the output node of the droop threshold register; and an output node; the DAC configured to provide the droop threshold voltage on the output node of the DAC; and wherein the detection circuit comprises a comparator circuit comprising: a first input node electrically coupled to the output node of the DAC; a second input node electrically coupled to the supply voltage; and an output node; the comparator circuit configured to provide the droop detection signal on the output node of the comparator circuit, wherein: the droop detection signal transitions to an active state in response to the droop threshold voltage being greater than the supply voltage; and the droop detection signal transitions to an inactive state in response to the droop threshold voltage being less than the supply voltage.

13. The adaptive voltage modulation circuit of claim 12, wherein the clock adjustment circuit comprises: a first input node that receives a root clock signal; a second input node electrically coupled to the output node of the comparator circuit; and an output node; the clock adjustment circuit configured to provide the load clock signal on the output node of the clock adjustment circuit, wherein the load clock signal is based on the root clock signal.

14. The adaptive voltage modulation circuit of claim 13, wherein the clock adjustment circuit is configured to adjust the load clock signal by being configured to: decrease a frequency of the load clock signal in response to the droop detection signal transitioning to an active state such that the frequency of the load clock signal is lower than a frequency of the root clock signal; and increase the frequency of the load clock signal in response to the droop detection signal transitioning to an inactive state such that the frequency of the load clock signal is equal or substantially equal to the frequency of the root clock signal.

15. The adaptive voltage modulation circuit of claim 1, wherein the detection circuit comprises a critical path voltage monitoring circuit powered by the supply voltage and comprising: a first path, comprising: a first flip flop circuit configured to be clocked by a root clock signal,

comprising: an input node; and an output node; a buffer, comprising: an input node electrically coupled to the output node of the first flip flop circuit; and an output node; an inverter, comprising: an input node electrically coupled to the output node of the buffer; and an output node; an AND-based gate, comprising: a first input node electrically coupled to the output node of the inverter; a second input node configured to receive an enable signal; and an output node electrically coupled to the output node of the first flip flop circuit; a second path, comprising: a second flip flop circuit configured to be clocked by the root clock signal, comprising: an input node electrically coupled to the output node of the AND-based gate; and an output node; and a plurality of serially connected buffers, wherein: a first buffer of the plurality of serially connected buffers comprises an input node electrically coupled to the output node of the second flip flop circuit; and a last buffer of the plurality of serially connected buffers comprises an output node; an XOR-based gate, comprising: a first input node electrically coupled to the output node of the buffer of the first path; a second input node electrically coupled to the output node of the last buffer of the plurality of serially connected buffers of the second path; and an output node on which the XOR-based gate is configured to provide an output signal; and a flip flop circuit configured to be clocked by the root clock signal, comprising: an input node electrically coupled to the output node of the XOR-based gate; and an output node on which the flip flop circuit is configured to provide the droop detection signal.

16. The adaptive voltage modulation circuit of claim 1 integrated into an integrated circuit (IC).

17. The adaptive voltage modulation circuit of claim 1 integrated into a device selected from the group consisting of: a set top box; an entertainment unit; a navigation device; a communications device; a fixed location data unit; a mobile location data unit; a global positioning system (GPS) device; a mobile phone; a cellular phone; a smart phone; a session initiation protocol (SIP) phone; a tablet; a phablet; a server; a computer; a portable computer; a mobile computing device; a wearable computing device; a desktop computer; a personal digital assistant (PDA); a monitor; a computer monitor; a television; a tuner; a radio; a satellite radio; a music player; a digital music player; a portable music player; a digital video player; a video player; a digital video disc (DVD) player; a portable digital video player; an automobile; a vehicle component; avionics systems; a drone; and a multicopter.

18. An adaptive voltage modulation circuit, comprising: a means for generating a droop detection signal in an active state in response to a supply voltage being less than a droop threshold voltage; a means for adjusting a load clock signal provided to a load circuit in response to the droop detection signal; a means for incrementing a count in response to each cycle of a reference clock signal in which the droop detection signal is in an active state; a means for generating a voltage adjust-up signal in an active state in response to the count being greater than an adjust-up threshold value; a means for generating a voltage adjust-down signal in an active state in response to the count being less than an adjust-down threshold value at an end of a

defined period as measured by the reference clock signal; a means for increasing the supply voltage provided to the load circuit in response to the voltage adjust-up signal being in an active state; and a means for decreasing the supply voltage provided to the load circuit in response to the voltage adjust-down signal being in an active state.

19. The adaptive voltage modulation circuit of claim 18, further comprising: a means for generating the voltage adjust-up signal in an inactive state in response to the count being less than the adjust-up threshold value at the end of the defined period; and a means for generating the voltage adjust-down signal in an inactive state in response to the count being greater than the adjust-down threshold value at the end of the defined period.

20. The adaptive voltage modulation circuit of claim 18, further comprising a means for resetting the count to an initial count value in response to the end of the defined period.

21. The adaptive voltage modulation circuit of claim 18, further comprising a means for generating the droop threshold voltage based on a digital threshold signal, wherein the digital threshold signal is a digital representation of the droop threshold voltage stored in a register in the adaptive voltage modulation circuit.

22. The adaptive voltage modulation circuit of claim 18, further comprising: a means for performing a comparison of the supply voltage to the droop threshold voltage; and a means for generating the droop detection signal in an inactive state in response to the droop threshold voltage being less than the supply voltage.

23. The adaptive voltage modulation circuit of claim 22, wherein the means for adjusting the load clock signal comprises: a means for decreasing a frequency of the load clock signal in response to the droop detection signal transitioning to an active state such that the frequency of the load clock signal is lower than a frequency of a root clock signal; and a means for increasing the frequency of the load clock signal in response to the droop detection signal transitioning to an inactive state such that the frequency of the load clock signal is equal or substantially equal to the frequency of the root clock signal.

24. A method for adaptively modulating a supply voltage, comprising: generating a droop detection signal in an active state in response to a supply voltage being less than a droop threshold voltage; adjusting a load clock signal provided to a load circuit in response to the droop detection signal; incrementing a count in response to each cycle of a reference clock signal in which the droop detection signal is in an active state; generating a voltage adjust-up signal in an

active state in response to the count being greater than an adjust-up threshold value; generating a voltage adjust-down signal in an active state in response to the count being less than an adjust-down threshold value at an end of a defined period as measured by the reference clock signal; increasing the supply voltage provided to the load circuit in response to the voltage adjust-up signal being in an active state; and decreasing the supply voltage provided to the load circuit in response to the voltage adjust-down signal being in an active state.

25. The method of claim 24, further comprising: generating the voltage adjust-up signal in an inactive state in response to the count being less than the adjust-up threshold value at the end of the defined period; and generating the voltage adjust-down signal in an inactive state in response to the count being greater than the adjust-down threshold value at the end of the defined period.

26. The method of claim 24, further comprising resetting the count to an initial count value in response to the end of the defined period.

27. The method of claim 24, further comprising generating the droop threshold voltage based on a digital threshold signal, wherein the digital threshold signal is a digital representation of the droop threshold voltage.

28. The method of claim 24, wherein generating the droop detection signal comprises: performing a comparison of the supply voltage to the droop threshold voltage; and generating the droop detection signal in an inactive state in response to the droop threshold voltage being less than the supply voltage.

29. The method of claim 28, wherein adjusting the load clock signal comprises: decreasing a frequency of the load clock signal in response to the droop detection signal being in an active state such that the frequency of the load clock signal is lower than a frequency of a root clock signal; and increasing the frequency of the load clock signal in response to the droop detection signal being in an inactive state such that the frequency of the load clock signal is equal or substantially equal to the frequency of the root clock signal.

30. A processor-based system, comprising: a processor; a power management circuit configured to provide a supply voltage to the processor; and an adaptive voltage modulation circuit comprising: a supply voltage droop detection and mitigation circuit comprising: a detection circuit configured to generate a droop detection signal in an active state in response to the supply voltage being less than a droop threshold voltage; and a clock adjustment circuit configured to adjust a load clock signal provided to the processor in response to the droop detection signal; a

supply voltage adjust circuit comprising: a counter circuit configured to increment a count in response to each cycle of a reference clock signal in which the droop detection signal is in an active state; a voltage adjust-up circuit configured to generate a voltage adjust-up signal in an active state in response to the count being greater than an adjust-up threshold value; and a voltage adjust-down circuit configured to generate a voltage adjust-down signal in an active state in response to the count being less than an adjust-down threshold value at an end of a defined period as measured by the reference clock signal; and a supply voltage controller circuit configured to: increase the supply voltage provided to the processor in response to the voltage adjust-up signal being in an active state; and decrease the supply voltage provided to the processor in response to the voltage adjust-down signal being in an active state.