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Abstract:

CACHE MEMORY CONTROL SYSTEM

A cache memory control system includes a circuit for clearing valid bits of data and address data, both of which are stored in a cache memory⁽²⁰⁾, a circuit⁽¹⁾ for outputting a signal representing valid bits are being cleared, and a circuit for changing the cache memory⁽²⁰⁾ from cache access status to cache bypass status in response to the signal representing that the valid bits are being cleared. (Fig. 1)

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