

ABSTRACT

Disclosed are semiconductor devices and their fabrication methods. The semiconductor device comprises a logic cell on a substrate, and a first metal layer on the logic cell. The first metal layer includes first and second power lines and first to third lower lines on first to third wiring tracks therebetween. The first to third wiring tracks extend in parallel in the first direction. The first lower line includes first and second lines spaced apart in the first direction from each other at a first distance. The third lower line includes third and fourth lines spaced apart in the first direction at a second distance. The first line has a first end facing the second line. The third line has a second end facing the fourth line. A curvature at the first end is substantially the same as that at the second end.

FIG. 3