CLAIMS

What is claimed is:

1. A method of forming a device comprising:

forming epitaxial silicon germanium on a substrate;

forming epitaxial silicon on the epitaxial silicon germanium;

patterning the epitaxial silicon disposed on the epitaxial silicon germanium to form fin structures;

forming spacers across and on the fin structures;

removing a portion of the fin structures from source/drain regions on the substrate, then forming source/drain structures on the source/drain regions, wherein the source/drain regions are adjacent the spacers; and

removing one of the silicon and the epitaxial silicon germanium layers from the fin structures disposed between the spacers.

2. The method of claim 1 further comprising wherein the structure comprises a portion of a gate all around nanowire device.

3. The method of claim 1 further comprising forming additional alternating layers of epitaxial silicon germanium on epitaxial silicon.

4. The method of claim 1 further comprising wherein the silicon is removed from the fin structure to form silicon germanium nanowire structures separated from each other by a gap.

5. The method of claim 1 further comprising wherein the silicon germanium is removed from the fin structure to form silicon nanowire structures separated from each other by a gap.

6. The method of claim 4 further comprising wherein a gate dielectric is formed around all sides of the silicon germanium nanowire structures.

7. The method of claim 5 further comprising wherein a gate dielectric is formed around all sides of the silicon nanowire structures.

8. The method of claim 6 further comprising wherein a gate electrode material is formed around the silicon germanium nanowire structures.

9. The method of claim 7 further comprising wherein a gate electrode material is formed around the silicon nanowire structures.

10. The method of claim 8 further comprising wherein a gate electrode material is formed around the silicon germanium nanowire structures.

11. The method of claim 9 further comprising wherein the gate electrode material comprises metal.

12. The method of claim 10 further comprising wherein the gate electrode material comprises metal.

13. The method of claim 9 further comprising wherein a trench contact couples to the source drain structure, and wherein the source drain structure comprises n+ doped silicon.

14. The method of claim 13 further comprising wherein a silicon epitaxial tip is disposed between the source/drain structure and the substrate.

15. The method of claim 9 further comprising wherein the device comprises a portion of an NMOS gate all around channel device.

16. The method of claim 9 further comprising wherein a trench contact couples to the source drain structure, wherein the source/drain structure comprises p+ silicon germanium.

17. The method of claim 16 wherein a silicon epitaxial tip is disposed between the source drain structure and the substrate.

18. The method of claim 17 wherein the device comprises a portion of a PMOS gate all around channel device, and wherein the silicon nanowires comprises strained silicon nanowires.

19. A method of forming a nanowire device comprising:

forming alternating layers of epitaxial silicon on epitaxial silicon germanium on a SOI substrate;

patterning the alternating layers to form fin structures;

forming spacers across and on the fin structures;

removing a portion of the fin structures from source/drain regions on the substrate, then forming source/drain structures on the source/drain regions, wherein the source/drain regions are adjacent the spacers; and

removing one of the silicon and the epitaxial silicon germanium layers from the fin structures disposed between the spacers.

20. The method of claim 19 further comprising wherein a bottom nanowire geometry of the fin structure is defined by controlling the etching of a bottom oxide portion of the SOI substrate.

21. The method of claim 20 further comprising wherein the bottom oxide is etched to form one nanowire and one trigate structure.

22. The method of claim 20 further comprising wherein the bottom oxide is etched to form two nanowires.

23. A method of forming a nanowire device comprising:

forming alternating layers of epitaxial silicon on epitaxial silicon germanium on a substrate;

forming fin structures by etching the alternating layers and forming trenches adjacent to the fin structures;

forming fin spacers on the fin structures;

performing a second trench etch to expose a bottom fin area of the fin structure;

oxidizing the bottom fin area;

forming spacers across and on the fin structures;

removing a portion of the fin structures from source/drain regions on the substrate, then forming source/drain structures on the source/drain regions, wherein the source/drain regions are adjacent the spacers; and

removing the silicon layers from the fin structures disposed between the spacers.

24. The method of claim 23 further comprising wherein a bottom nanowire is disposed on the oxidized bottom fin area.

25. A method of forming a nanowire device comprising:

forming alternating layers of epitaxial silicon on epitaxial silicon germanium on a substrate;

forming fin structures by etching the alternating layers and forming trenches adjacent to the fin structures;

forming oxide in the trenches;

forming fin spacers on the fin structures;

oxidizing a bottom fin area;

forming spacers across and on the fin structures;

removing a portion of the fin structures from source/drain regions on the substrate, and then forming source/drain structures on the source/drain regions, wherein the source/drain regions are adjacent the spacers; and

removing the epitaxial silicon layers from the fin structures disposed between the spacers.

26. The method of claim 25 wherein a bottom nanowire is disposed on the oxidized bottom fin area.

27. A method of forming a nanowire device comprising:

forming alternating layers of an epitaxial semiconductor material on epitaxial oxide material on a substrate;

forming fin structures by etching the alternating layers;

forming spacers across and on the fin structures;

removing a portion of the fin structures from source/drain regions on the substrate, then forming source/drain structures on the source/drain regions, wherein the source/drain regions are adjacent the spacers; and

removing a portion of the epitaxial oxide material from the fin structures disposed between the spacers.

28. The method of claim 27 wherein a bottom semiconductor material nanowire is disposed on the epitaxial oxide material.

29. The method of claim 27 wherein the epitaxial oxide is fully removed from the fin structures.

30. The method of claim 27 wherein the epitaxial oxide is partially removed from the fin structures.

31. A method of forming a nanowire device comprising:

forming alternating layers of an epitaxial silicon material on epitaxial silicon germanium material on a substrate;

forming fin structures by etching the alternating layers and forming trenches adjacent to the fin structures;

forming spacers across and on the fin structures;

removing a portion of the fin structures from source/drain regions on the substrate;

filling a gap in the spacers that is adjacent to the fin structures with a second spacer;

forming source/drain structures on the source/drain regions, wherein the source/drain regions are adjacent the spacers;

removing one of the silicon and the epitaxial silicon germanium layers from the fin structures disposed between the spacers.

32. The method of claim 31 wherein the second spacer material comprises at least one of a spacer like material and a low-k material.

33. The method of claim 31 further comprising wherein the gap in the spacers is filled on a source/drain side of the spacer.

34. The method of claim 31 further comprising wherein the gap in the spacers is filled on a gate side of the spacer.

35. A method of forming a nanowire device comprising:

forming alternating layers of an epitaxial silicon material on epitaxial silicon germanium material on a (100) substrate comprising a <111> channel;

forming fin structures by etching the alternating layers and forming trenches adjacent to the fin structures;

forming spacers across and on the fin structures;

removing a portion of the fin structures from source/drain regions on the substrate, and then forming source/drain structures on the source/drain regions, wherein the source/drain regions are adjacent the spacers;

removing the epitaxial silicon layers from the fin structures disposed between the spacers by using a wet etch that is selective to silicon and not to silicon germanium.

36. The method of claim 35 wherein silicon germanium nanowires are partially etched after removing all of the silicon between the SiGe nanowires of the fin structure.

37. The method of claim 36 wherein the wet etch comprises an anisotropic etch to minimize lateral etching within the spacers.

38. A method of forming a nanowire device comprising:

patterning alternating layers of nitride and oxide disposed on a silicon substrate to expose a back region and a trench region;

forming one of a silicon material and a silicon germanium material in the trench and back regions;

forming a hard mask on one of the silicon germanium and silicon;

forming a fin structure by removing a portion of the alternating layers of nitride and oxide not covered by the hard mask; and

forming nanowire structures by oxidizing the fin structure and then removing the oxidized portions.

39. The method of claim 38 further comprising wherein the nanowire structures are disposed across substantially all of the device.

40. A method of forming a nanowire device comprising:

patterning alternating layers of nitride and oxide disposed on a silicon substrate to expose a back region and a trench region;

forming one of a silicon material and a silicon germanium material in the trench and back regions;

forming a hard mask on one of the silicon germanium and silicon;

forming a forming a fin structure by removing a portion of the alternating layers of nitride and oxide not covered by the hard mask;

forming a second hard mask around the fin structure;

forming a gate region adjacent the fin structure, wherein a portion of the fin structure may be exposed;

forming nanowire structures by oxidizing the fin structure and then removing the oxidized portions.

41. The method of claim 40 further comprising wherein the nanowire structures are disposed only in the gate area.

42. The method of claim 40 further comprising wherein the oxidized portions of the fin structure is removed by:

etching the oxide with a wet etch; and

etching one of the silicon and silicon germanium with an anisotropic etch.

43. A nanowire device comprising:

a substrate;

a tall contact to couple with N and P nanowire channels,;

a short contact coupled to one of the N and P nanowire channels, wherein the N and P nanowire channels are disposed above the substrate; and

a bottom contact disposed below the short contact coupled to one of the N and P nanowire channels and the substrate.

44. The structure of claim 43 wherein the substrate comprises N+ inverter comprising for Vss

45. The structure of claim 43 wherein the short contact and the bottom contact are misaligned to one another.

46. The structure of claim 43 wherein the N and P nanowires comprise left and right wing structures.

47. A nanowire device structure comprising:

nanowire channel structures disposed vertically over a gate region of a CMOS device, wherein the nanowire channel structures comprise one of silicon nanowire and a silicon germanium nanowire.

48. The structure of claim 47 wherein the nanowire channel structures comprise a first nanowire disposed vertically over a second nanowire.

49. The structure of claim 47 wherein the nanowire channel structures are disposed over substantially the entire device structure.

50. A nanowire device comprising:

a substrate comprising source/drain structures disposed adjacent spacers; and

nanowire channel structures disposed between the spacers, wherein the nanowire channel structures are vertically stacked above each other.

51. The nanowire device of claim 50 wherein the nanowire channel structures comprise epitaxial silicon nanowire channel structures that are separated from each other by a gap.

52. The nanowire device of claim 50 wherein the nanowire channel structures comprise epitaxial silicon germanium nanowire channel structures that are separated from each other by a gap.

53. The nanowire device of claim 50 further comprising wherein the nanowire channel structures comprises a gate dielectric material all around the nanowire channel structures, and a metal gate surrounding the nanowire channel structures.

54. The nanowire device of claim 50 further comprising wherein the gate dielectric material comprises a high k gate dielectric material.

55. The nanowire device of claim 50 further comprising wherein the nanowire channel structures comprise one of epitaxial silicon and epitaxial silicon germanium.

56. The nanowire device of claim 50 further comprising wherein the source/drain structures comprise epitaxial silicon germanium.

57. The nanowire device of claim 50 wherein the substrate comprises a SOI substrate, and a bottom nanowire channel structure is disposed on an oxide portion of the SOI substrate.

58. The nanowire device of claim 50 wherein the substrate comprises a SOI substrate, and a bottom nanowire channel structure is disposed on an oxide portion of the SOI substrate.

59. The nanowire device of claim 50 wherein the device comprises an NMOS device, wherein a trench contact is coupled to the source drain structures, wherein the source drain structures comprise n+ doped silicon, and wherein a silicon epitaxial tip is disposed between the source drain structures and the substrate.

60. The nanowire device of claim 50 wherein the device comprises a PMOS device, wherein a trench contact couples to the source drain structures, which comprises p+ doped silicon germanium, and wherein a silicon epitaxial tip is disposed between the source drain structures and the substrate 100.

61. The nanowire device of claim 50 wherein the nanowire channel structures comprise an epitaxial silicon germanium nanowire channel disposed on an epitaxial oxide nanowire channel structure.

62. The nanowire device of claim 61 wherein the epitaxial oxide nanowire is partially etched.

CLAIMS

What is claimed is:

1. A method of forming a device comprising:

forming epitaxial silicon germanium on a substrate;

forming epitaxial silicon on the epitaxial silicon germanium;

patterning the epitaxial silicon disposed on the epitaxial silicon germanium to form fin structures;

forming a sacrificial gate electrode over said fin structures;

forming spacers adjacent to sidewalls of the sacrificial gate electrode and over the fin structures;

removing a semiconductor portion of the fin structures from source/drain regions on the substrate, then forming source/drain structures on the source/drain regions, wherein the source/drain regions are adjacent the spacers;

removing said sacrificial gate electrode from between the spacers; and

removing one of the silicon and the epitaxial silicon germanium layers from the fin structures disposed between the spacers.

2. The method of claim 1 further comprising wherein the device comprises a portion of a gate all around nanowire device.

3. The method of claim 1 further comprising forming additional alternating layers of epitaxial silicon germanium on epitaxial silicon.

4. The method of claim 3 further comprising wherein the silicon is removed from the fin structures to form silicon germanium nanowire structures separated from each other by a gap.

5. The method of claim 3 further comprising wherein the silicon germanium is

removed from the fin structures to form silicon nanowire structures separated from each other by a gap.

6. The method of claim 4 further comprising wherein a gate dielectric is formed around all sides of the silicon germanium nanowire structures.

7. The method of claim 5 further comprising wherein a gate dielectric is formed around all sides of the silicon nanowire structures.

8. The method of claim 6 further comprising wherein a gate electrode material is formed around the silicon germanium nanowire structures.

9. The method of claim 7 further comprising wherein a gate electrode material is formed around the silicon nanowire structures.

10. The method of claim 1 further comprising an epitaxial tip disposed between the source/drain structures and the substrate.

11. The method of claim 9 further comprising wherein the gate electrode material comprises metal.

12. The method of claim 8 further comprising wherein the gate electrode material comprises metal.

13. The method of claim 9 further comprising wherein a trench contact couples to the source/drain structures, and wherein the source/drain structures comprise n+ doped silicon.

14. The method of claim 13 further comprising wherein a silicon epitaxial tip is disposed between the source/drain structure and the substrate.

15. The method of claim 9 further comprising wherein the device comprises a portion of an NMOS gate all around channel device.

16. The method of claim 9 further comprising wherein a trench contact couples to the source/drain structures, wherein the source/drain structures comprise p+ silicon germanium.

17. The method of claim 16 wherein a silicon epitaxial tip is disposed between the source/drain structures and the substrate.

18. The method of claim 17 wherein the device comprises a portion of a PMOS gate all around channel device, and wherein the silicon nanowires comprises strained silicon nanowires.

19. A method of forming a nanowire device comprising:

forming alternating layers of epitaxial silicon on epitaxial silicon germanium on a substrate;

patterning the alternating layers to form fin structures;

forming a sacrificial gate electrode over said fin structures;

forming spacers adjacent to sidewalls of the sacrificial gate electrode and over said fin structures;

removing a semiconductor portion of the fin structures from source/drain regions on the substrate, then forming source/drain structures on the source/drain regions, wherein the source/drain regions are adjacent the spacers;

after removing the semiconductor portion of the fin structures from the source/drain regions, removing said sacrificial gate electrode from between the spacers; and

removing one of the silicon and the epitaxial silicon germanium layers from the fin structures disposed between the spacers.

20. The method of claim 19 further comprising wherein said substrate is an SOI

substrate and wherein a bottom nanowire geometry of the fin structure is defined by controlling the etching of a bottom oxide portion of the SOI substrate.

21. The method of claim 20 further comprising wherein the bottom oxide is etched to form two nanowires.

22. A method of forming a device comprising:

forming a sacrificial material on a substrate;

forming an epitaxial semiconductor on the sacrificial material;

patterning the epitaxial semiconductor disposed on the sacrificial material to form a fin structure;

forming a sacrificial gate electrode over the fin structure;

forming spacers adjacent to sidewalls of the sacrificial gate electrode and over the fin structure;

removing a semiconductor portion of the fin structure from source/drain regions on the substrate, then forming source/drain structures on the source/drain regions wherein the source/drain regions are adjacent to the spacers;

removing the sacrificial gate electrode from between the spacers; and

removing the sacrificial material from the fin structure disposed between the spacers.

23. The method of claim 22 further comprising wherein the device comprises a gate all around nanowire device.

24. The method of claim 22 further comprising additional alternating layers of epitaxial semiconductor and sacrificial material.

25. The method of claim 24 wherein the sacrificial material is removed from the fin structure to form semiconductor nanowire structures separated from each other by a

gap.

26. The method of claim 25 further comprising wherein a gate dielectric is formed around all sides of the semiconductor nanowire structures.

27. The method of claim 26 further comprising wherein a gate electrode material is formed around the semiconductor nanowire structures.

28. The method of claim 27 wherein the gate electrode material comprises metal.

29. The method of claim 22 further comprising wherein a semiconductor epitaxial tip is disposed between the source/drain structures and the substrate.

30. The method of claim 25 wherein semiconductor nanowires comprises strained semiconductor nanowires.