

SPECIFICATION

Transistor circuit

5 The present invention relates to a transistor circuit for obtaining a large amplitude voltage signal from a transistor circuit, for example from the collector electrode of the transistor.

10 A large amplitude A-class amplifying circuit is used in an operational amplifying circuit or in a low frequency power amplifying circuit as a circuit for driving a push-pull output stage. In this circuit, driving transistors are caused to operate in the saturation region at the time of maximum voltage output or minimum voltage output.

15 However, when an amplifying transistor operates in the saturation region (i.e. the operation region in which the collector-emitter voltage V_{CE} is about 0.25 to 0.4 V), the output voltage against distortion ratio characteristic becomes a "hard-clip" characteristic and contains higher harmonics of particularly high values. Hence, the output distortion increases and has an adverse effect on the tone quality produced by an audio amplifier.

25 On the other hand, the amplifying transistor operates in the quasi-saturation region (i.e. the operation region in which the collector-emitter voltage is about 1 V) before it reaches the saturation region. In the operation of the transistor in this quasi-saturation region, the cut-off frequency f_r lowers and hence the phase shift of the transistor becomes great and, consequently, causes an increase in the instability of the negative feed-back action in the negative feed-back circuit.

35 When, for example, a driving transistor in a large amplitude A-class transistor amplifying circuit for driving two push-pull output transistors acting between two power source voltages $+V$ and $-V$, is driven into its quasi-saturation region, the push-pull output voltage V_{OUT} is lowered to a value immediately above the power source voltage $-V$. In such circumstances, the push-pull output V_{OUT} exhibits a local oscillation wave form V_{OCS} due to the large phase shift in the negative feed-back circuit resulting from a substantial reduction in the cut-off frequency f_r .

45 According to the present invention there is provided a transistor circuit comprising a first transistor, and means for detecting the collector-emitter voltage of said first transistor and comparing it with a reference voltage, said detection-comparison means limiting the base current of said first transistor before said first transistor is driven into a quasi-saturation operation region, thereby to prevent said first transistor from being driven into the quasi-saturation operation region.

According to the present invention there is provided a transistor circuit including:

- 50 a first transistor to be protected from being driven into the quasi-saturation operation region;
- a reference voltage set to voltage corresponding to approximately twice a p-n junction voltage in the forward direction; and
- a detection comparison circuit for detecting the collector-emitter voltage of the first transistor and

comparing said collector-emitter voltage with the reference voltage;

70 said detection comparison circuit limiting, firstly the base current of the first transistor before it is driven to the quasi-saturation operation region, and secondly the drop of the collector-emitter voltage of the first transistor to a value approximately equal to the reference voltage.

75 The present invention will now be described in greater detail, by way of example, with reference to the accompanying drawings wherein:-

Figure 1 is a circuit diagram of a first embodiment of a transistor circuit according to the present invention;

80 Figure 2 is a sectional view of a first embodiment of an integrated circuit according to the present invention when the principal portion of the first embodiment of the transistor circuit shown in Figure 1 is constructed in the form of an integrated circuit;

85 Figure 3 is a circuit diagram of a second embodiment of a transistor circuit according to the present invention;

90 Figure 4 is a diagram showing the waveform when the transistor is operated in the quasi-saturation region;

Figure 5 is a diagram showing the dependence of the cut-off frequency of the transistor on the collector-emitter voltage and on the collector current;

95 Figure 6 is a sectional view of a second embodiment of an integrated circuit according to the present invention forming the principal portion of a transistor circuit of the present invention;

100 Figure 7 is a circuit diagram of a third embodiment of a transistor circuit according to the present invention; and

Figure 8 is a sectional view of a third embodiment of an integrated circuit according to the present invention when the principal portion of the embodiment of the transistor circuit shown in Figure 7 is constructed in the form of a semiconductor integrated circuit.

105 Figure 1 is a circuit diagram when a first embodiment of a transistor circuit according to the present invention is applied to an integrated circuit for an audio equipment.

110 Transistors Q_1 and Q_2 are differential amplifying transistors, and a constant-current circuit I_{01} is connected to the collector electrodes of both these transistors while transistors Q_3 and Q_4 are connected to their emitter electrodes respectively.

115 A bias voltage V_{B1} is applied to the base electrodes of the transistors Q_3 and Q_4 and a voltage level-shifted by a base-emitter voltage value is applied as a bias voltage to the emitter electrodes of both the differential amplifying transistors Q_1 and Q_2 .

120 A transistor Q_5 having its base and collector electrodes connected together so that it acts as a diode, is connected to the emitter electrode of the differential amplifying transistor Q_1 via the bias transistor Q_3 while a transistor Q_6 is connected to the emitter electrode of the other differential amplifying transistor Q_2 via the transistor Q_4 whereby the base and emitter electrodes of the transistor Q_6 are connected to the respective electrodes of the transistor Q_5 .

Since these transistors Q_5 and Q_6 together form a current mirror circuit, the collector current of the transistor Q_6 becomes substantially equal to the emitter current of the differential amplifying transistor Q_1 . Hence, an output current is obtained from the collector electrode of the transistor Q_6 , the output current being the difference in the emitter current between the differential amplifying transistors Q_1 and Q_2 .

A diode D_3 is connected between the level-shifting transistor Q_4 and the current mirror transistor Q_6 , and is a level-shifting diode used for controlling amplifying transistors Q_7 and Q_8 .

This differential amplifying circuit converts an input voltage signal into a current which is applied to the transistors Q_7 and Q_8 . The transistors Q_7 and Q_8 which are connected in Darlington configuration form an amplifying transistor stage in a large amplitude A-class transistor amplifying circuit and a constant-current circuit I_{O2} forms its collector load means.

This circuit converts the driving input current signal into a voltage signal and transfers an output voltage V_{OUT} to an output terminal T_3 via transistors Q_9 and Q_{10} that together form an output stage push-pull circuit.

Diodes D_1 and D_2 connected in series between the base electrodes of the output push-pull transistors Q_9 and Q_{10} form a bias circuit for reducing the cross-over distortion of these transistors Q_9 and Q_{10} .

A transistor Q_{11} having its base electrode connected to the collector electrode of the driving transistor Q_8 , its emitter electrode connected to the collector electrode of the bias transistor Q_4 of the pre-amplification circuit and its collector electrode connected to the negative power source voltage terminal T_2 forms means for detecting the quasi-saturation operating condition and for restricting the input current.

Thus, the emitter voltage of this transistor Q_{11} is fixed at $[V_{BEQ8} + V_{BEQ7} + V_{FD3}]$ where V_{BEQ8} is the base-emitter voltage of the transistor Q_8 in the forward direction (approx. 0.68 V); V_{BEQ7} is the base-emitter voltage of the transistor Q_7 in the forward direction (approx. 0.65 V); and V_{FD3} is the voltage of the diode D_3 in the forward direction (approx. 0.68 V).

Hence, the transistor Q_{11} is turned on and limits the base current feed to the driving transistor Q_7 when the collector-base voltage V_{CEQ8} of the driving transistor Q_8 becomes substantially less than the voltage $[V_{BEQ8} + V_{BEQ7} + V_{FD3} - V_{BEQ11}]$, where V_{BEQ11} is the base-emitter voltage of the transistor Q_{11} in the forward direction (approx. 0.65 V).

If the collector-emitter voltage V_{CEQ8} of the driving transistor Q_8 becomes less than about 1.33 V, therefore, the transistor Q_{11} is turned on, so that the voltage drop of the collector-emitter voltage V_{CEQ8} is limited to approximately 1.33 V.

According to this first embodiment, the collector-emitter voltage becomes about 1 V and the transistor Q_{11} is turned on and restricts any further increase in the input current before the operation reaches the quasi-saturation or saturation region where the cut-off frequency f_T is markedly reduced. It is therefore possible to prevent operation of the transistor in the

quasi-saturation and saturation region and to overcome the problems of an increase in distortion, or oscillation.

In addition, a diode or diodes similar to the level-shifting diode D_3 may be added in series with the diode D_3 if the collector-emitter voltage is large in the quasi-saturation region, and omitted if the collector-emitter voltage is small.

In this first embodiment, when the transistor Q_8 operates in the unsaturated range (that is, in the active region or in the cut-off region), the transistor Q_{11} is in the OFF state and a reverse bias voltage is applied across its base and emitter electrodes in accordance with the collector electrode potential of the transistor Q_8 . For this reason, the reverse breakdown voltage BV_{BEQ11} between the base and emitter electrodes of the transistor Q_{11} is set to a value substantially equal to the breakdown voltage BV_{CEQ8} between the collector and emitter electrodes of the transistor Q_8 .

The transistor Q_{11} is a p-n-p type. In producing an integrated circuit, the transistor Q_{11} may be of a known lateral construction that can be produced simultaneously with the production of the n-p-n type transistor Q_8 , which is produced with a vertical construction. In such a case, since the collector electrode of the transistor Q_8 and the base electrode of the transistor Q_{11} are connected together it is possible to form the lateral type transistor Q_{11} in the collector region of the transistor Q_8 . By forming the transistors Q_8 and Q_{11} in the same semiconductor region in this manner, it is possible to reduce the area required for an isolation region when compared with the case where these transistors are individually and independently formed in semiconductor regions and formed separately from the semiconductor substrate.

In the second embodiment of an integrated circuit according to the present invention shown in Figure 6, since the collector electrode of the transistor Q_{11} is connected to the voltage terminal T_2 ($-V_{CC}$), the transistors Q_8 and Q_{11} are formed in the same n⁻-type semiconductor region 4 and the collector of the transistor Q_{11} uses the p-type semiconductor substrate 1 while the base of the transistor Q_{11} uses the n⁻-type semiconductor region 4 formed on the p-type semiconductor substrate 1. A p-type semiconductor region 7 is formed simultaneously with the formation of a p-type base region 5 of the n-p-n transistor on the surface of this n⁻-type semiconductor region 4 and is used as the emitter of the transistor Q_{11} . Hence this p-n-p transistor Q_{11} is formed with a substrate type construction.

The n⁻-type semiconductor region 4, the p-type semiconductor region 5 and the n⁺-type semiconductor region 6 are respectively the collector, base and emitter of the n-p-n type transistor Q_8 having a vertical construction.

Unlike the lateral type p-n-p transistor in which two p-type regions must be formed in juxtaposition on the surface of the n-type semiconductor region for the emitter and the collector, this substrate type p-n-p transistor requires the formation of only one p-type region on the surface of the n-type semiconductor region as described above. Hence, the area

required becomes small on the surface of the semiconductor region. The distribution of the impurity concentration in the semiconductor region for forming the base-emitter junction of the substrate type p-n-p transistor is substantially equal to the distribution of the impurity concentration in the semiconductor region for forming the collector-base junction of the n-p-n transistor. Thus, the breakdown voltage between the base and the emitter electrodes of the substrate type p-n-p transistor Q_{11} is equal to the breakdown voltage between the base and the collector electrodes of the n-p-n transistor and consequently, the normal operation of the circuit shown in Figure 1 is not restricted.

In accordance with the first embodiment of an integrated circuit according to the present invention, the n-p-n transistor Q_8 and the substrate-type p-n-p transistor Q_{11} are not formed in the semiconductor regions independently of each other but in a common semiconductor region, thereby reducing the area required for the semiconductor region. Figure 2 shows an example of such an embodiment.

As shown in Figure 2, an n⁻-type epitaxial growth layer 4 formed on the p-type semiconductor substrate 1 is an element-forming region surrounded by a p⁺-type isolation region 3. A vertical type n-p-n transistor Q_8 is obtained by forming the base region 5 in this element-forming n⁻-type region 4 and the emitter region 6 in this base region 5. A substrate type p-n-p transistor Q_{11} is obtained by then forming a p-type emitter region 7.

The n⁺-type region 2 is a collector buried layer and the collector of the transistor Q_{11} uses the p⁺-type isolation region 3 and the p-type substrate 1.

Alternatively to the first embodiment of the transistor circuit, voltage comparison means and current limiting means may be separated from each other in the present invention according to a second embodiment of the transistor circuit, shown in Figure 3.

In other words, as shown in Figure 3, a voltage comparison circuit is formed by applying the collector voltage of the driving transistor Q_8 to the base electrode of the detection transistor Q_{12} via the base-emitter junction of the output transistor Q_{10} and also applying a voltage V_{B2} , corresponding to the voltage to be detected, to the emitter electrode of the transistor Q_{12} and by connecting a diode D_4 to its collector electrode, while a current mirror circuit is formed by arranging an input current limiting transistor Q_{13} on the input side of the driving transistors Q_7 and Q_8 in cooperation with the diode D_4 , thereby to limit the input current.

In this circuit, when the base voltage of the transistor Q_{12} becomes less than $(V_{B2} - V_{BEQ12})$ or when the collector voltage of the transistor Q_8 becomes less than $(V_{B2} - V_{BEQ12} - V_{BEQ10})$, the transistor Q_{12} is turned on and reduces the input current by an amount corresponding to its collector current, via the transistor Q_{13} . It is therefore possible to prevent operation in the quasi-saturation region by properly selecting the abovementioned voltage V_{B2} .

Since V_{BEQ10} is about 0.68 V and V_{BEQ12} is about 0.65 V and since the operation of the transistor Q_8 in the quasi-saturation range starts when its collector voltage V_{CE} is about 1.0 V, the abovementioned voltage

V_{B2} is set to about 2.33 V.

In this manner, the collector voltage of the driving transistor Q_8 may be level-shifted by the use of the output stage circuit and then applied as an input to the voltage comparison means. Alternatively, it may be applied as an input to the voltage comparison means via the bias diodes D_1 and D_2 , that is, via the base-emitter voltage of the output transistors Q_{10} and Q_9 .

Also, the present invention can be applied to a wide range of applications such as a circuit for preventing the operation of a large amplitude A-class amplifying circuit in the quasi-saturation and saturation region, in addition to the driving stage amplifying transistor circuit of a push-pull output circuit.

Figure 7 is a circuit diagram of the transistor amplifying circuit according to a third embodiment of a transistor circuit according to the present invention. All circuit elements in the integrated circuit encircled by the dotted line may be formed in one silicon chip by a method known in the art and the circuit is formed in a monolithic semiconductor integrated circuit.

An input signal applied to the terminal *tin* is transmitted to a terminal T_5 through an input circuit 1 consisting of resistors R_{101} , R_{102} and R_{103} and capacitors C_{101} and C_{102} .

This signal is amplified by an initial stage differential amplifying circuit consisting of transistors Q_{11} to Q_{17} and resistors R_{11} to R_{13} and the amplified signal appears at the collector electrode of the transistor Q_{14} . A D.C. current flowing through the differential amplifying transistors Q_{11} and Q_{12} is set by a constant current that is supplied from the collector electrode of a constant-current transistor Q_{15} .

This constant current is in turn determined by a bias current flowing through a bias circuit 3 consisting of resistors R_{17} to R_{19} and a transistor Q_{24} having its base and collector electrodes interconnected so as to act as a diode. This bias current can be adjusted by a resistor R_{110} connected between terminals T_7 and T_2 outside the integrated circuit.

A transistor Q_{16} connected between the emitter electrodes of the differential amplifying transistors Q_{11} and Q_{12} and the collector electrode of the constant-current transistor Q_{15} is provided in order to reduce the current change due to the Early effect of the transistor arising from the voltage fluctuation of the power source voltages +Vcc and -Vcc applied respectively to the power source terminals T_1 and T_2 .

The output signal of the initial stage differential amplifying circuit 1 obtained from the collector electrode of the transistor Q_{14} is amplified by a large amplitude A-class transistor amplifying circuit 4 comprising transistors Q_{18} and Q_{19} connected in Darlington configuration, a resistor R_{14} , a phase compensating capacitor C_1 , diode-connected transistors Q_{20} and Q_{21} for adjustment of an idling current, a resistor R_{15} , a constant-current load transistor Q_{23} and a resistor R_{16} .

This signal is amplified by a B-class output push-pull circuit 5 consisting of transistors Q_{27} and Q_{28} and resistors R_{21} and R_{22} , and is finally transmitted to the output terminal T_3 .

A negative feed-back circuit 6 is connected bet-

ween the output terminal T_3 and a feed-back terminal T_4 in order to obtain an RIAA characteristic and this negative feed-back circuit 6 consists of resistors R_{104} to R_{107} and capacitors C_{104} to C_{108} as illustrated in Figure 7.

The collector electrodes of the transistors Q_{18} and Q_{19} connected in the Darlington configuration are directly connected to each other so that it is possible to make the distortion ratio of this amplifying circuit extremely low.

As shown in the third embodiment of an integrated circuit according to the present invention shown in Figure 8, both collectors of these transistors Q_{18} and Q_{19} are formed by a single n⁻-type semiconductor region 4 and this region 4 can also be used as the base region for the transistor Q_{25} for preventing operation in the quasi-saturation region. Thus, since these three transistors Q_{18} and Q_{19} and Q_{25} can be formed in the single element-forming region 4, the arrangement is preferable for enhancing the integrity of the semiconductor integrated circuit. Other reference numerals 1 to 3, 5 to 7, 5" and 6" represent the same or similar regions to those shown in Figures 2 and 6.

In exactly the same way as in the embodiment shown in Figure 1, the collector-emitter voltage V_{CEQ19} of the transistor Q_{19} of the large amplitude A-class amplifying circuit 4 in the embodiment shown in Figure 7 drops only to the neighbourhood of 1.33 V. Hence, it is possible to prevent its operation in the quasi-saturation region.

In other words, the output of the large amplitude A-class amplifying circuit 4 falls only to the lower limit value of $-V_{CC} + V_{CEQ19}$. It is therefore desirable to enhance symmetry between the rising wave-form and the falling wave-form of this output by making the upper limit value of the rise in the output equal to the lower limit value of the fall in the output. A limiter circuit 7 consisting of a transistor Q_{26} and a resistor R_{20} is provided for that purpose. The limiter action of this limiter circuit is accomplished when the transistor Q_{26} becomes conductive. As a result, a base current is fed to the base electrode of the transistor Q_{18} , thereby limiting the rise in the output of the large amplitude A-class amplifying circuit 4 and enabling symmetry of the waveforms to be obtained.

CLAIMS

1. A transistor circuit including:

a first transistor to be protected from being driven into the quasi-saturation operation region;

a reference voltage set to voltage corresponding to approximately twice a p-n junction voltage in the forward direction; and

a detection comparison circuit for detecting the collector-emitter voltage of the first transistor and comparing said collector-emitter voltage with the reference voltage;

said detection comparison circuit limiting, firstly the base current of the first transistor before it is driven to the quasi-saturation operation region, and secondly the drop of the collector-emitter voltage of the first transistor to a value approximately equal to the reference voltage.

2. A transistor circuit according to Claim 1,

further including: a second transistor of the same conductivity type as said first transistor; a third transistor of the opposite conductivity type to said first transistor; and level-shift diode means; said first and second transistors being connected in Darlington configuration; said second transistor being the first stage transistor of the Darlington configuration and said first transistor being the final stage; said reference voltage value being set to the sum of the base-emitter voltages in the forward direction of said first and second transistors connected in Darlington configuration; the base electrode of said third transistor being connected to the collector electrode of said first transistor and the base electrode of said second transistor being connected to the emitter electrode of said third transistor via said level-shift diode means.

3. A transistor circuit according to Claim 2, wherein said first and second transistors are both vertical type n-p-n transistors formed in a semiconductor integrated circuit, said third transistor is a substrate type p-n-p transistor using the p-type semiconductor substrate of said semiconductor integrated circuit as at least a part of its collector region, the collector region of said first transistor and the base region of said third transistor being formed by a single n-type element-forming region located on said p-type semiconductor substrate.

4. A transistor circuit according to Claim 3, wherein the collector region of said second transistor is further formed by said single n-type element-forming region so that the collector of said first transistor and the collector of said second transistor are connected together.

5. A transistor circuit according to any one of Claims 2 to 4, wherein said transistor circuit also drives an initial stage differential amplifying circuit; collector load means for said first and second transistor connected in Darlington configuration; a B-class push-pull circuit; and a negative feed-back circuit connected between the output of said B-class push-pull circuit and either one of two inputs of said initial stage differential amplifying circuit; said first and second transistors being driven by the output of said initial stage differential amplifying circuit and forming, together with said collector load means, a large amplitude A-class transistor amplifying circuit so as to drive said B-class push-pull circuit.

6. A transistor circuit according to any one of the preceding claims, wherein said detection comparison circuit limits the drop of the collector-emitter voltage to approximately 1.33 volts.

7. A transistor circuit according to Claim 2, wherein said first and second transistors are of the n-p-n type and the third transistor is of the p-n-p type.

8. A transistor circuit according to Claim 1, further including: a second transistor of the same conductivity type as the first transistor; a third transistor of the opposite conductivity type to said first transistor; a fourth transistor of the same conductivity type as the first transistor; and level shift diode means; said first and second transistors being connected in Darlington configuration; said second transistor being the first stage transistor of the Dar-



ween the output terminal T_3 and a feed-back terminal T_4 in order to obtain an RIAA characteristic and this negative feed-back circuit 6 consists of resistors R_{104} to R_{107} and capacitors C_{104} to C_{108} as illustrated in Figure 7.

The collector electrodes of the transistors Q_{18} and Q_{19} connected in the Darlington configuration are directly connected to each other so that it is possible to make the distortion ratio of this amplifying circuit extremely low.

As shown in the third embodiment of an integrated circuit according to the present invention shown in Figure 8, both collectors of these transistors Q_{18} and Q_{19} are formed by a single n-type semiconductor region 4 and this region 4 can also be used as the base region for the transistor Q_{25} for preventing operation in the quasi-saturation region. Thus, since these three transistors Q_{18} and Q_{19} and Q_{25} can be formed in the single element-forming region 4, the arrangement is preferable for enhancing the integrity of the semiconductor integrated circuit. Other reference numerals 1 to 3, 5 to 7, 5" and 6" represent the same or similar regions to those shown in Figures 2 and 6.

In exactly the same way as in the embodiment shown in Figure 1, the collector-emitter voltage V_{CEQ19} of the transistor Q_{19} of the large amplitude A-class amplifying circuit 4 in the embodiment shown in Figure 7 drops only to the neighbourhood of 1.33 V. Hence, it is possible to prevent its operation in the quasi-saturation region.

In other words, the output of the large amplitude A-class amplifying circuit 4 falls only to the lower limit value of $-V_{CC} + V_{CEQ19}$. It is therefore desirable to enhance symmetry between the rising wave-form and the falling wave-form of this output by making the upper limit value of the rise in the output equal to the lower limit value of the fall in the output. A limiter circuit 7 consisting of a transistor Q_{26} and a resistor R_{20} is provided for that purpose. The limiter action of this limiter circuit is accomplished when the transistor Q_{26} becomes conductive. As a result, a base current is fed to the base electrode of the transistor Q_{18} , thereby limiting the rise in the output of the large amplitude A-class amplifying circuit 4 and enabling symmetry of the waveforms to be obtained.

CLAIMS

1. A transistor circuit including:

a first transistor to be protected from being driven into the quasi-saturation operation region;

a reference voltage set to voltage corresponding to approximately twice a p-n junction voltage in the forward direction; and

a detection comparison circuit for detecting the collector-emitter voltage of the first transistor and comparing said collector-emitter voltage with the reference voltage;

said detection comparison circuit limiting, firstly the base current of the first transistor before it is driven to the quasi-saturation operation region, and secondly the drop of the collector-emitter voltage of the first transistor to a value approximately equal to the reference voltage.

2. A transistor circuit according to Claim 1,

further including: a second transistor of the same conductivity type as said first transistor; a third transistor of the opposite conductivity type to said first transistor; and level-shift diode means; said first and second transistors being connected in Darlington configuration; said second transistor being the first stage transistor of the Darlington configuration and said first transistor being the final stage; said reference voltage value being set to the sum of the base-emitter voltages in the forward direction of said first and second transistors connected in Darlington configuration; the base electrode of said third transistor being connected to the collector electrode of said first transistor and the base electrode of said second transistor being connected to the emitter electrode of said third transistor via said level-shift diode means.

3. A transistor circuit according to Claim 2, wherein said first and second transistors are both vertical type n-p-n transistors formed in a semiconductor integrated circuit, said third transistor is a substrate type p-n-p transistor using the p-type semiconductor substrate of said semiconductor integrated circuit as at least a part of its collector region, the collector region of said first transistor and the base region of said third transistor being formed by a single n-type element-forming region located on said p-type semiconductor substrate.

4. A transistor circuit according to Claim 3, wherein the collector region of said second transistor is further formed by said single n-type element-forming region so that the collector of said first transistor and the collector of said second transistor are connected together.

5. A transistor circuit according to any one of Claims 2 to 4, wherein said transistor circuit also drives an initial stage differential amplifying circuit; collector load means for said first and second transistor connected in Darlington configuration; a B-class push-pull circuit; and a negative feed-back circuit connected between the output of said B-class push-pull circuit and either one of two inputs of said initial stage differential amplifying circuit; said first and second transistors being driven by the output of said initial stage differential amplifying circuit and forming, together with said collector load means, a large amplitude A-class transistor amplifying circuit so as to drive said B-class push-pull circuit.

6. A transistor circuit according to any one of the preceding claims, wherein said detection comparison circuit limits the drop of the collector-emitter voltage to approximately 1.33 volts.

7. A transistor circuit according to Claim 2, wherein said first and second transistors are of the n-p-n type and the third transistor is of the p-n-p type.

8. A transistor circuit according to Claim 1, further including: a second transistor of the same conductivity type as the first transistor; a third transistor of the opposite conductivity type to said first transistor, a fourth transistor of the same conductivity type as the first transistor; and level shift diode means; said first and second transistors being connected in Darlington configuration; said second transistor being the first stage transistor of the Dar-



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lington configuration and the first transistor being the final stage; said reference voltage value being set to the sum of the base-emitter voltages in the forward direction of the first and second transistor in

- 5 Darlington configuration; the base electrode of the third transistor being connected to the collector electrode of the first transistor and the base electrode of the second transistor being connected to the collector electrode of the third transistor through the
- 10 collector-base junction of the fourth transistor, the level-shift diode means being connected across the base-emitter junction of the fourth transistor.

9. A transistor circuit substantially as herein described with reference to, and as illustrated in Figure 1, Figure 3 or Figure 7 of the accompanying
- 15 drawings.

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