

**A METHOD AND SYSTEM FOR IMPLEMENTING REMAINDER
INSTRUCTION OF RISC-V INSTRUCTION SET**

ABSTRACT

The invention relates to the technical field of a microprocessor, in particular to a method and a system for realizing the residual instruction of the RISC-V instruction set. The invention executes the CPU out of order, and the instruction enters the instruction decoding unit from the fetch unit to carry out instruction decoding; the instruction after decoding is renamed in the renaming unit, and the remainder instruction is optimized at the same time. If the remainder instruction does not meet the optimization condition, the renamed instruction enters the reservation station and then enters the execution unit for execution; the executed instruction is submitted through the reordering cache and the division instruction encoding cache resources allocated in the renaming phase are released. In the renaming stage, the invention realizes the function of the remainder instruction by adding the residue instruction acceleration unit. When the division instruction and the residue instruction pair appear, the target register of the residue instruction is mapped to the physical register of the remainder of the division instruction, and the remainder generated by the division instruction is taken, and the execution efficiency of the remainder instruction is high.

(The most illustrative figure is FIG 1)