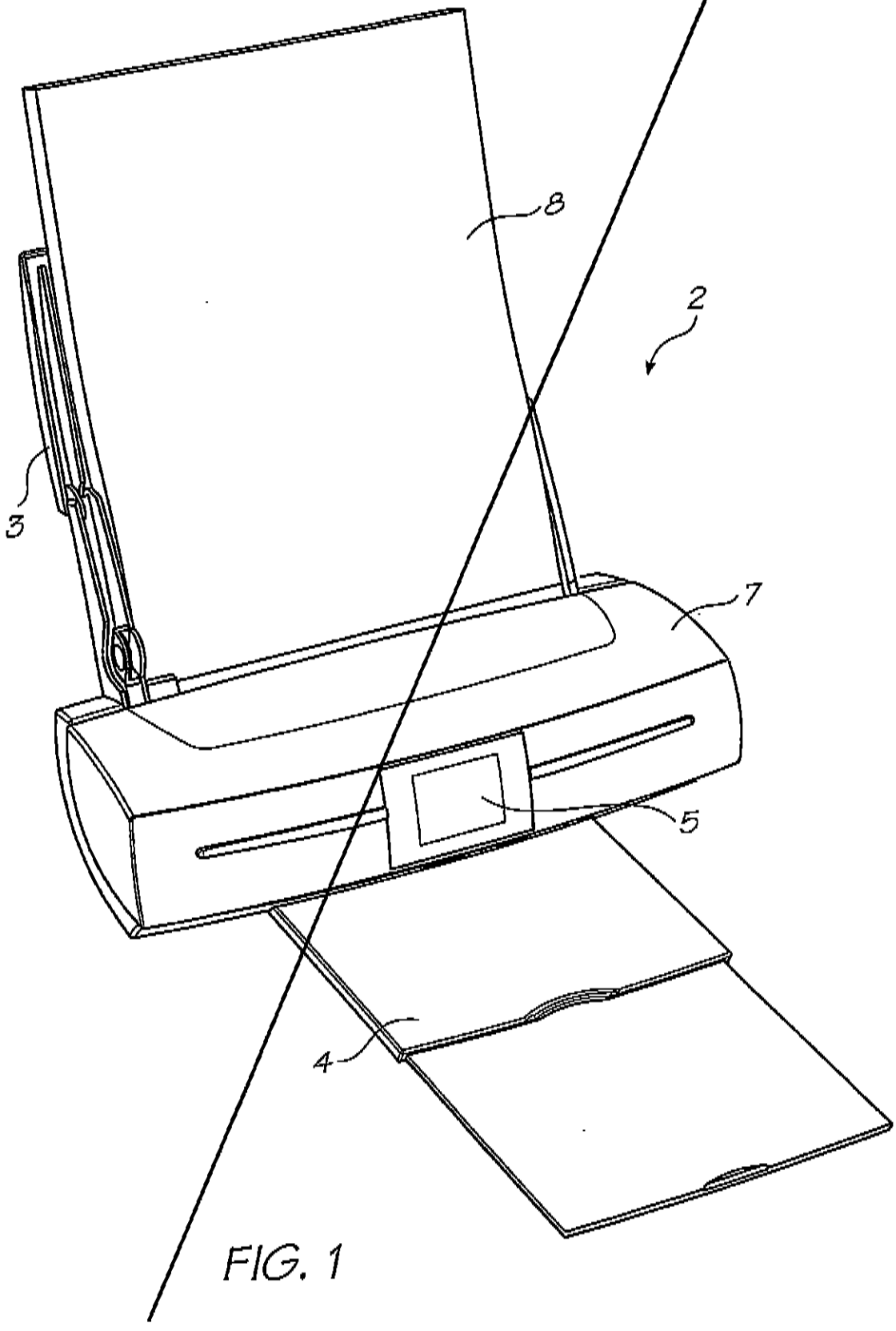


FIG. 1

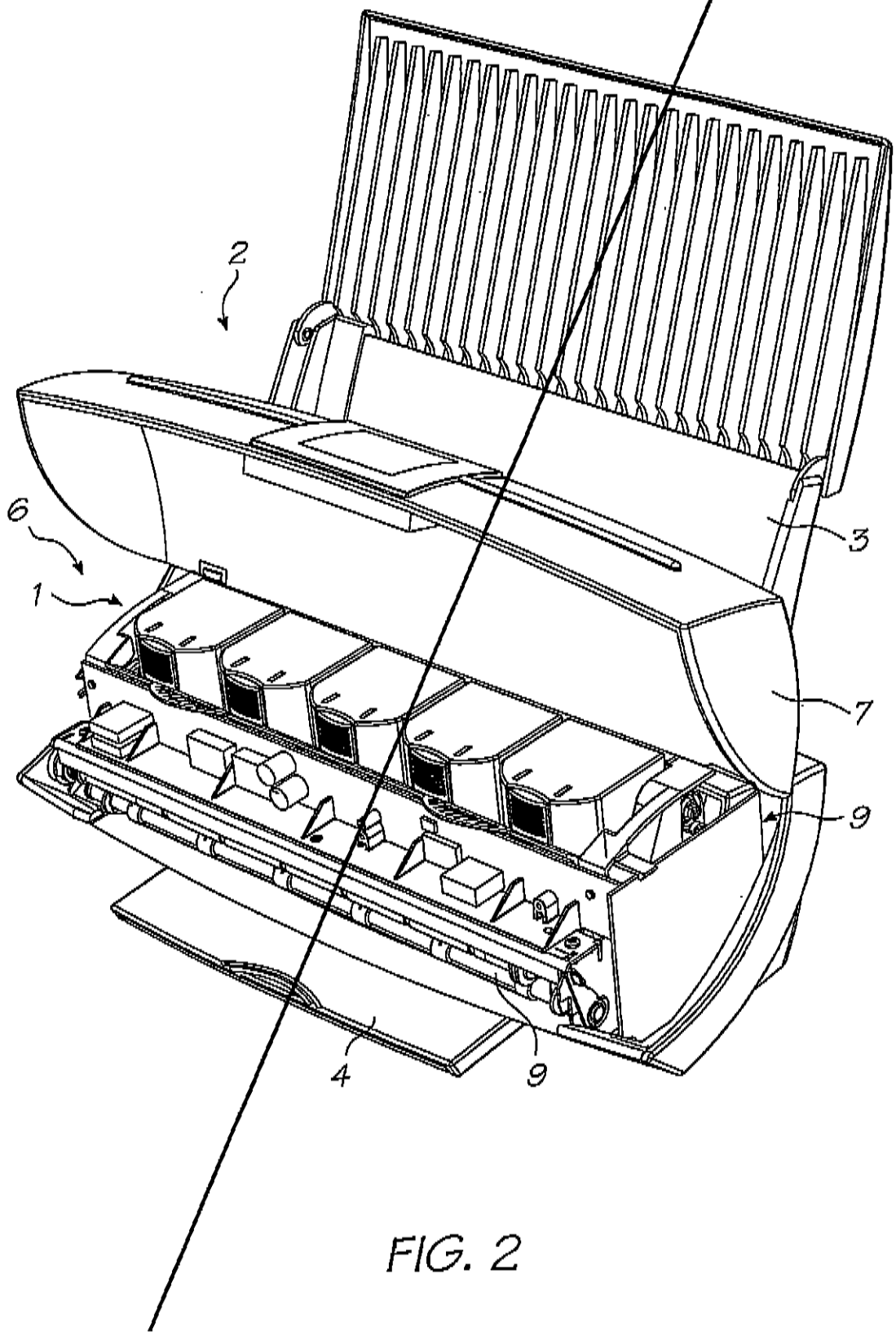


FIG. 2

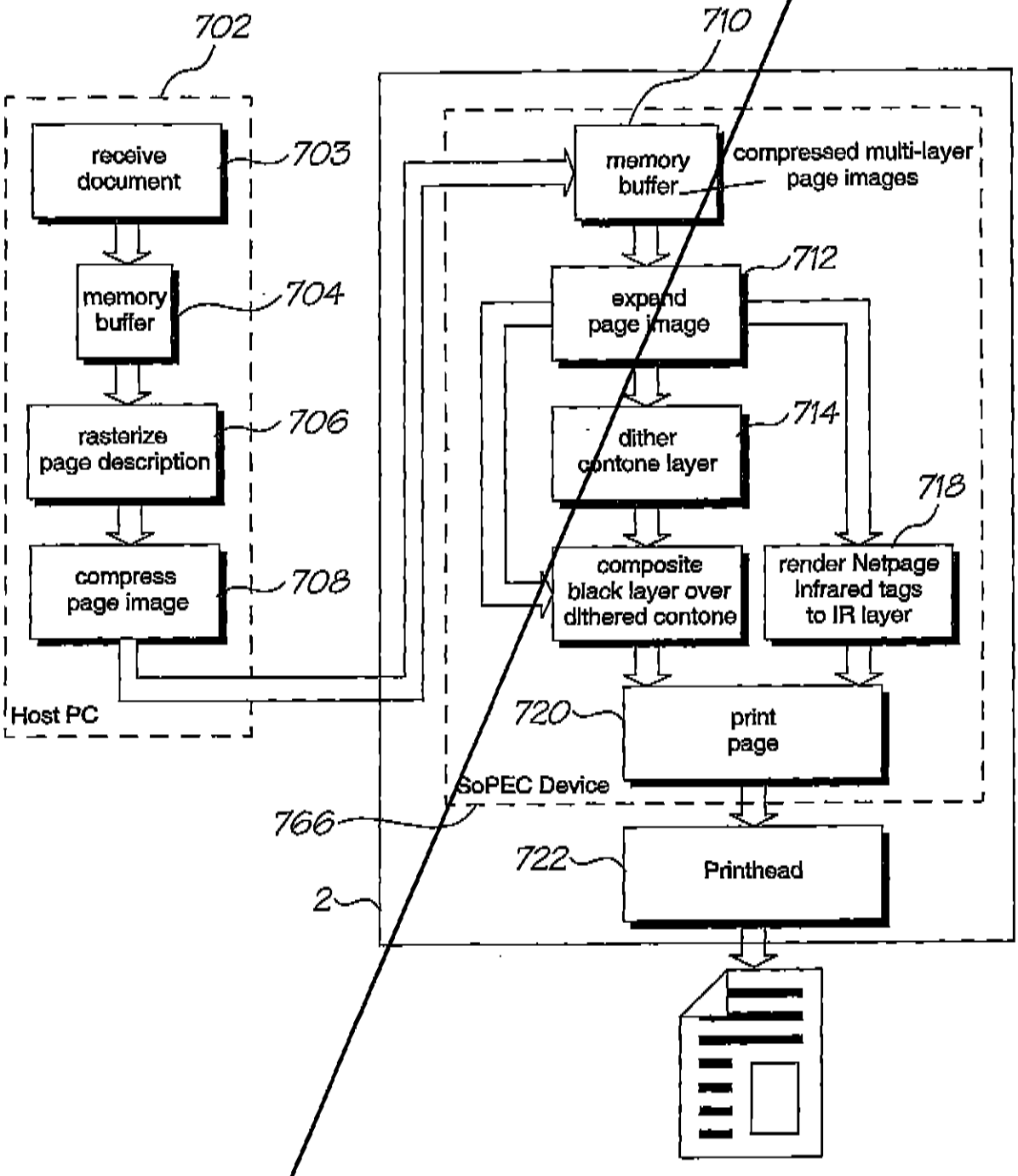

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710
receive document
703
memory buffer
704
rasterize page description
706
compress page image
708
Host PC
memory buffer
compressed multi-layer page images
712
expand page image
714
dither contone layer
718
composite black layer over dithered contone
render Netpage Infrared tags to IR layer
720
print page
SoPEC Device
766
722
Printhead
2

FIG. 3

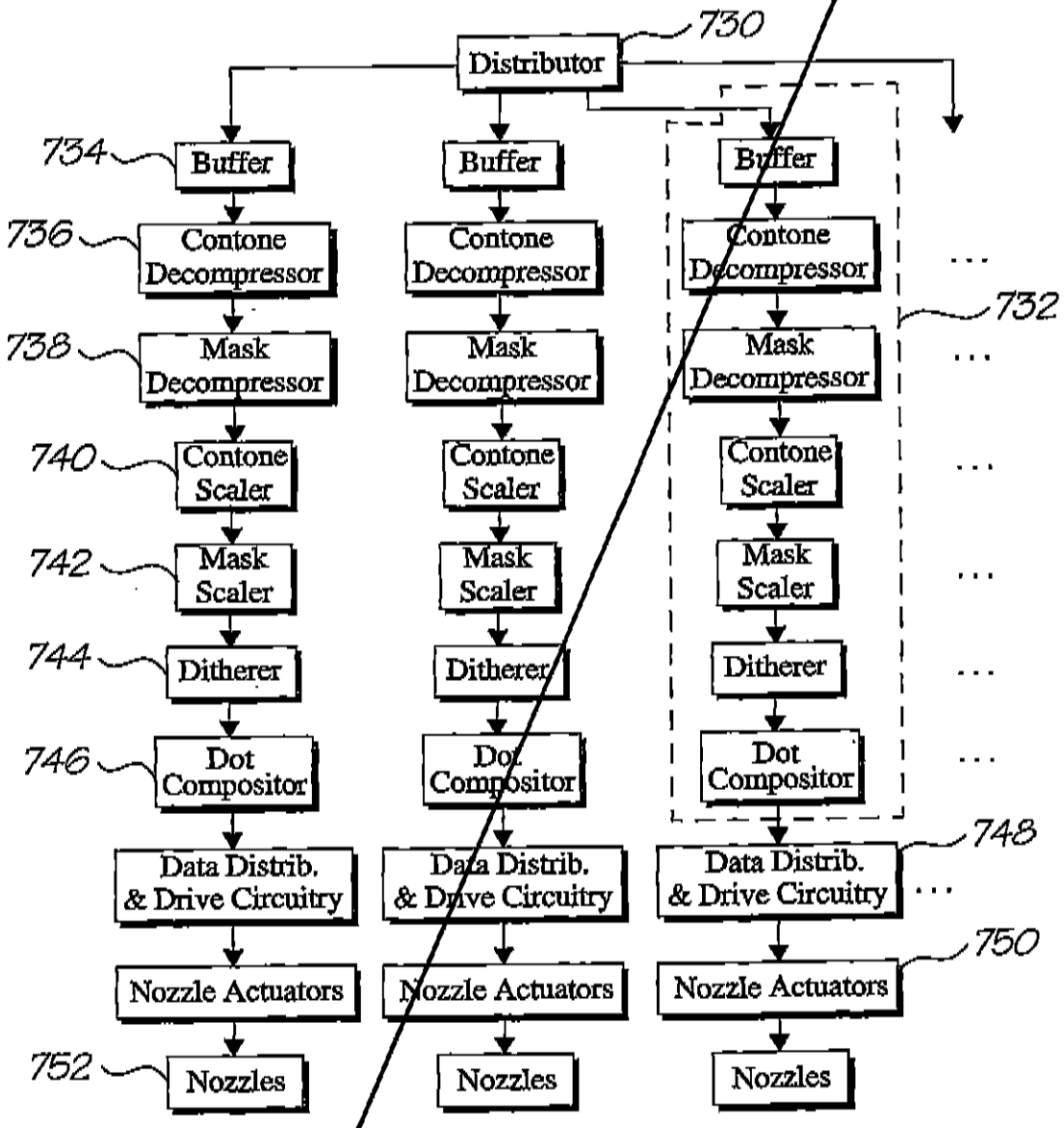

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Distributor
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Buffer
736
Contone Decompressor
738
Mask Decompressor
740
Contone Scaler
742
Mask Scaler
744
Ditherer
746
Dot Compositor
Data Distrib. & Drive Circuitry
Nozzle Actuators
752
Nozzles
732
748
750

FIG. 4

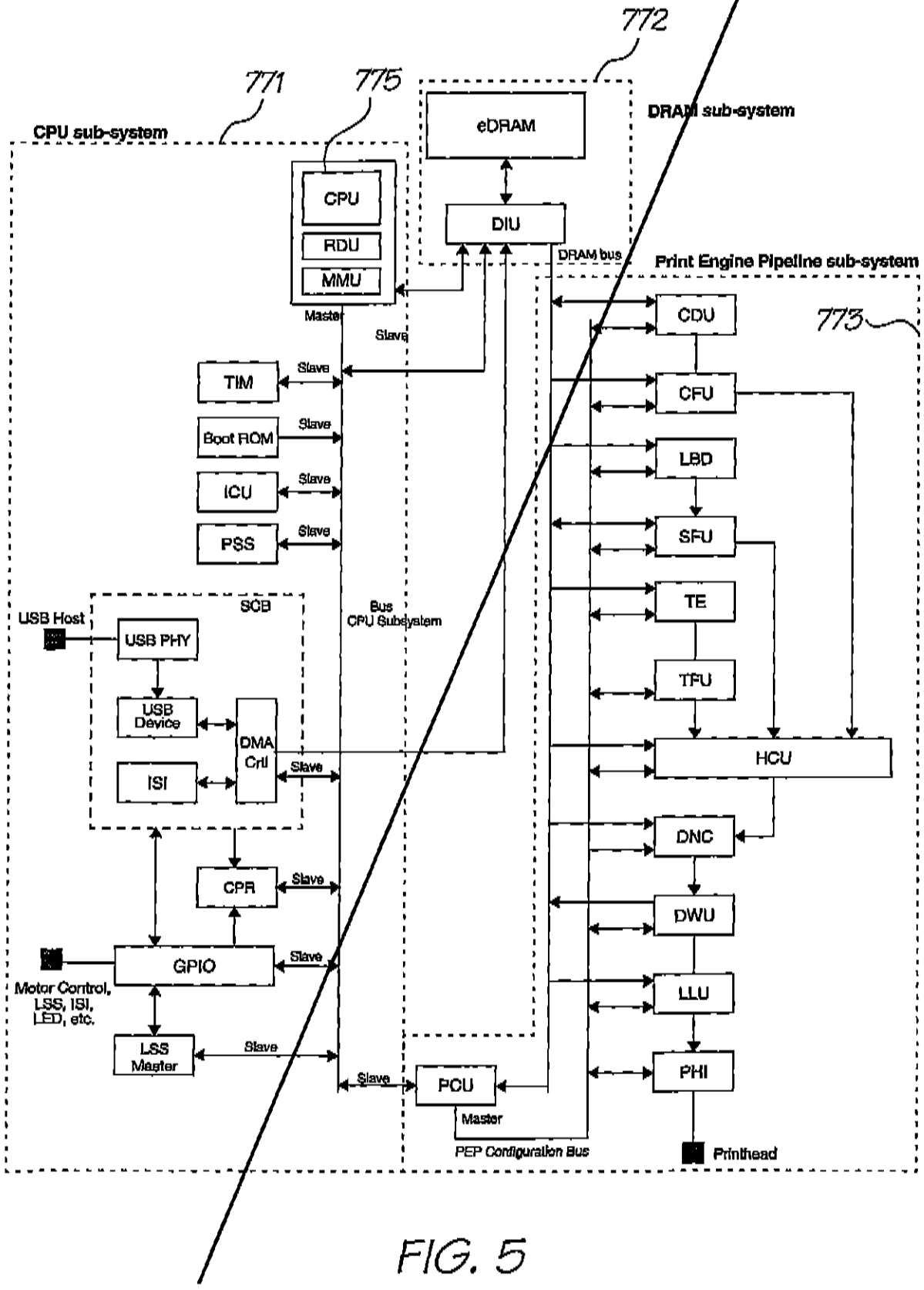

772
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775
CPU sub-system
DRAM sub-system
eDRAM
CPU
RDU
MMU
DIU
DRAM bus
Print Engine Pipeline sub-system
Master
Slave
CDU
773
TIM
CFU
Boot ROM
LBD
ICU
SFU
PSS
TE
SCB
Bus
CPU Subsystem
USB Host
USB PHY
TFU
USB Device
DMA Ctrl
HCU
ISI
DNC
CPR
DWU
GPIO
LLU
Motor Control, LSS, ISI, LED, etc.
LSS Master
PHI
PCU
Master
PEP Configuration Bus
Printhead

FIG. 5

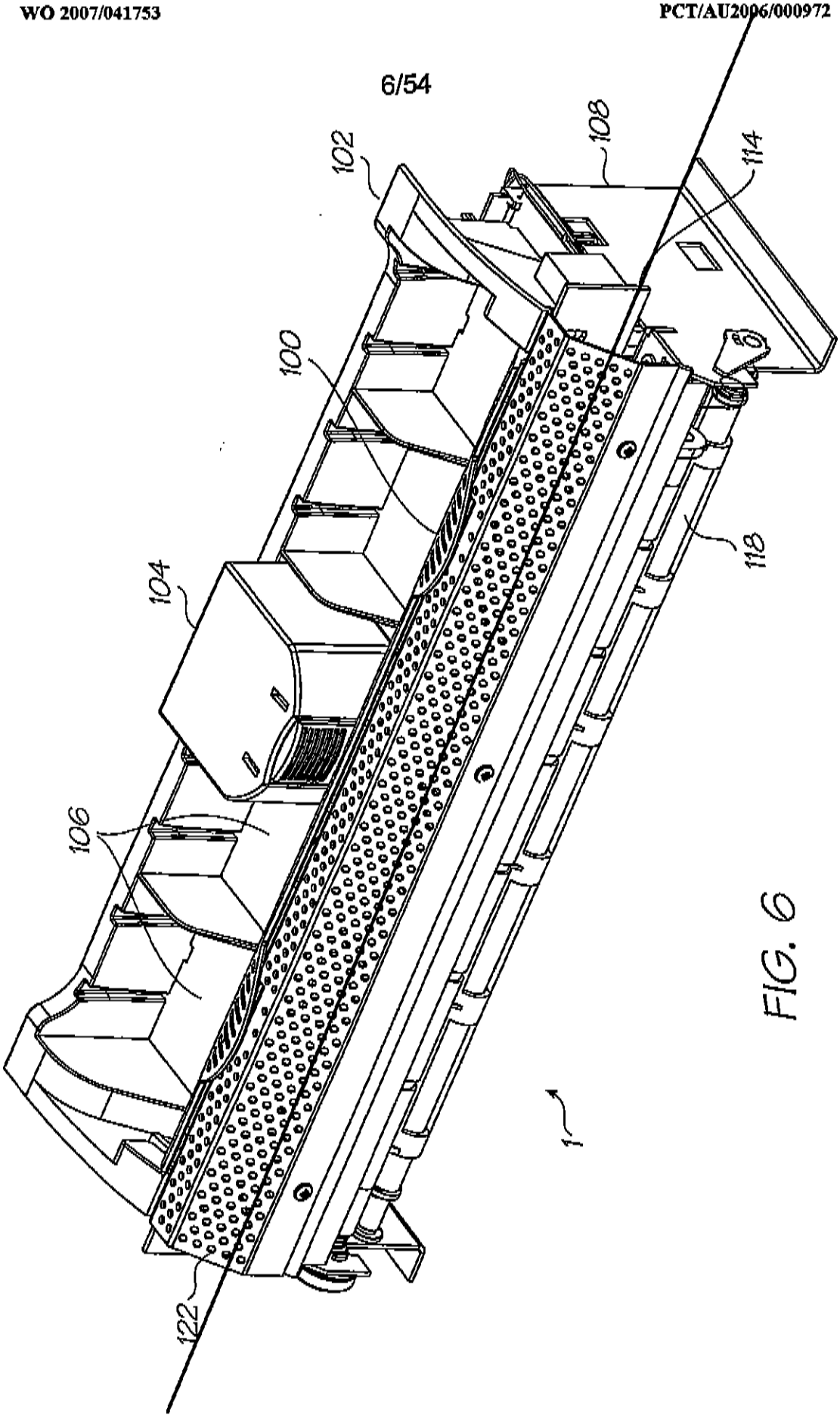


FIG. 6

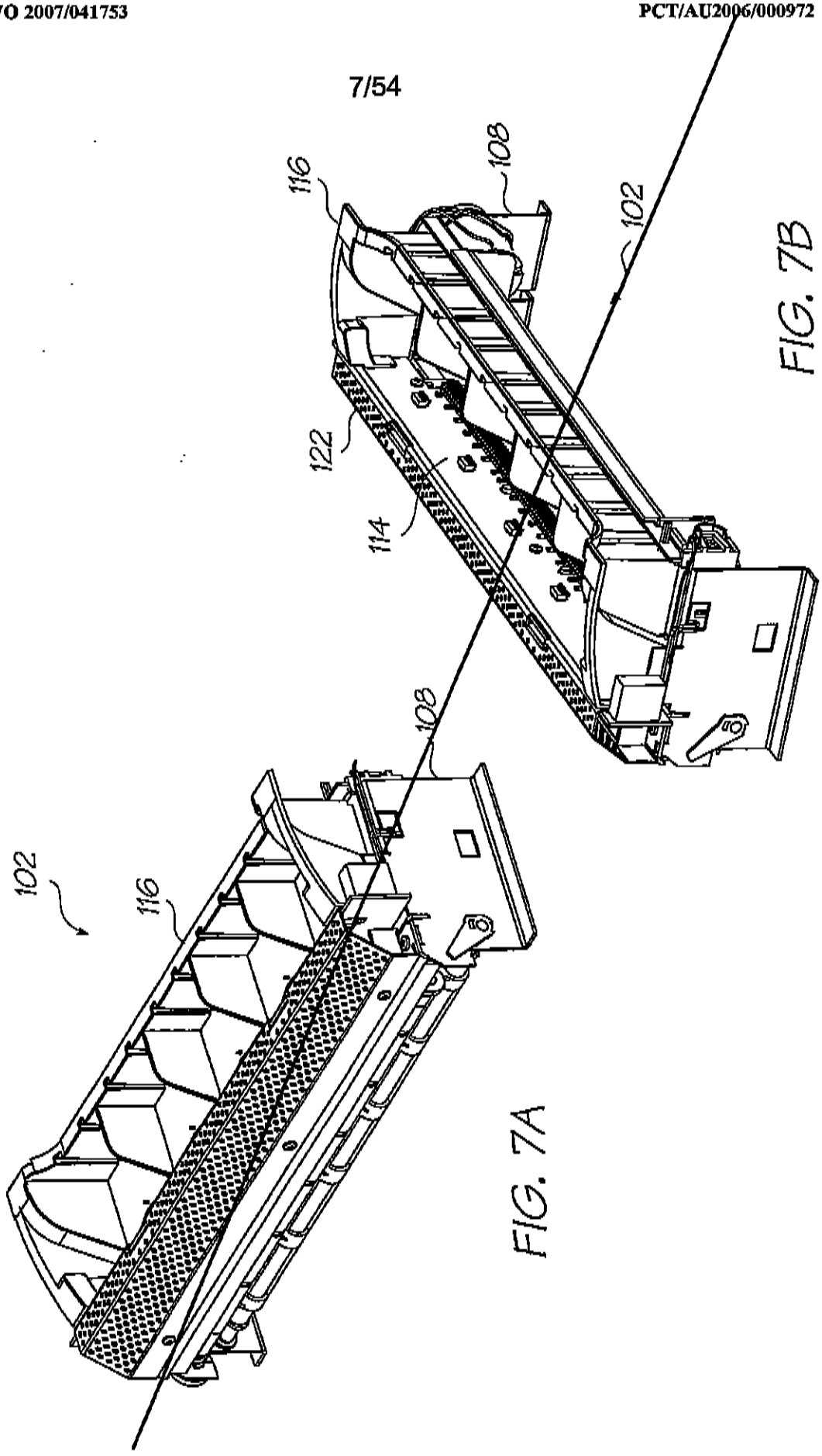


FIG. 7B

FIG. 7A

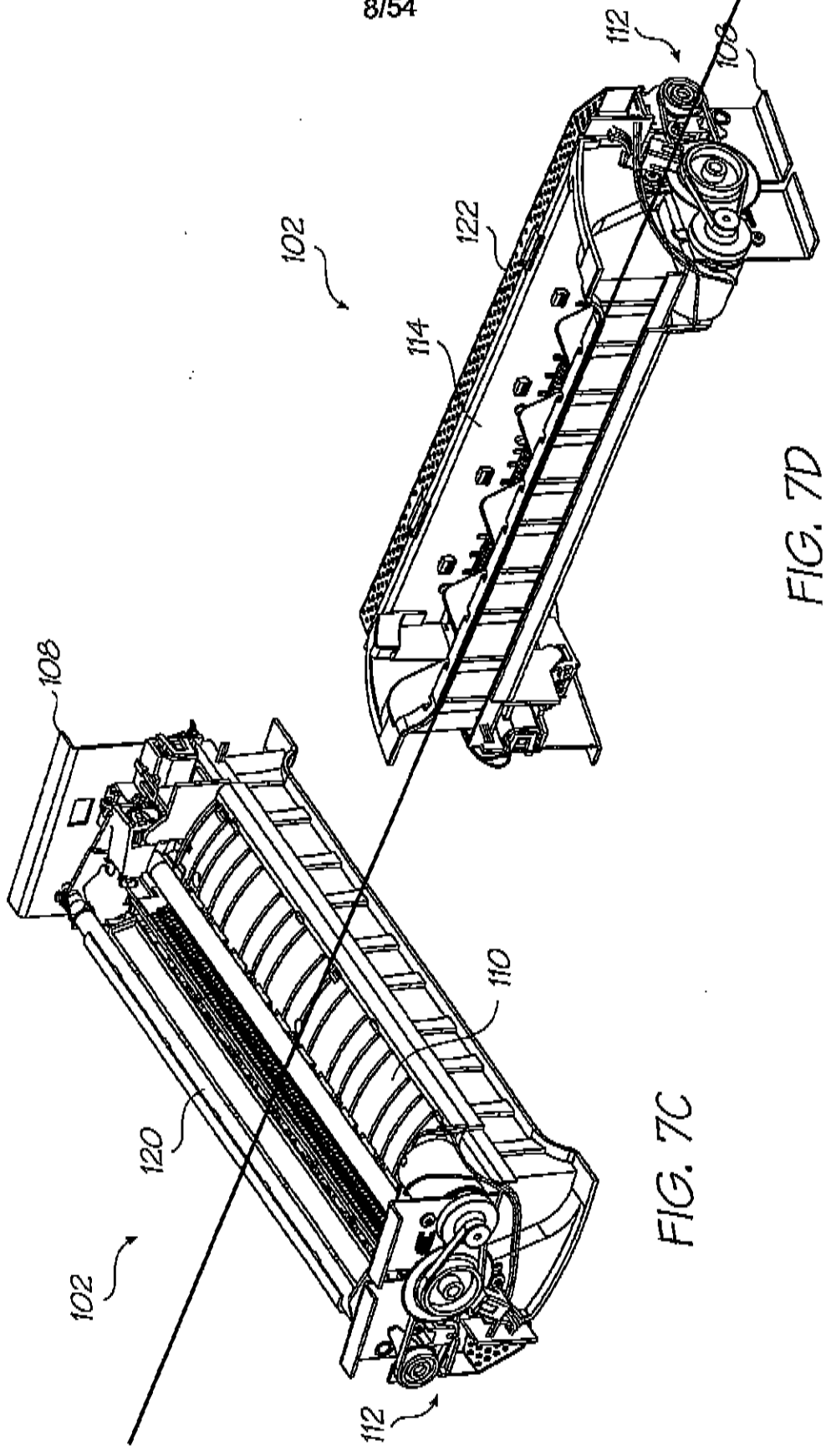


FIG. 7D

FIG. 7C

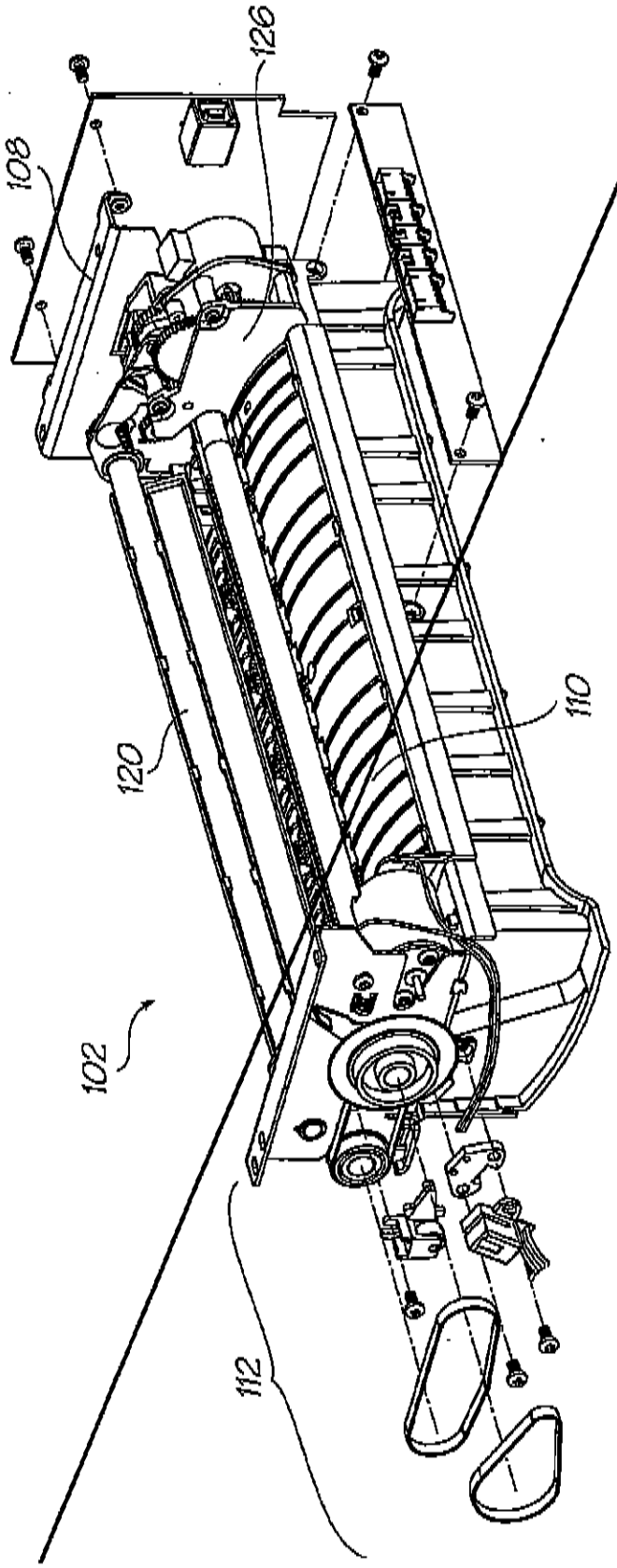


FIG. 8

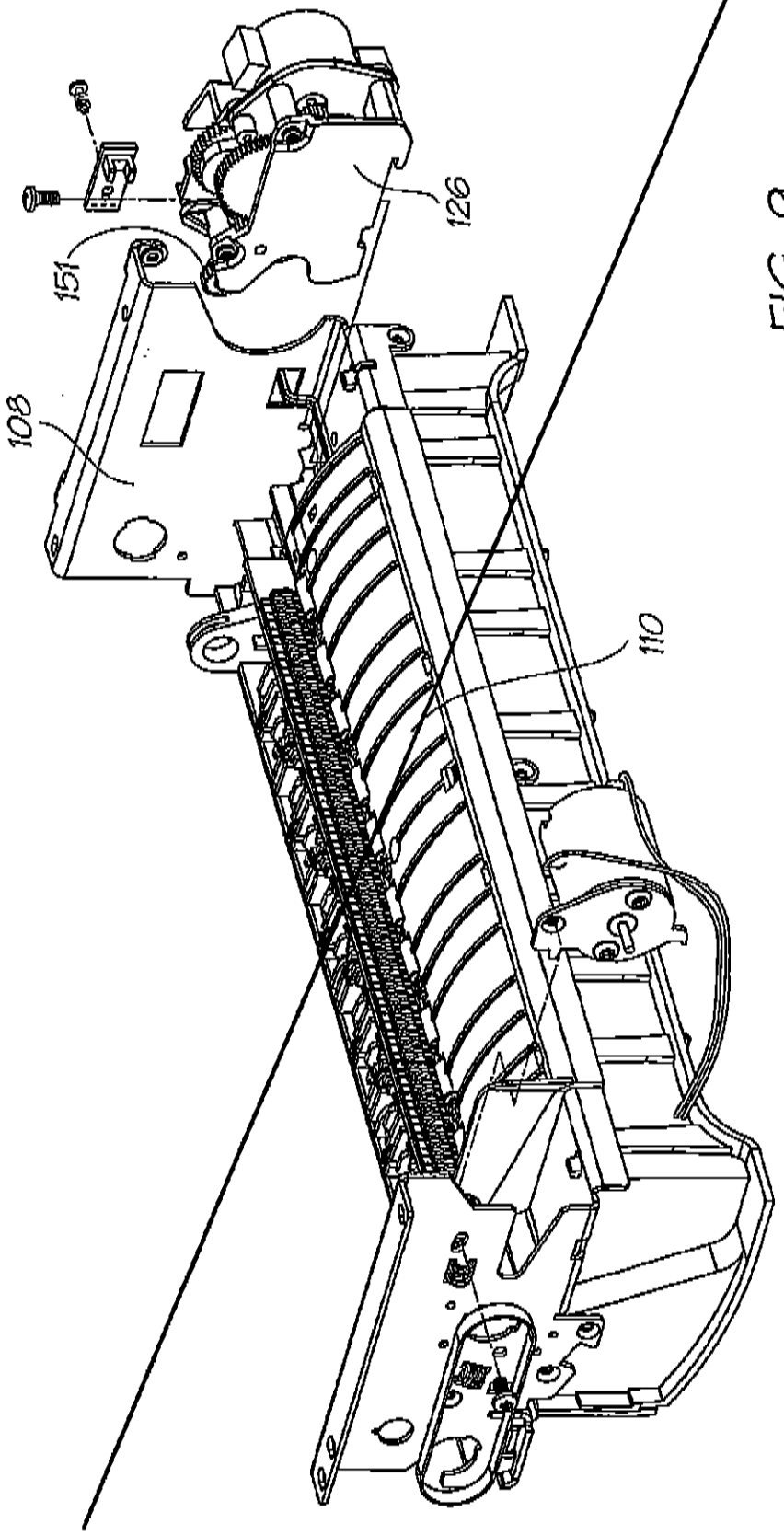


FIG. 9

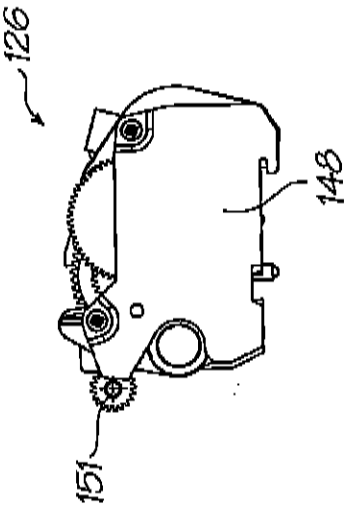


FIG. 10

FIG. 11

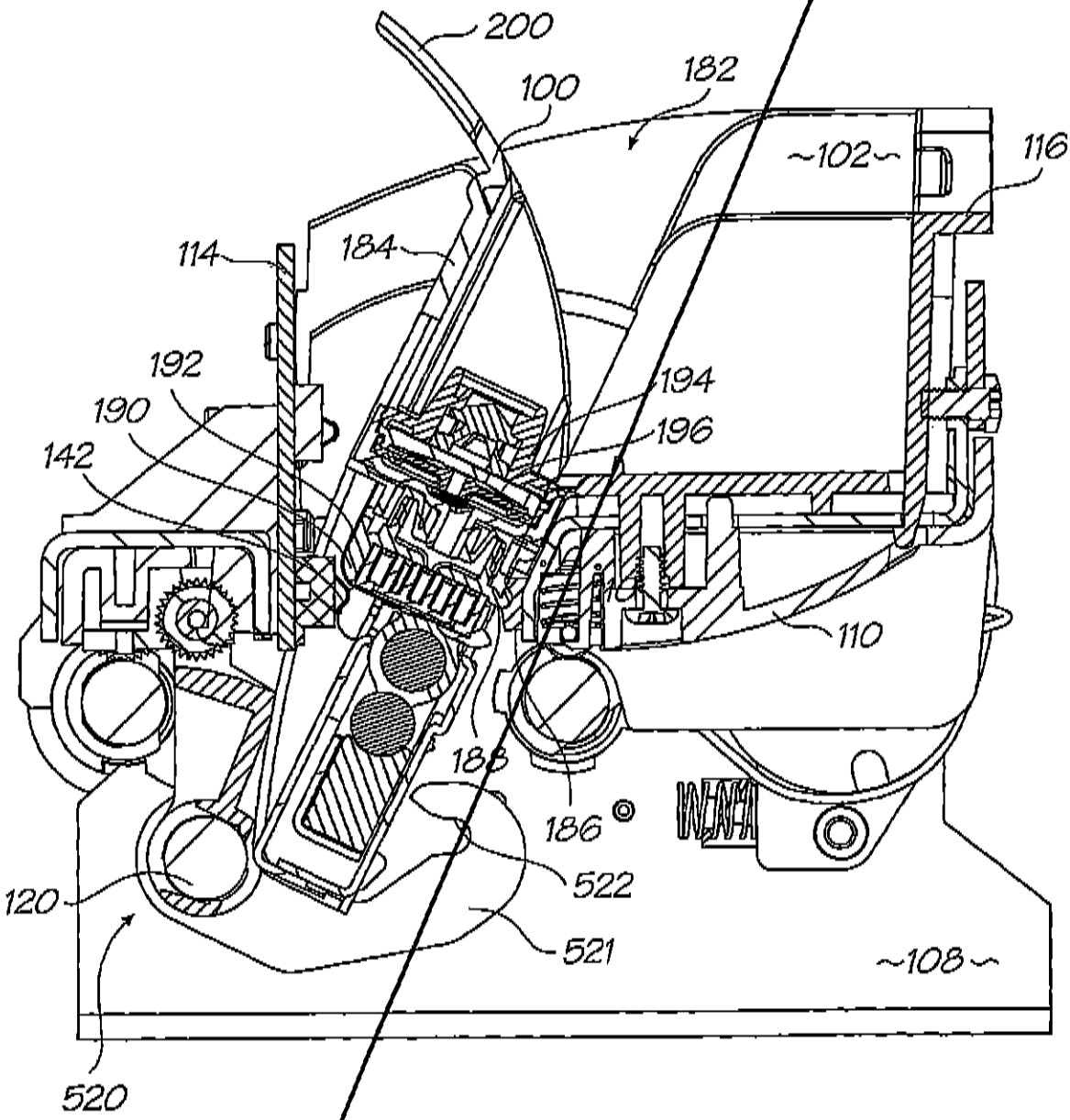

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FIG. 12

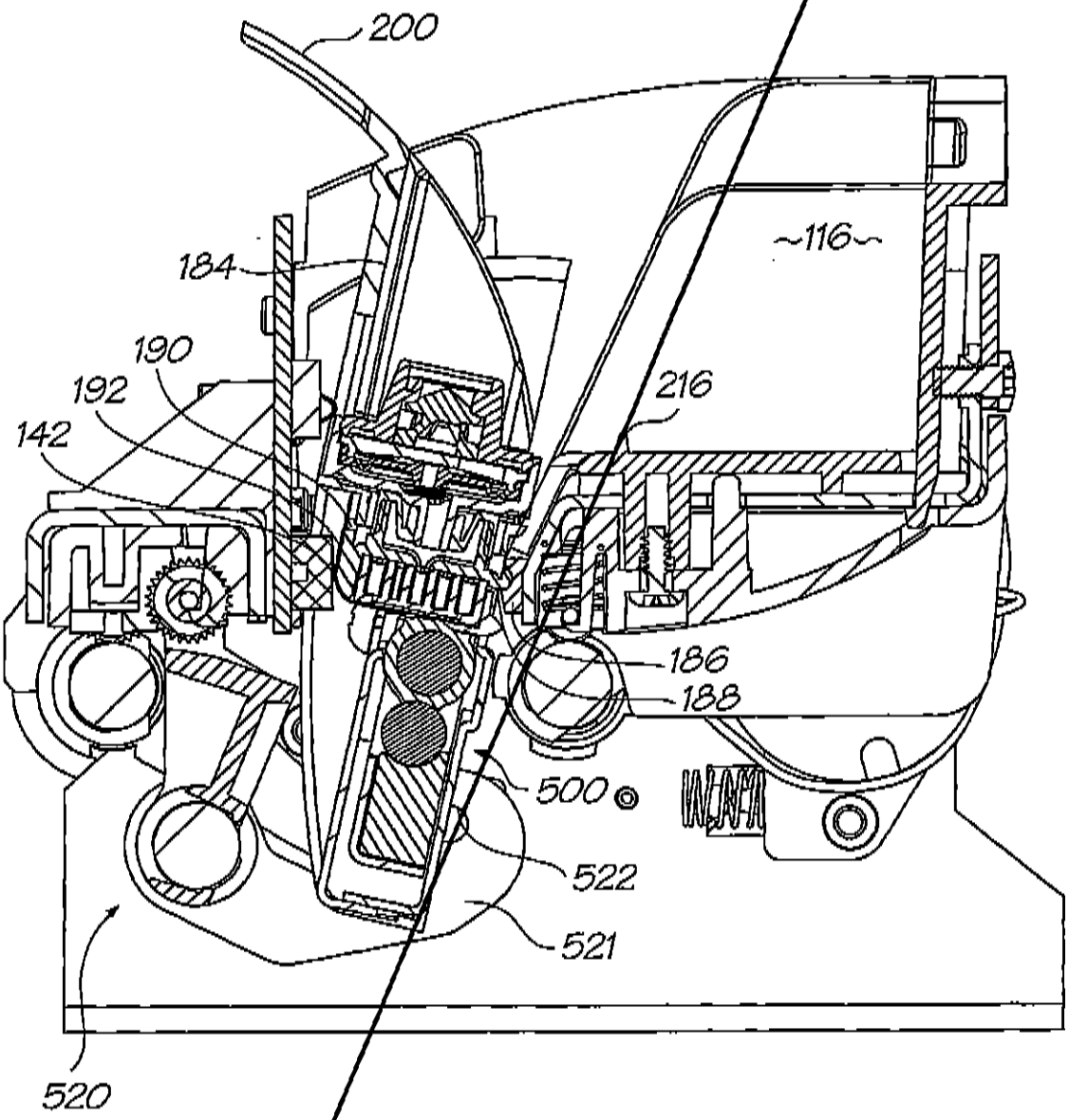


FIG. 13

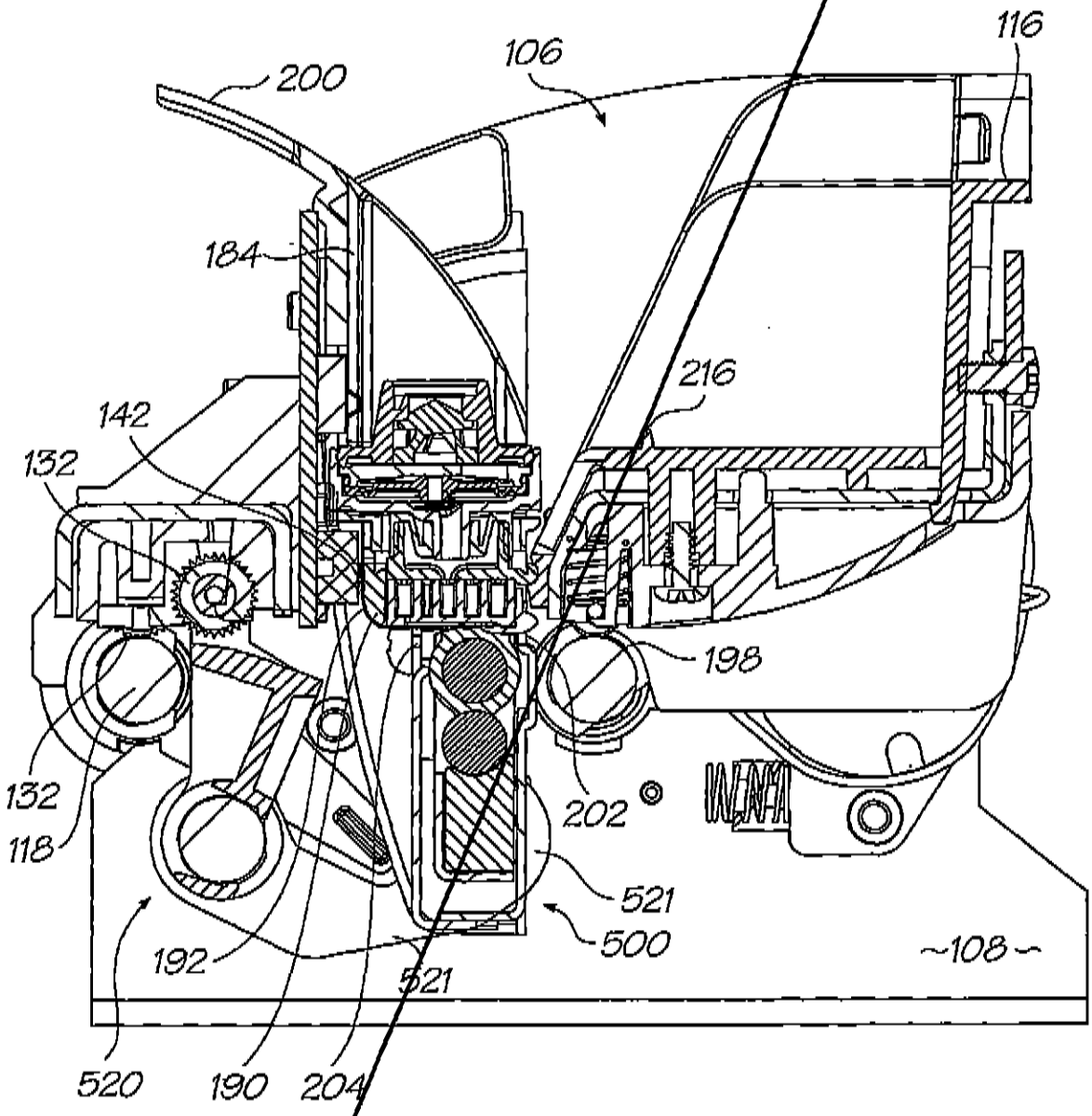

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FIG. 14

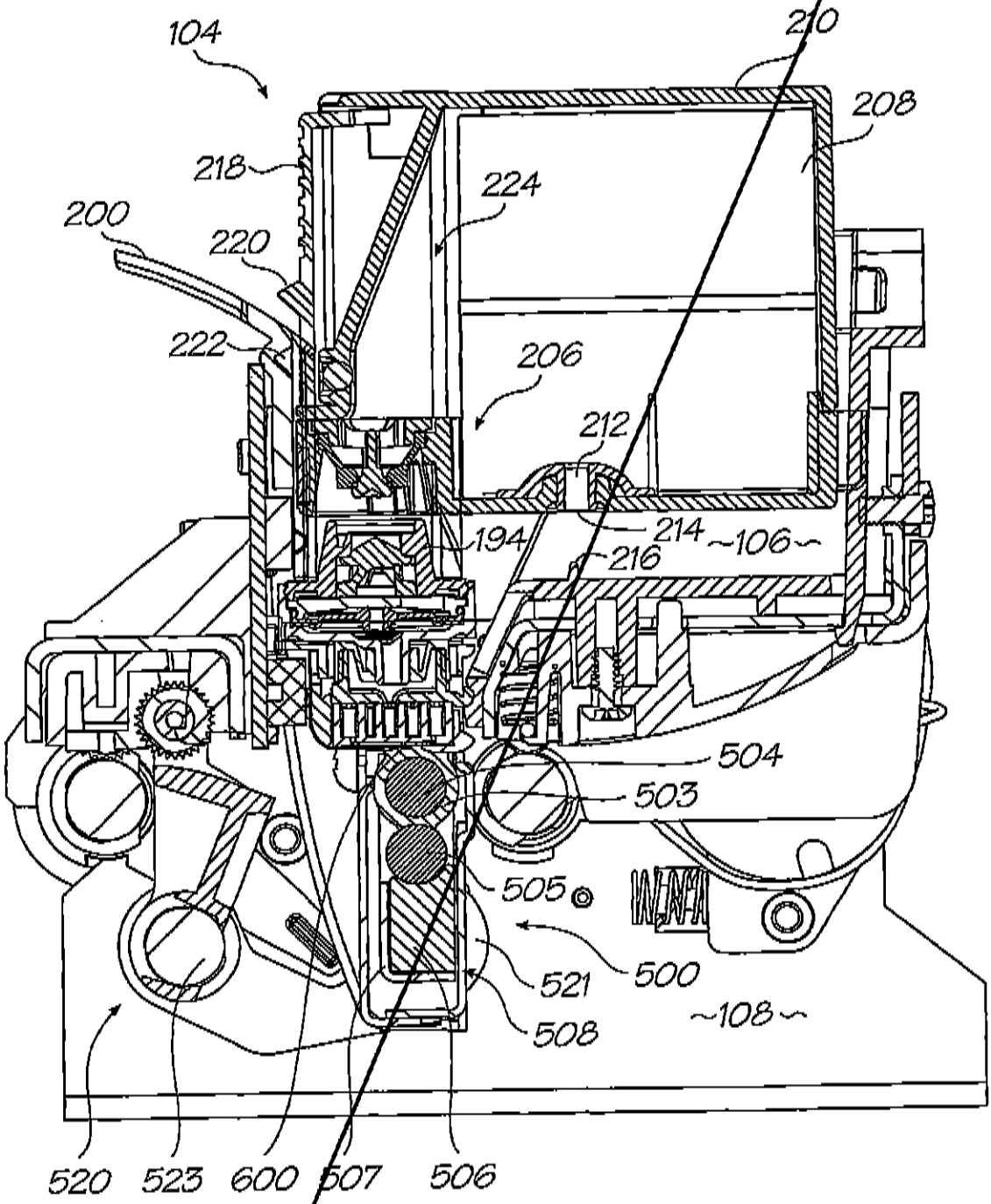

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FIG. 15

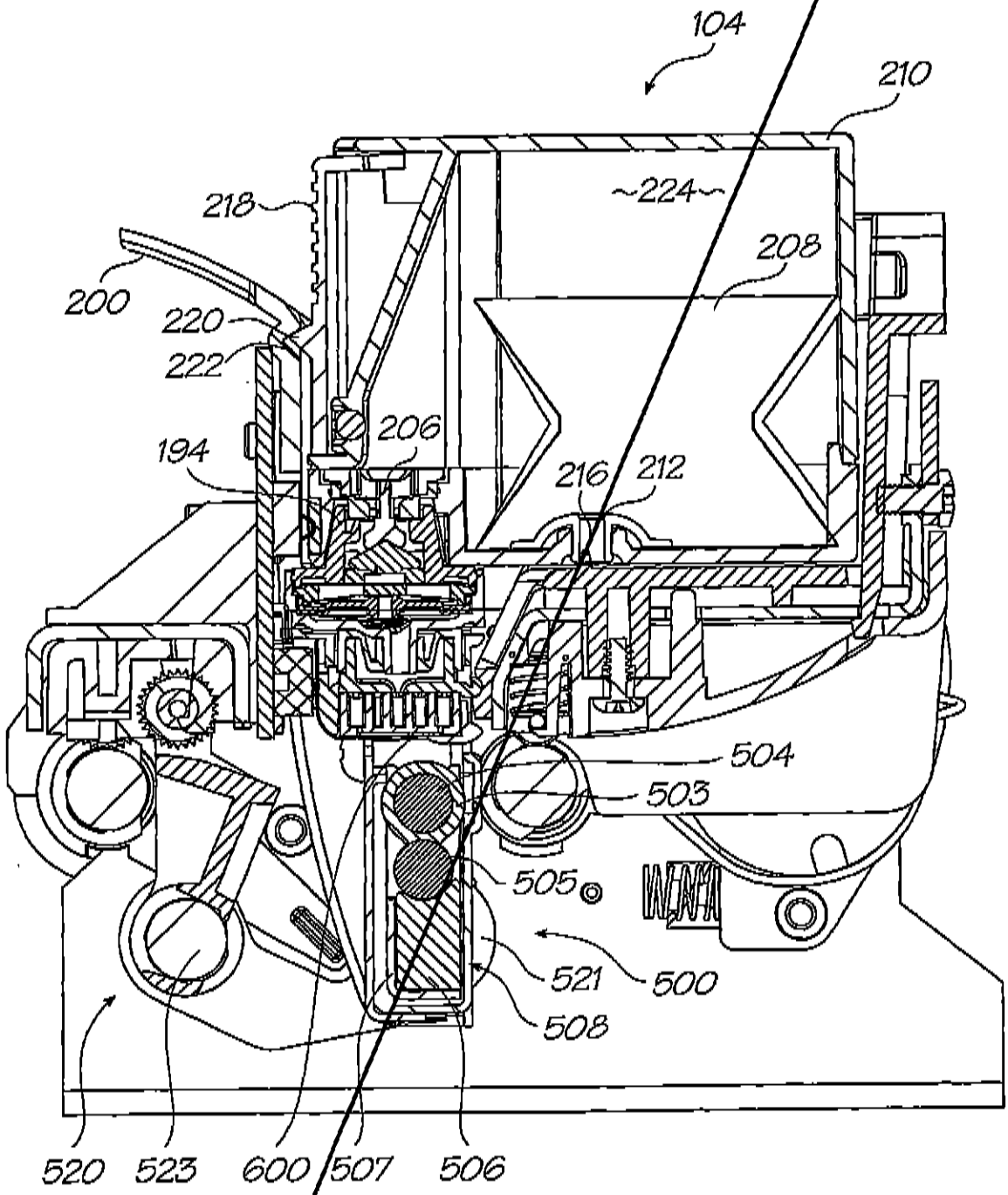

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FIG. 16

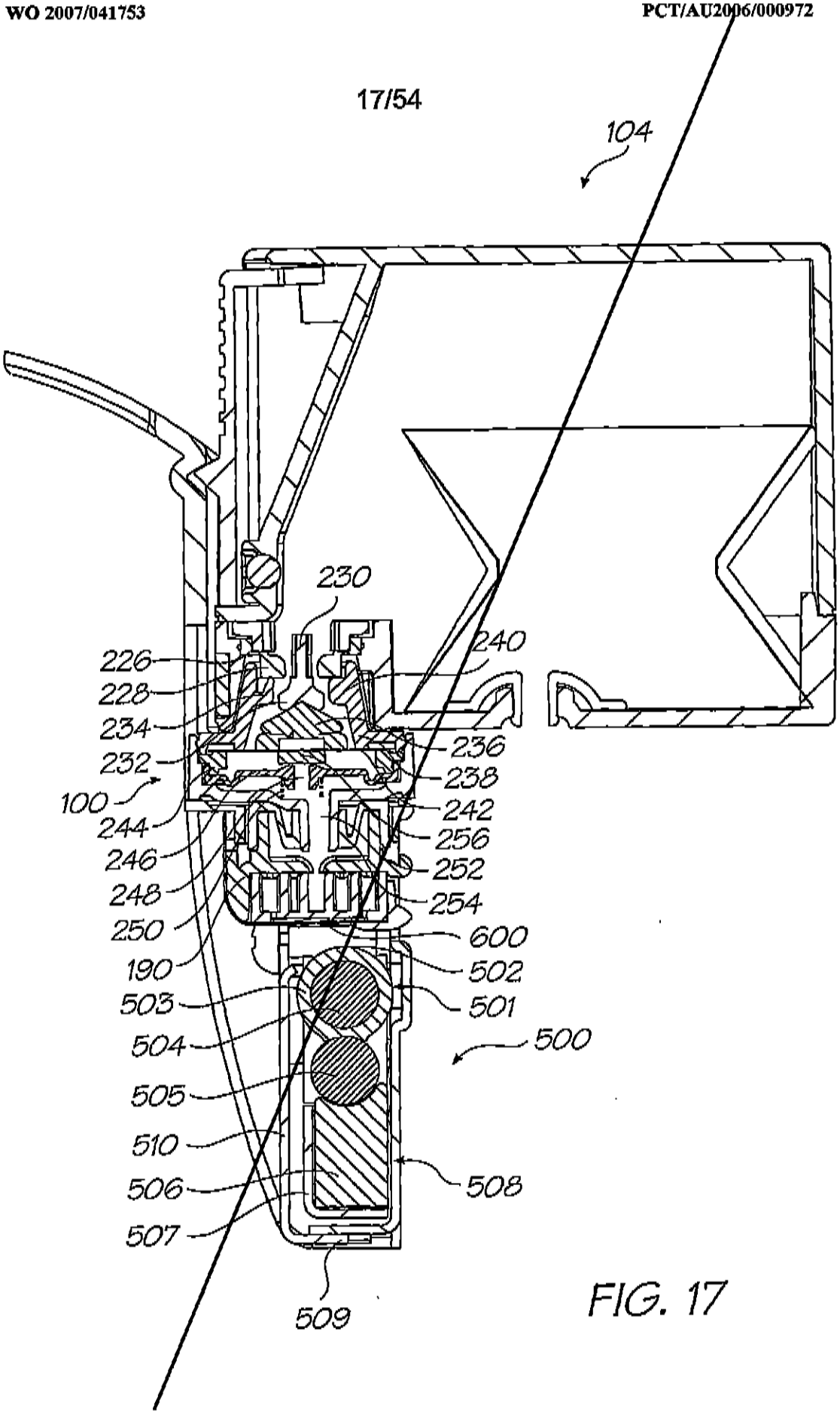

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FIG. 17

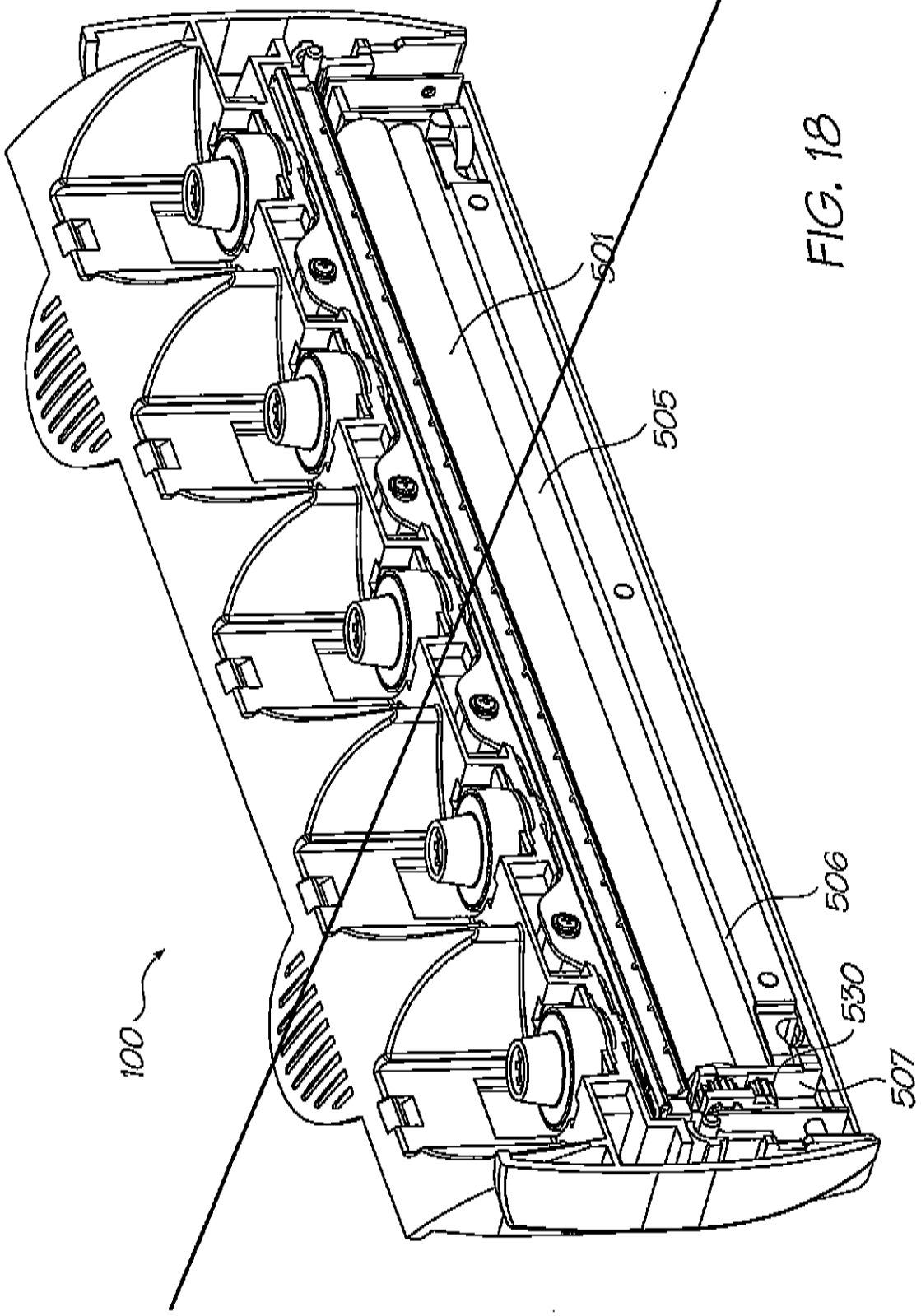


FIG. 18

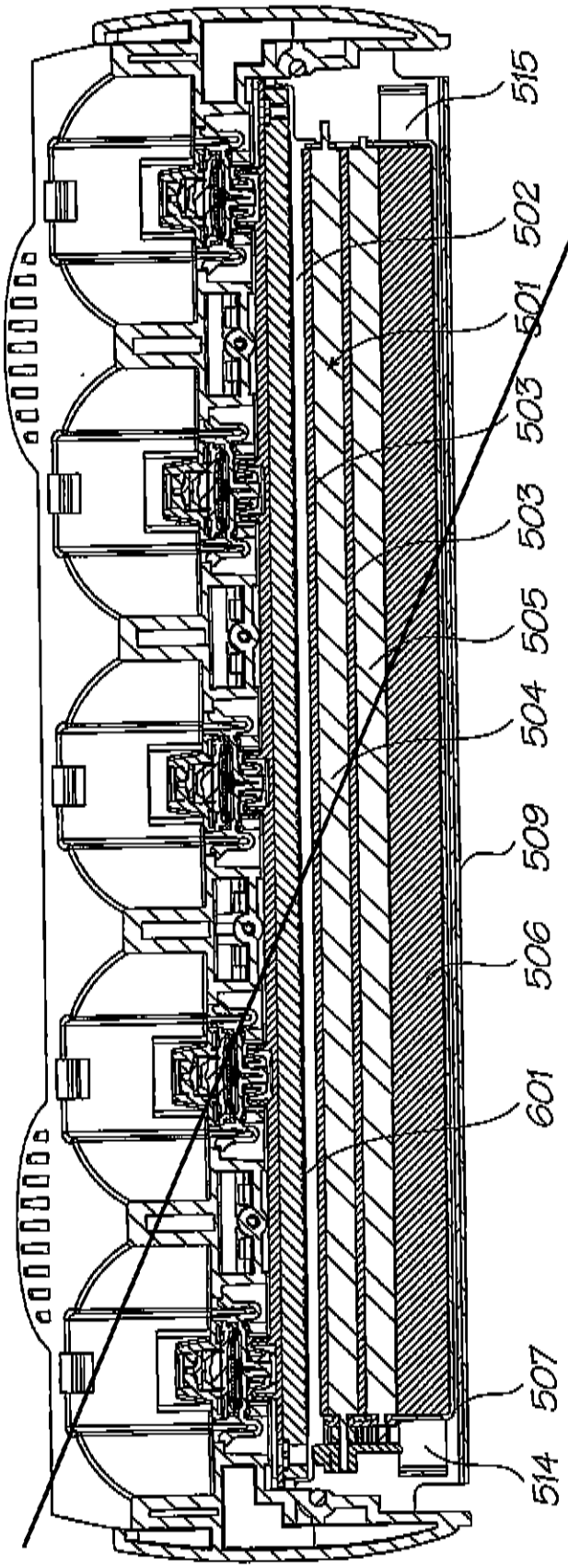


FIG. 19

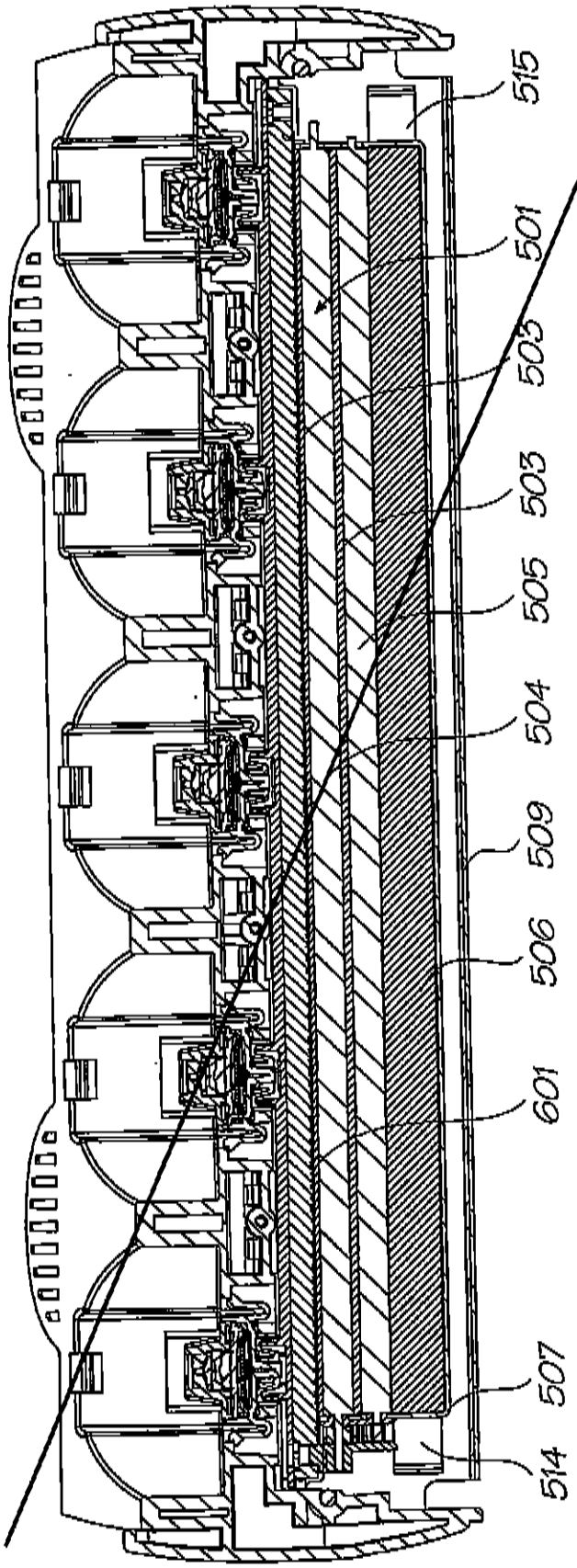


FIG. 20

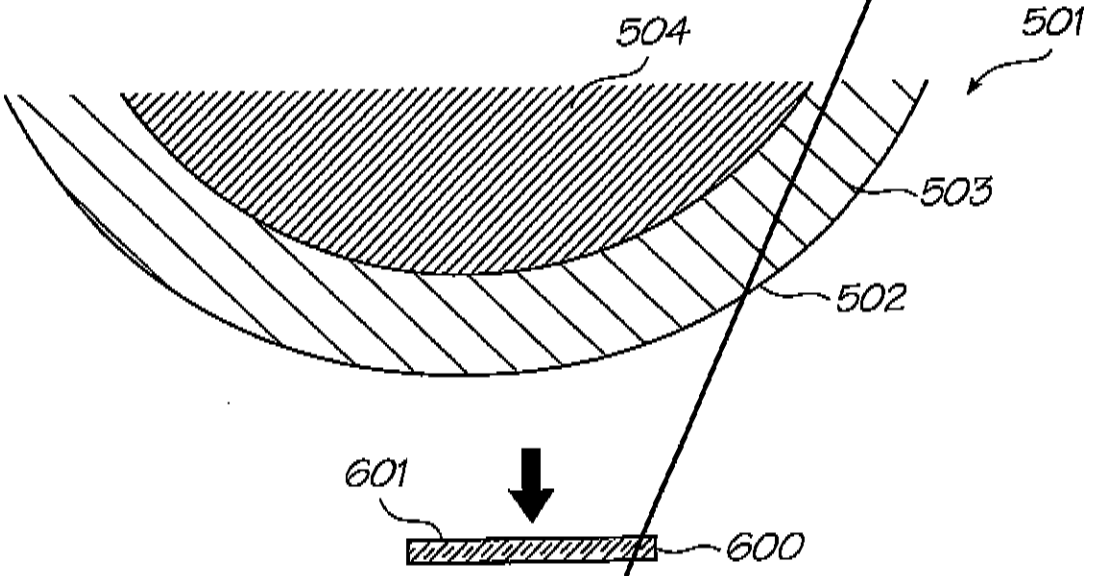


FIG. 21A

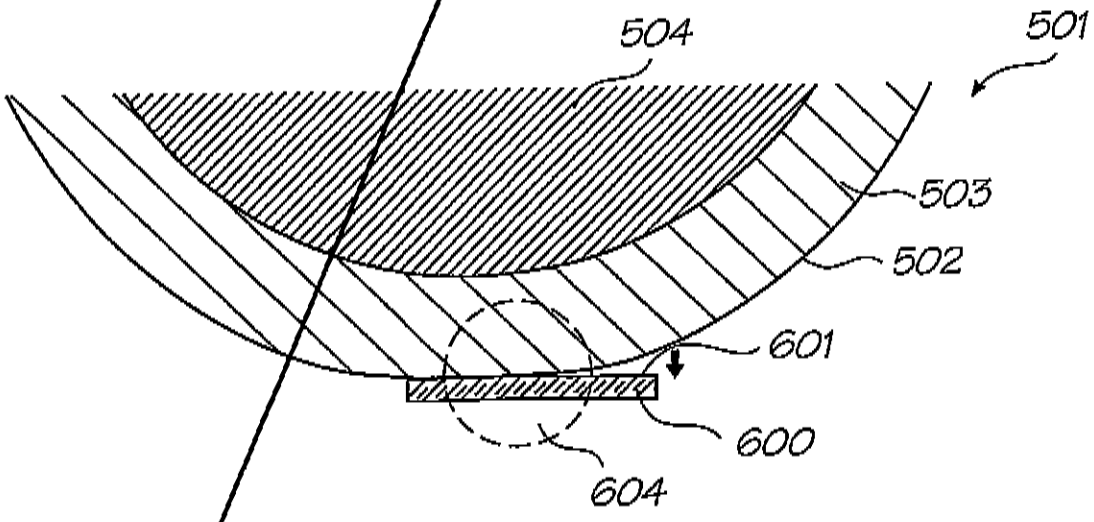


FIG. 21B

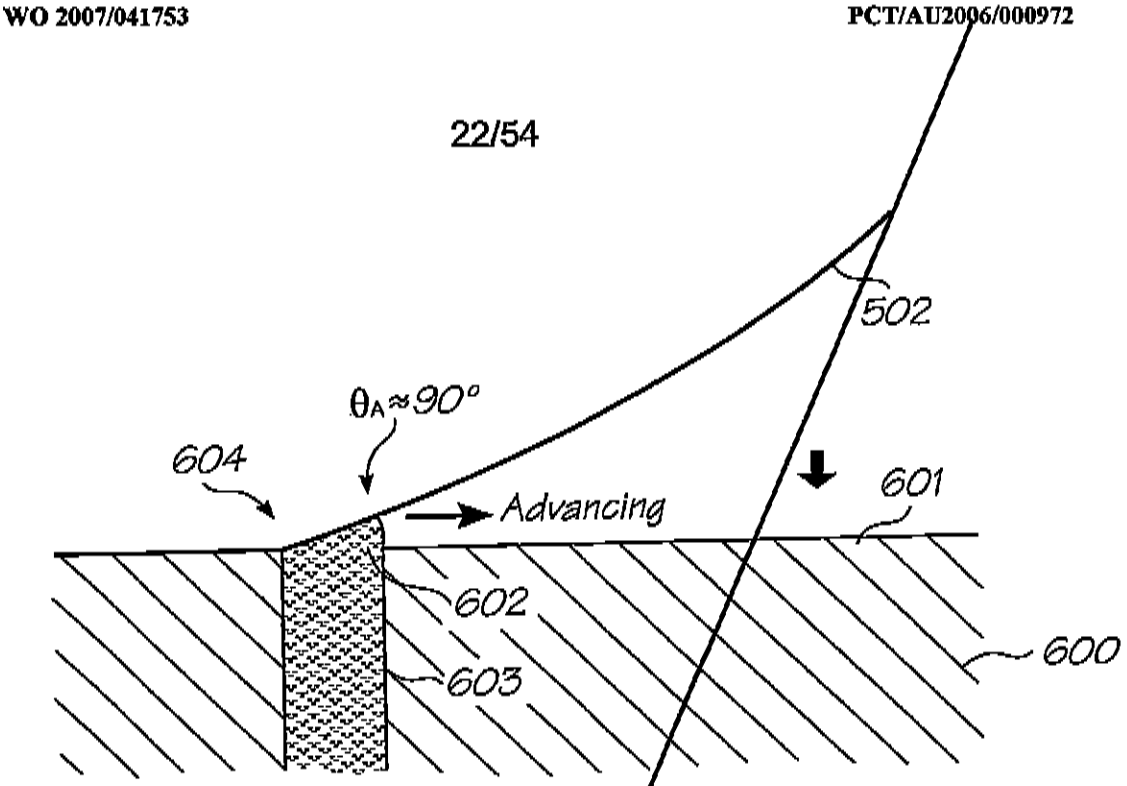


FIG. 21C

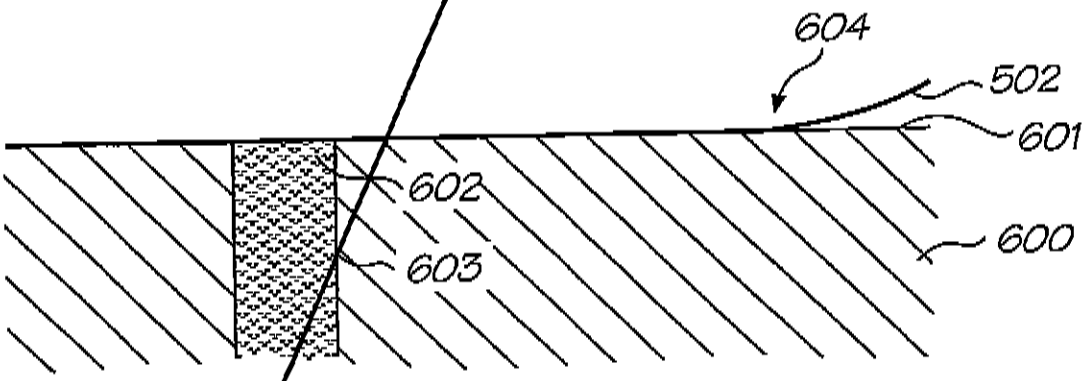


FIG. 21D

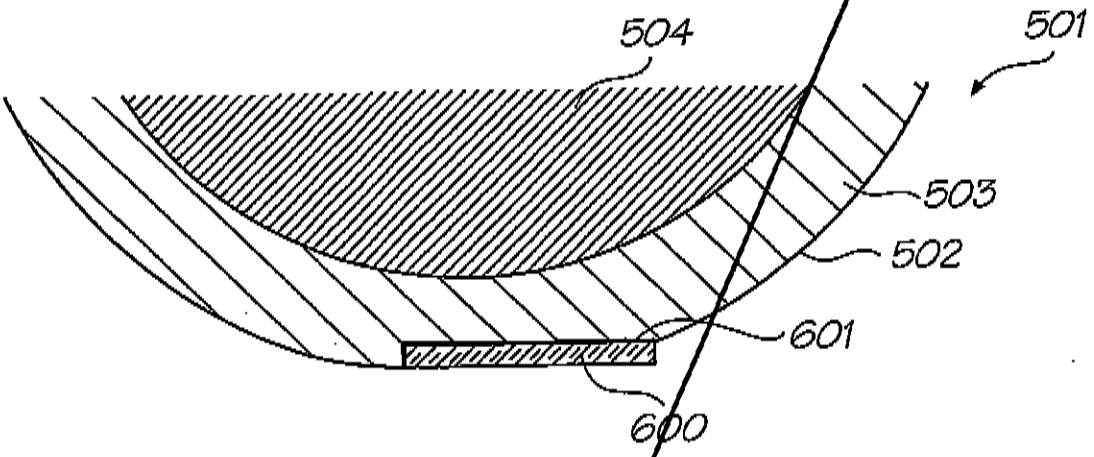


FIG. 22A

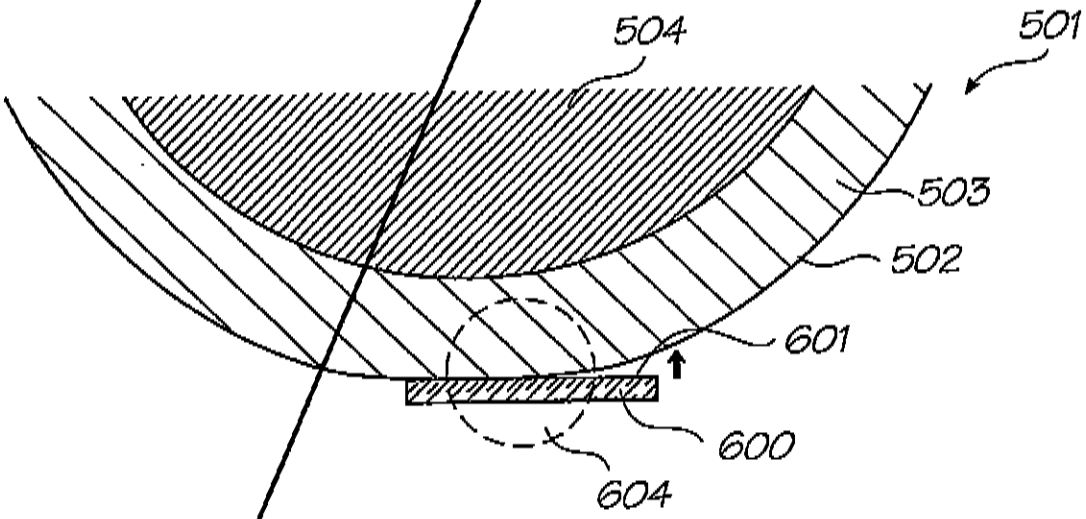


FIG. 22B

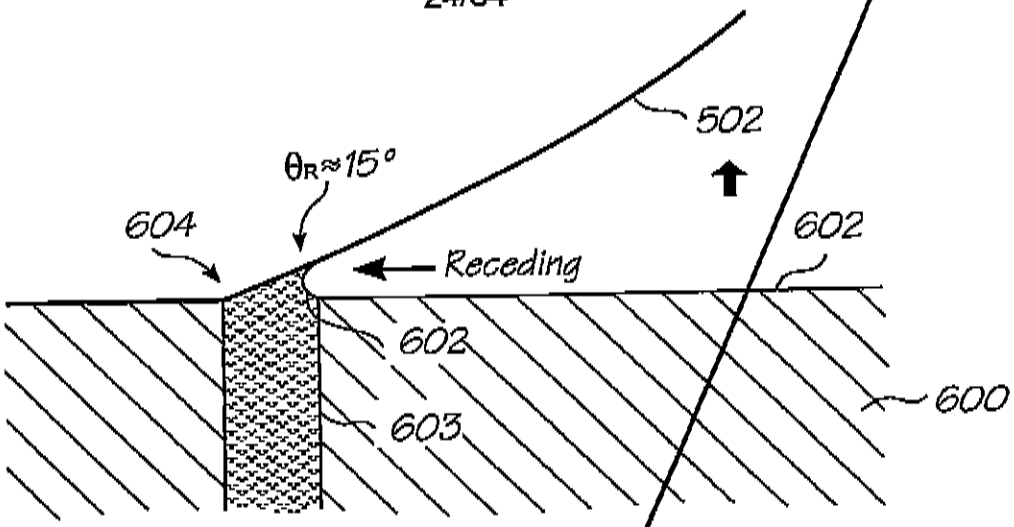


FIG. 22C

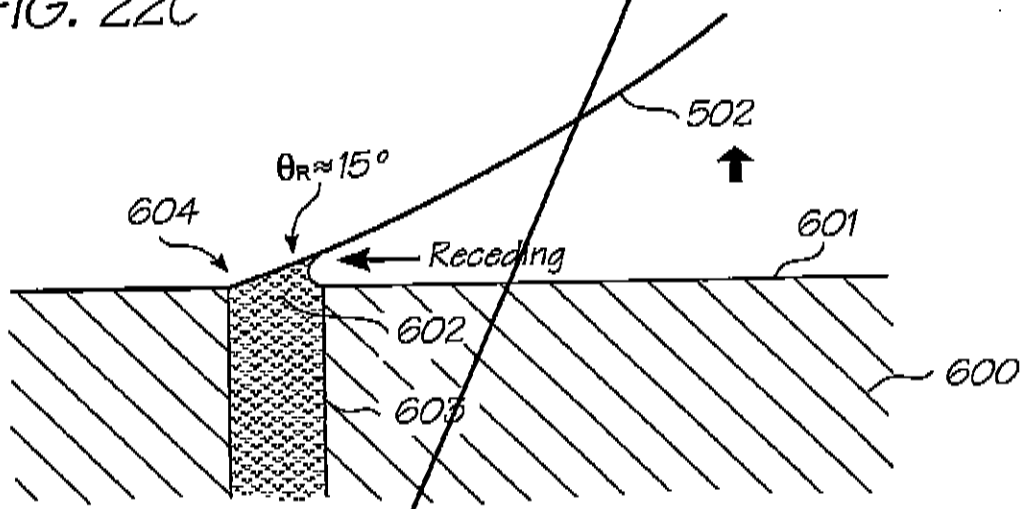


FIG. 22D

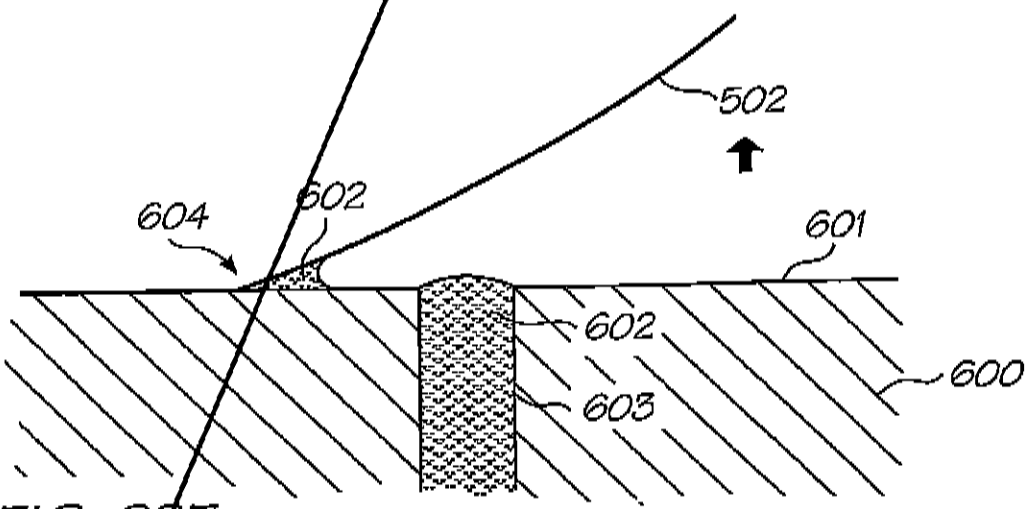


FIG. 22E

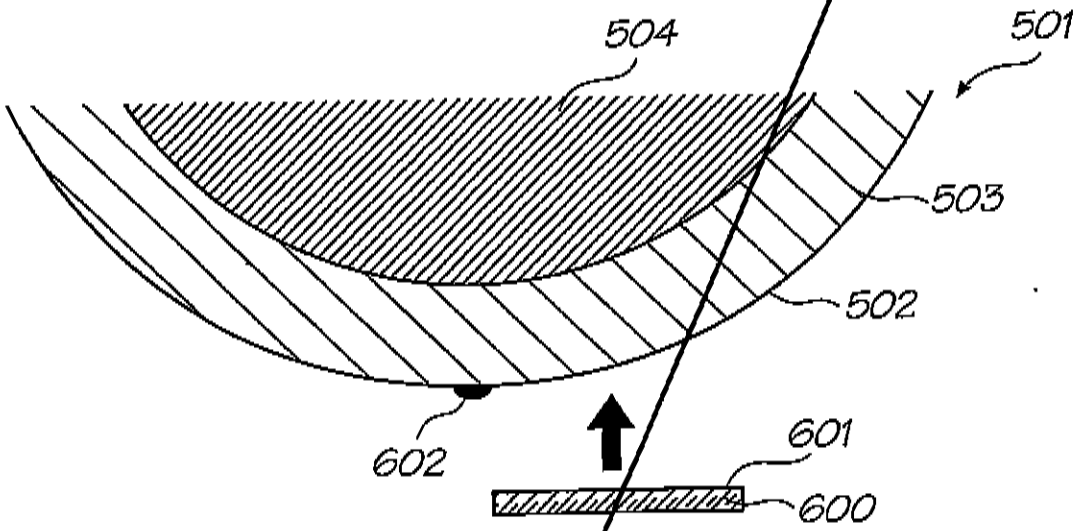


FIG. 23

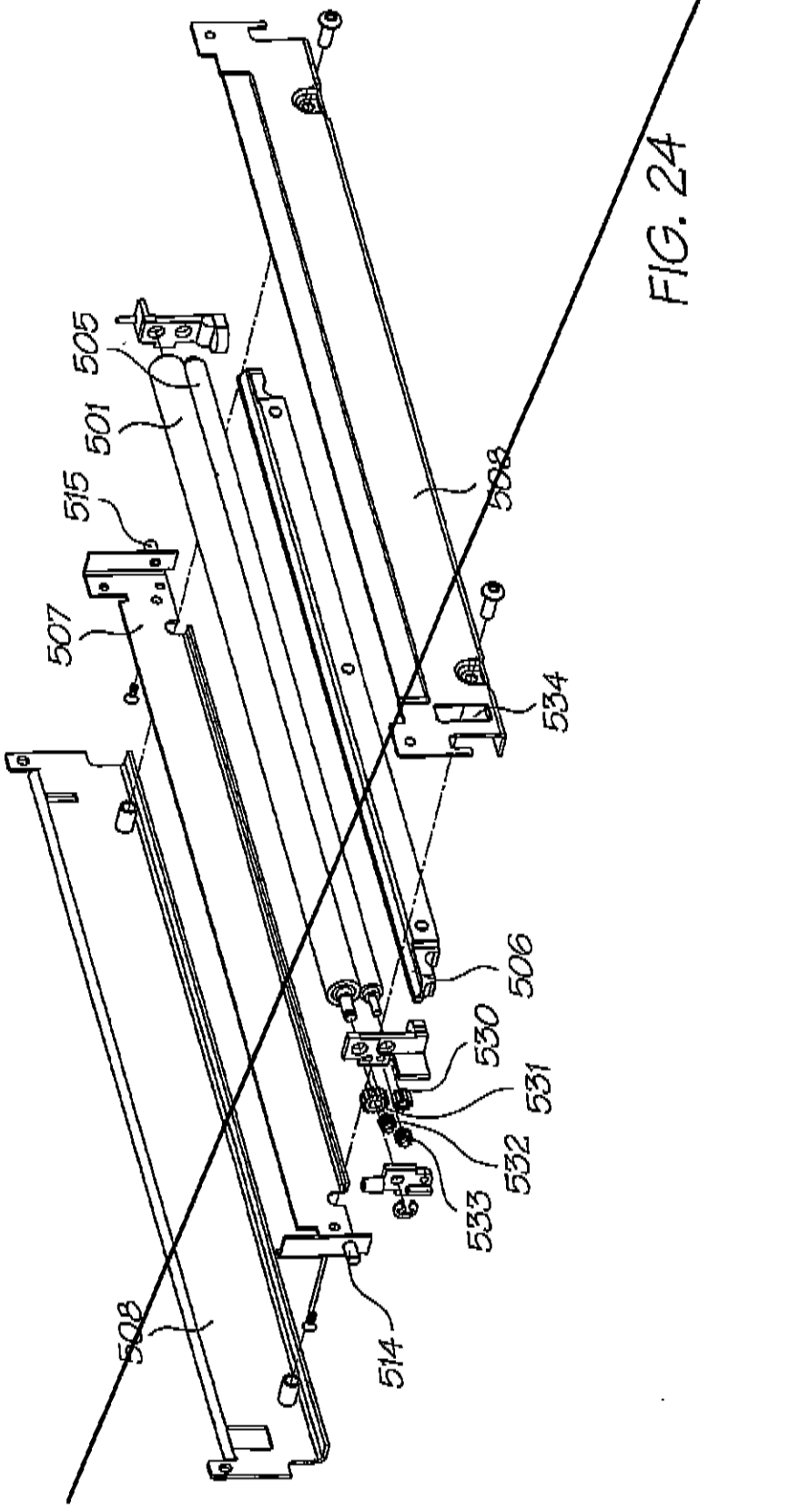


FIG. 24

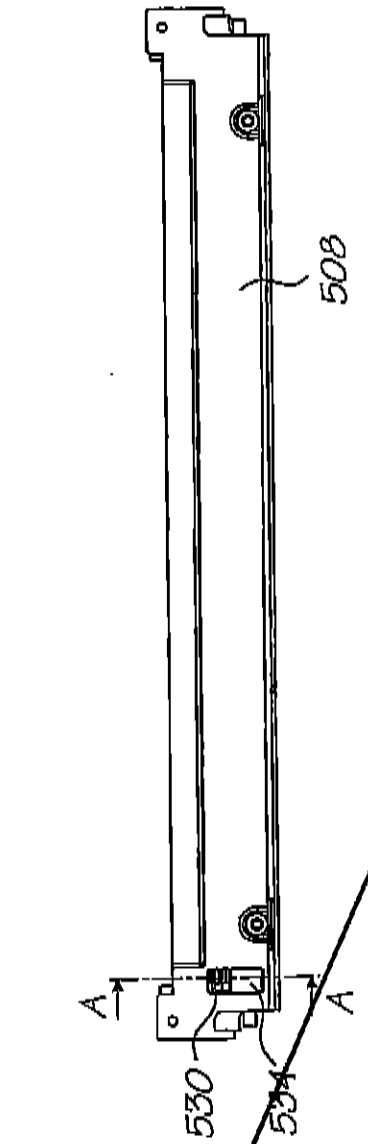


FIG. 25

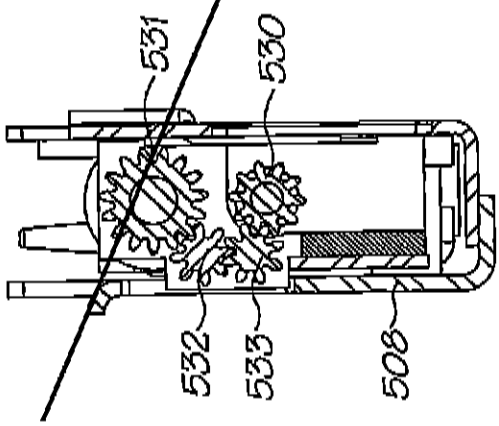


FIG. 26

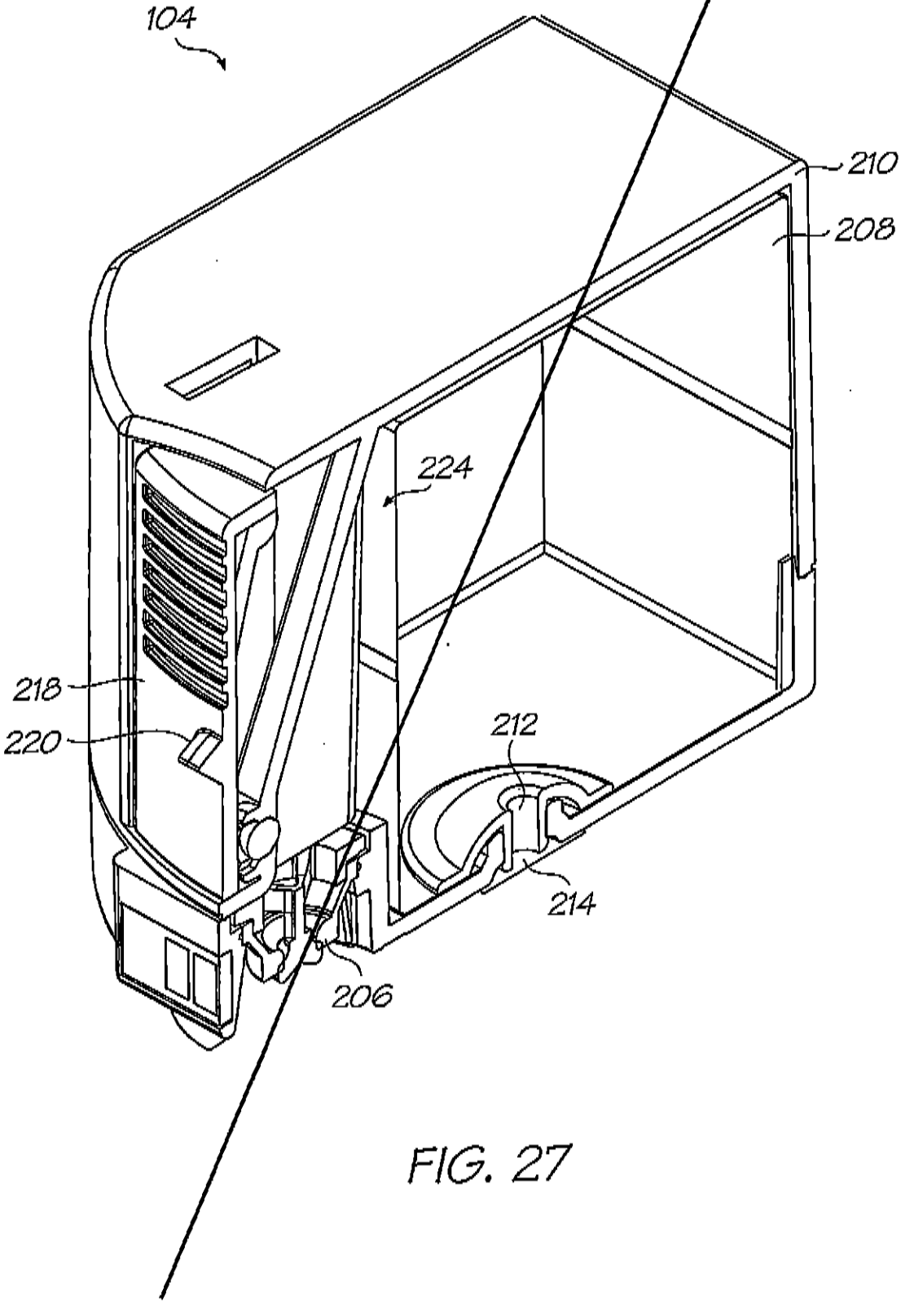


FIG. 27

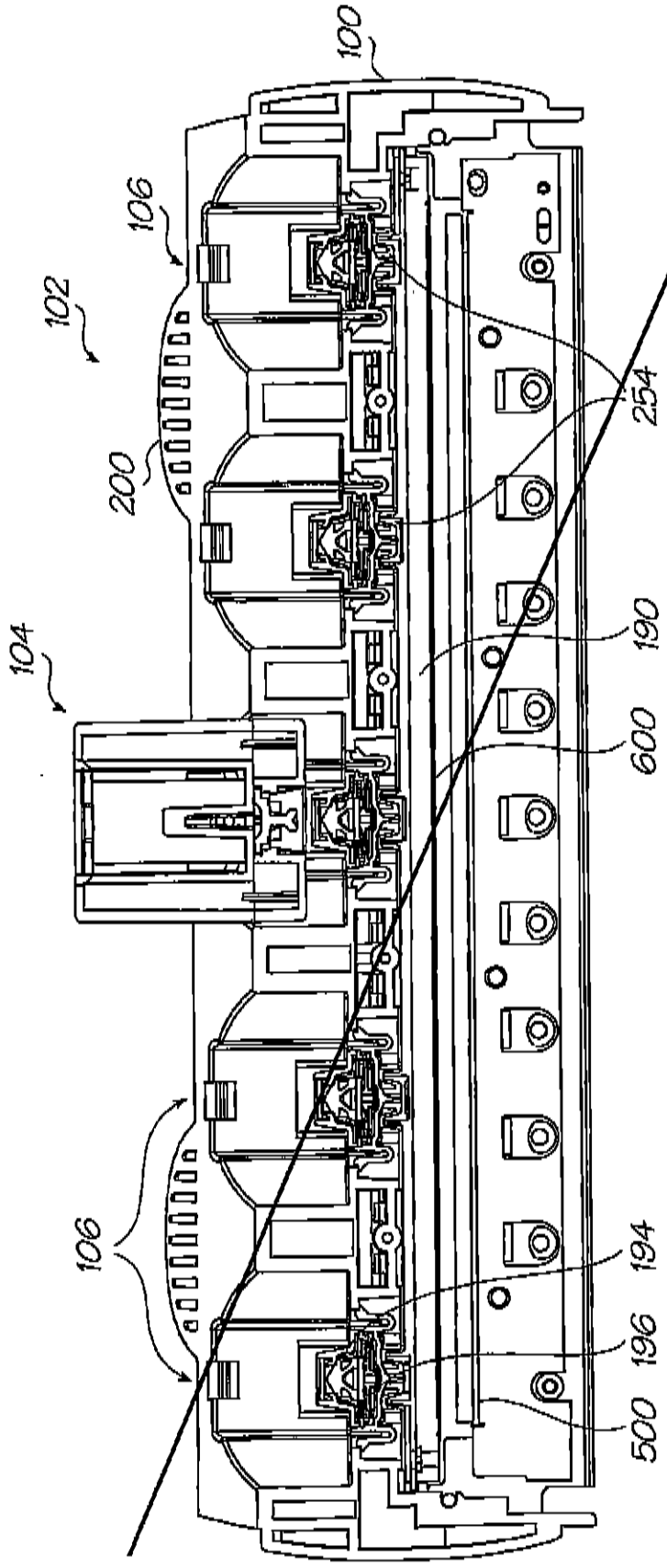


FIG. 28

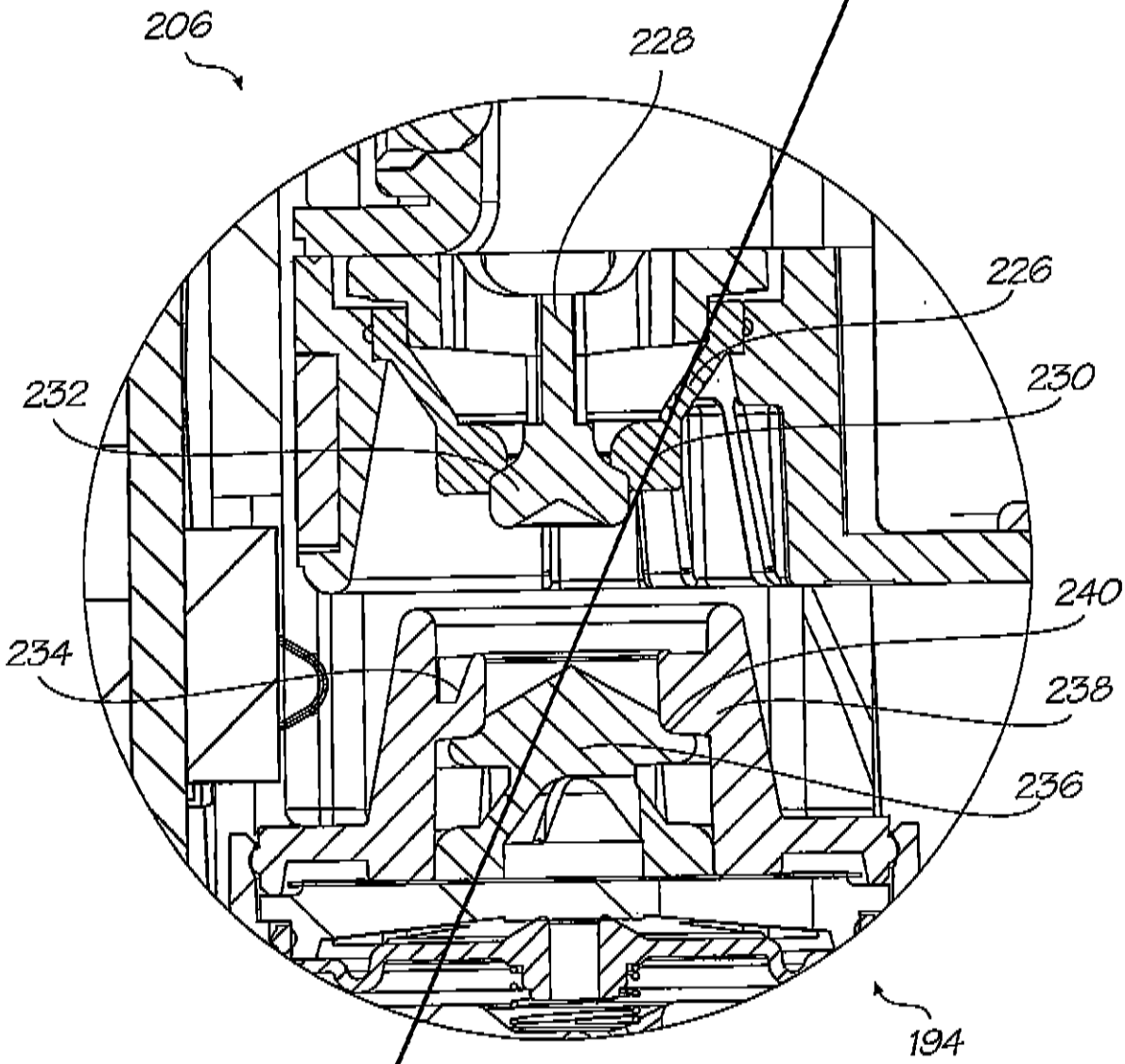


FIG. 29

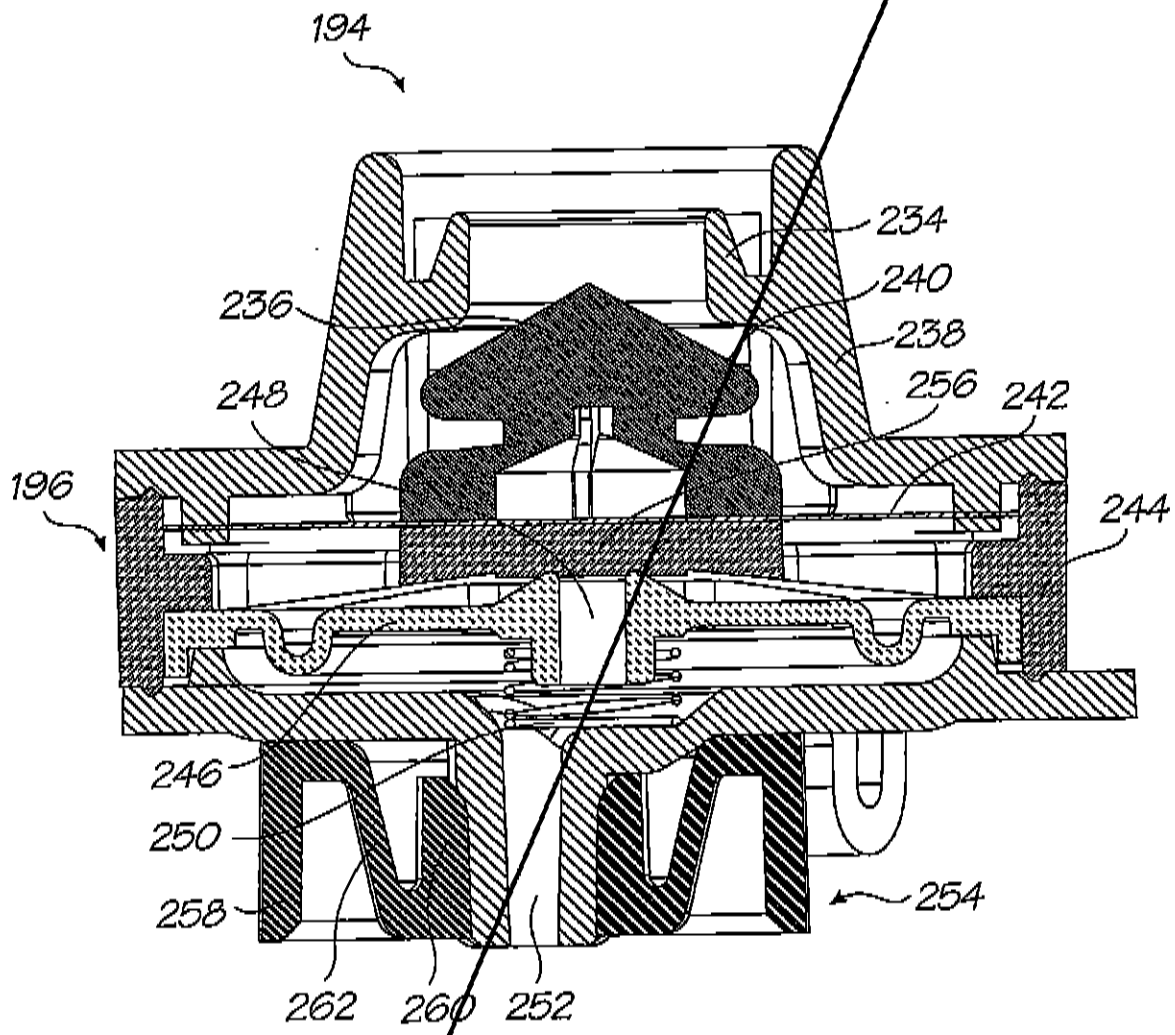

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FIG. 30A

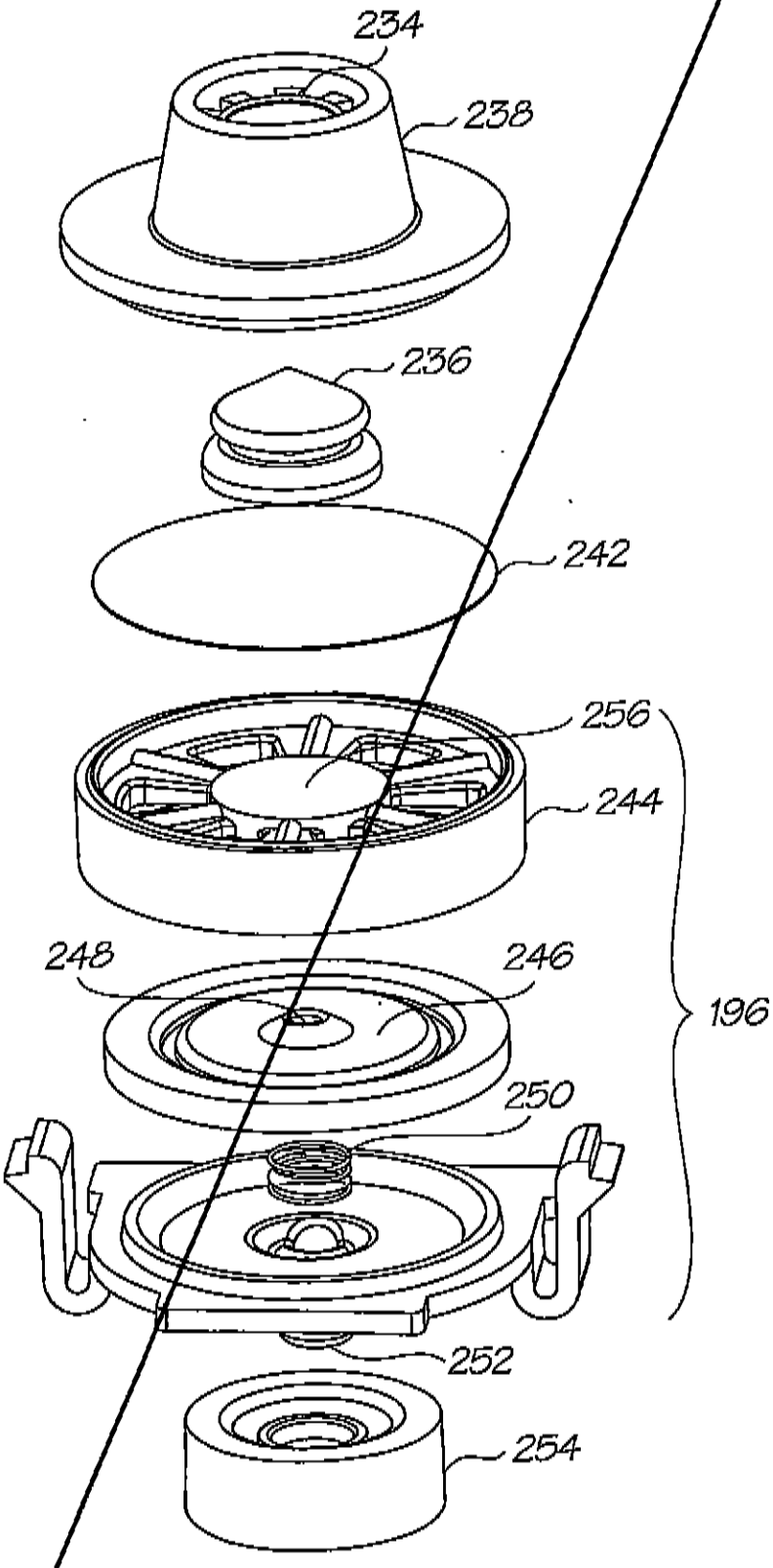


FIG. 30B

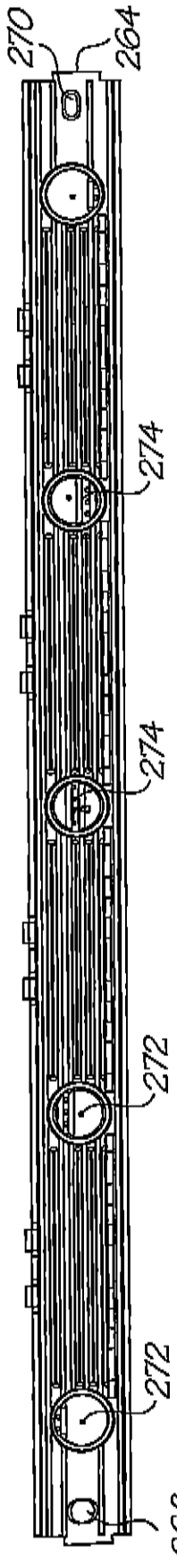


FIG. 31A

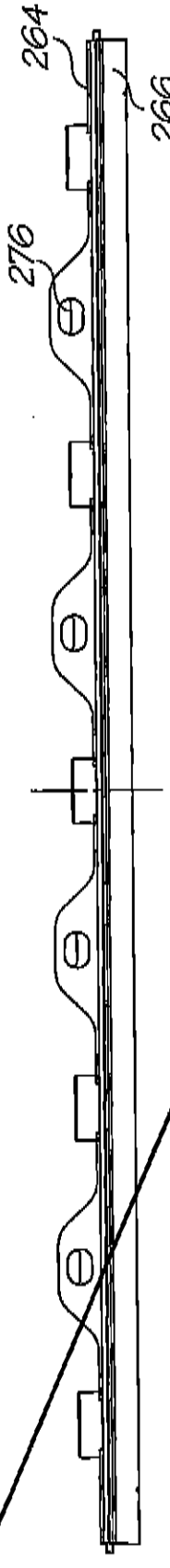


FIG. 31B

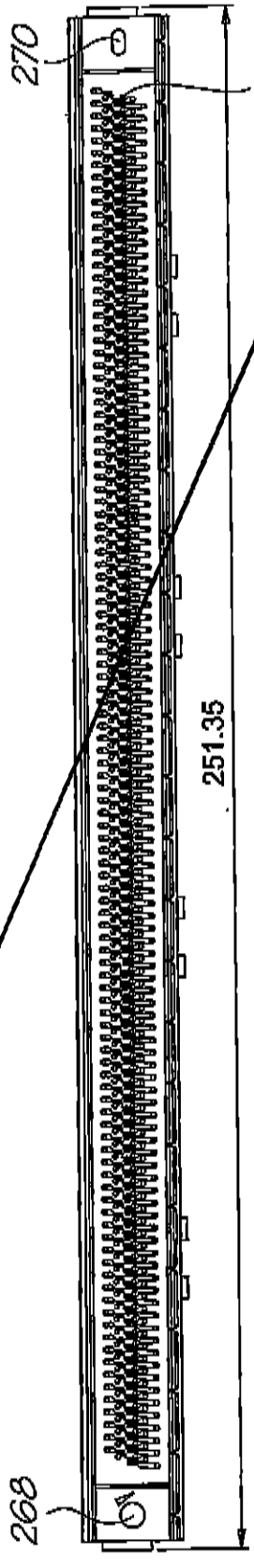


FIG. 31C

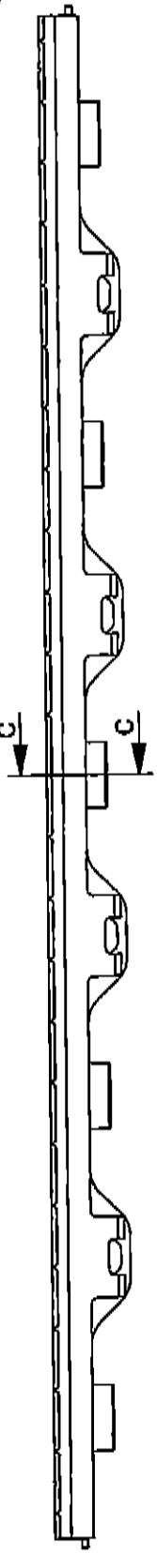


FIG. 31D

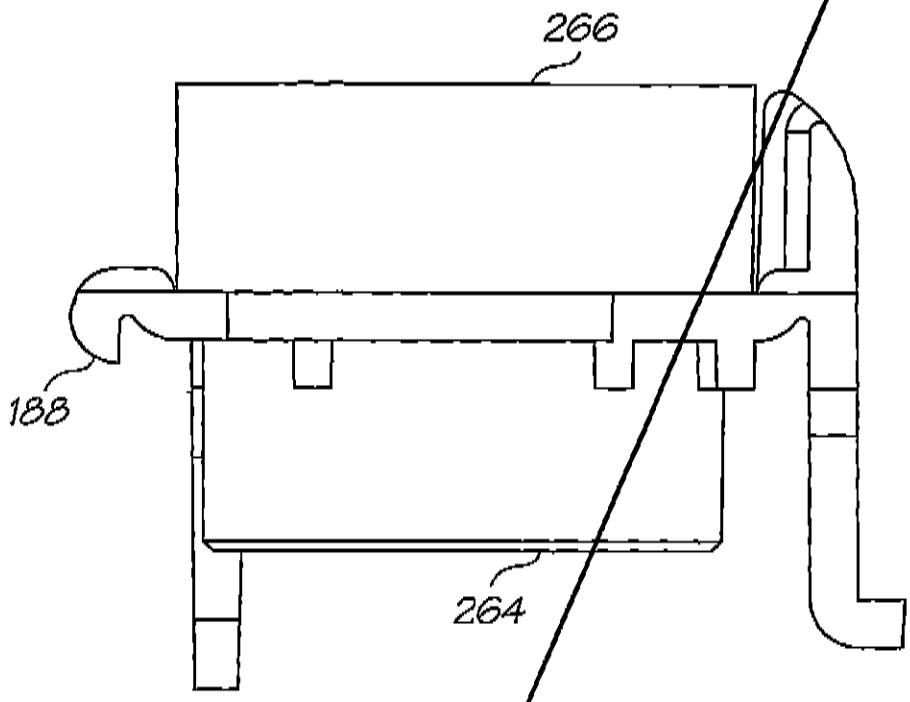


FIG. 31E

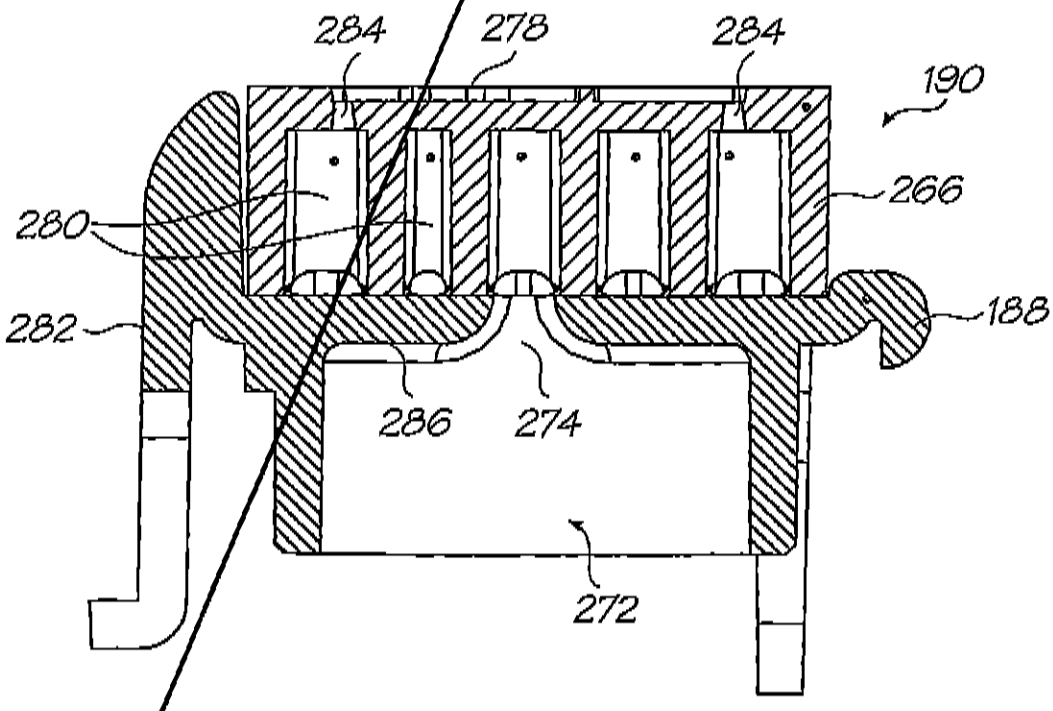


FIG. 32

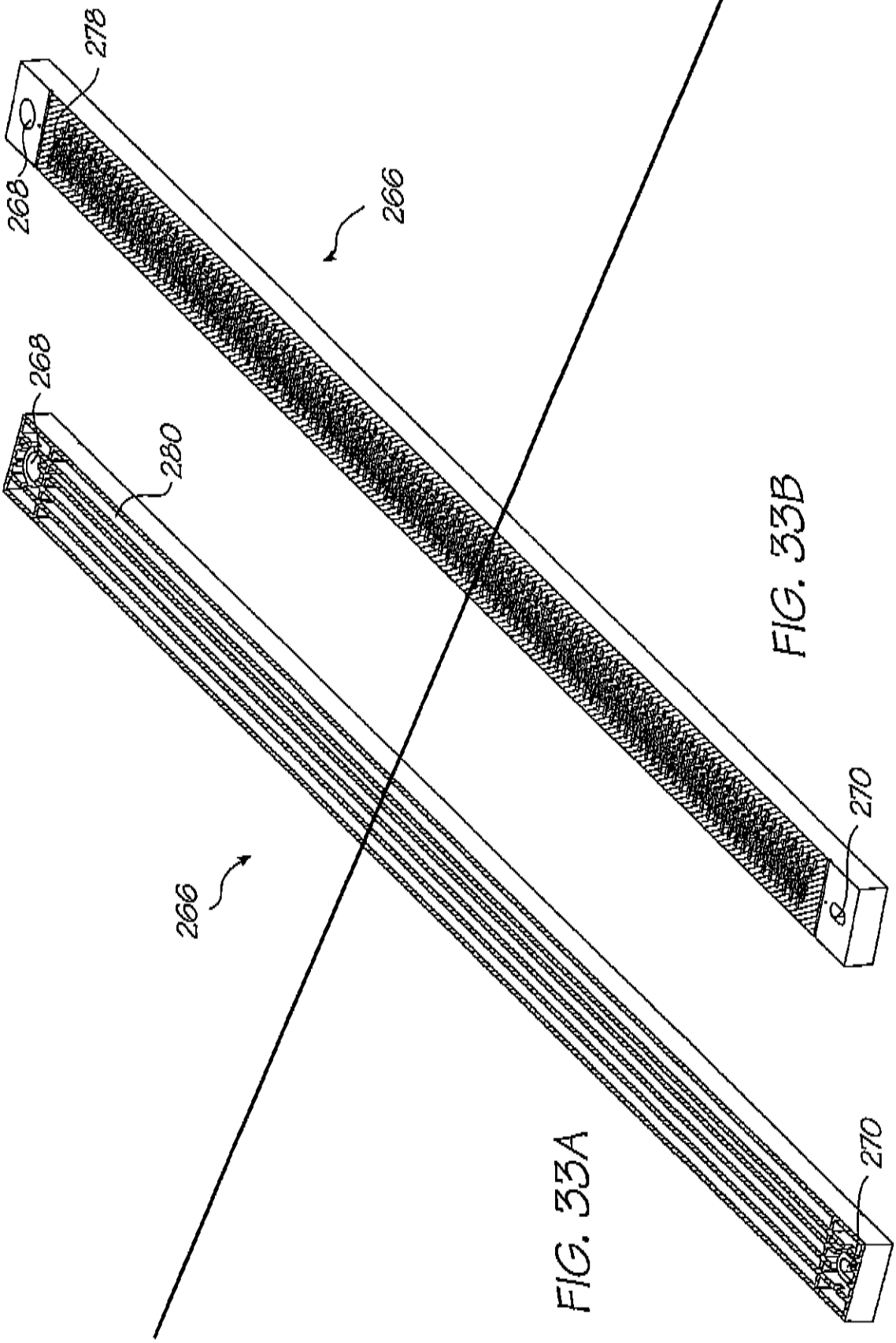


FIG. 33B

FIG. 33A

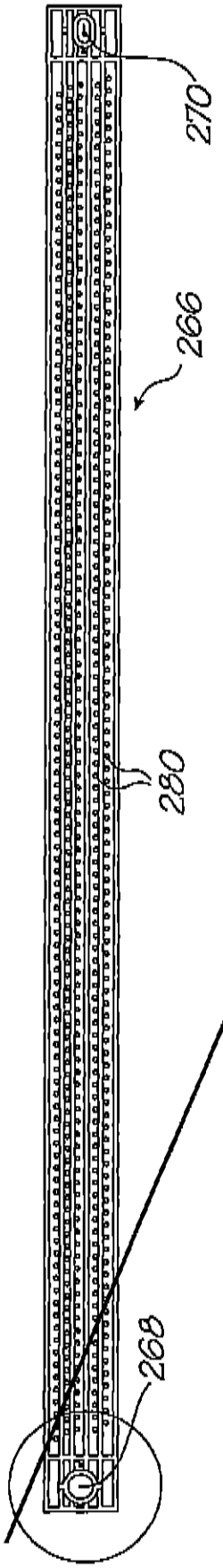


FIG. 34

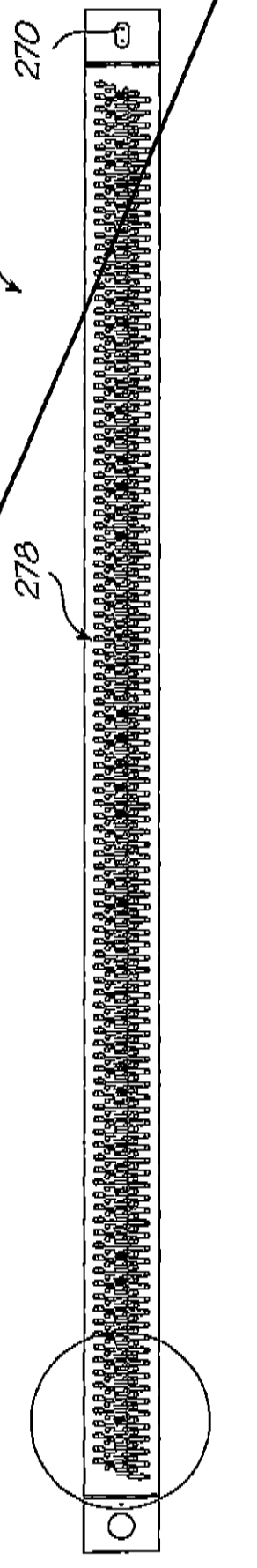


FIG. 36

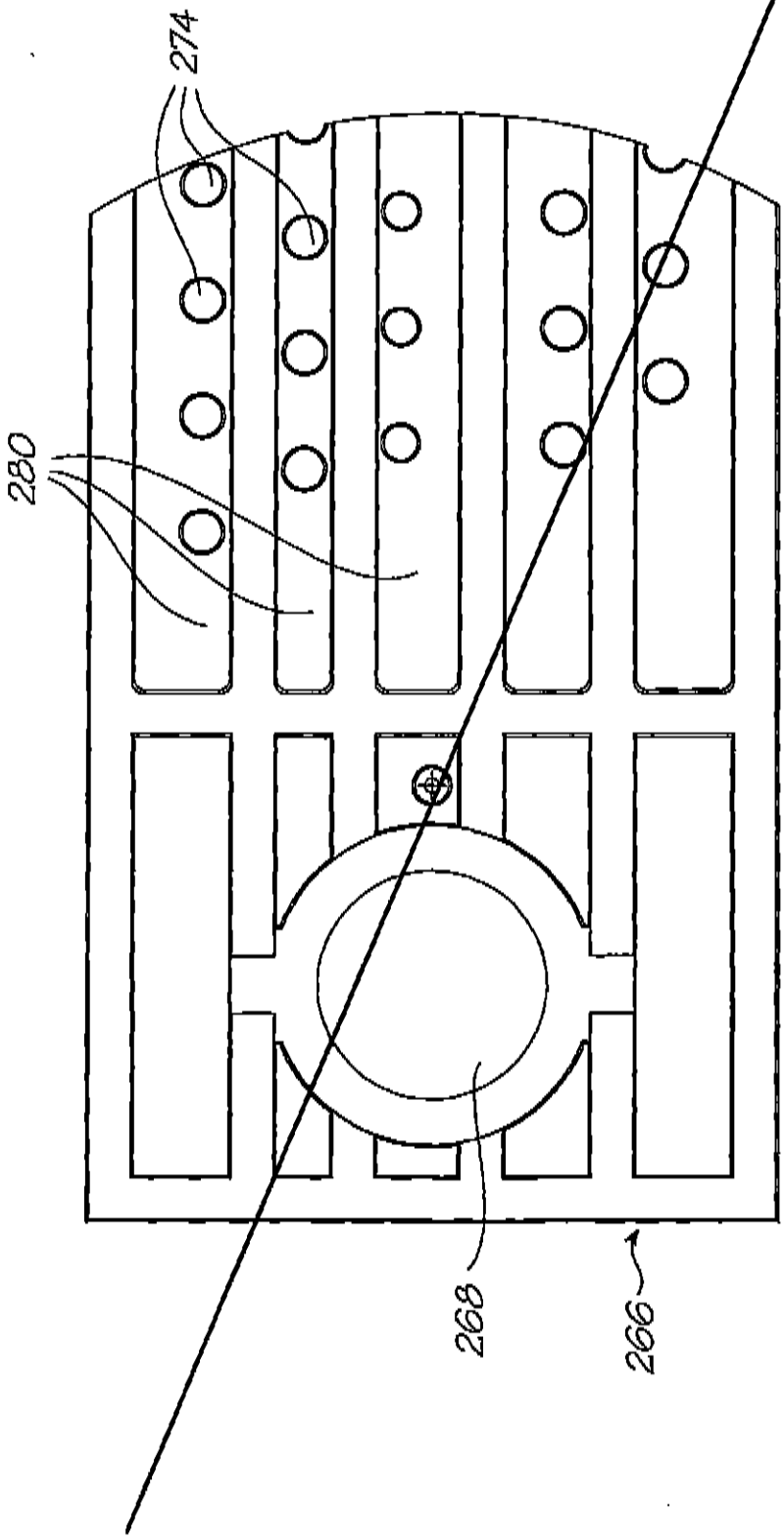


FIG. 35

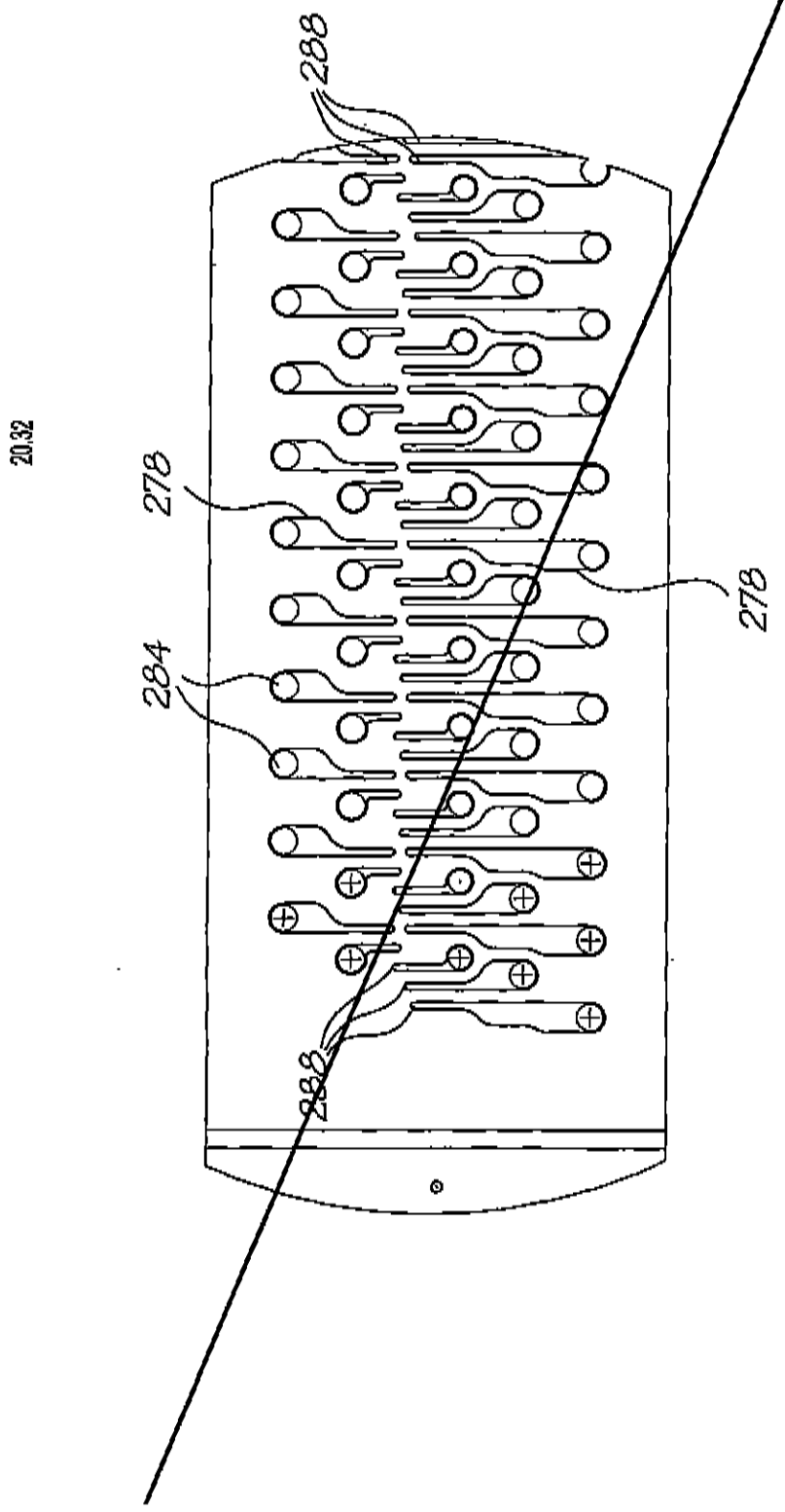


FIG. 37

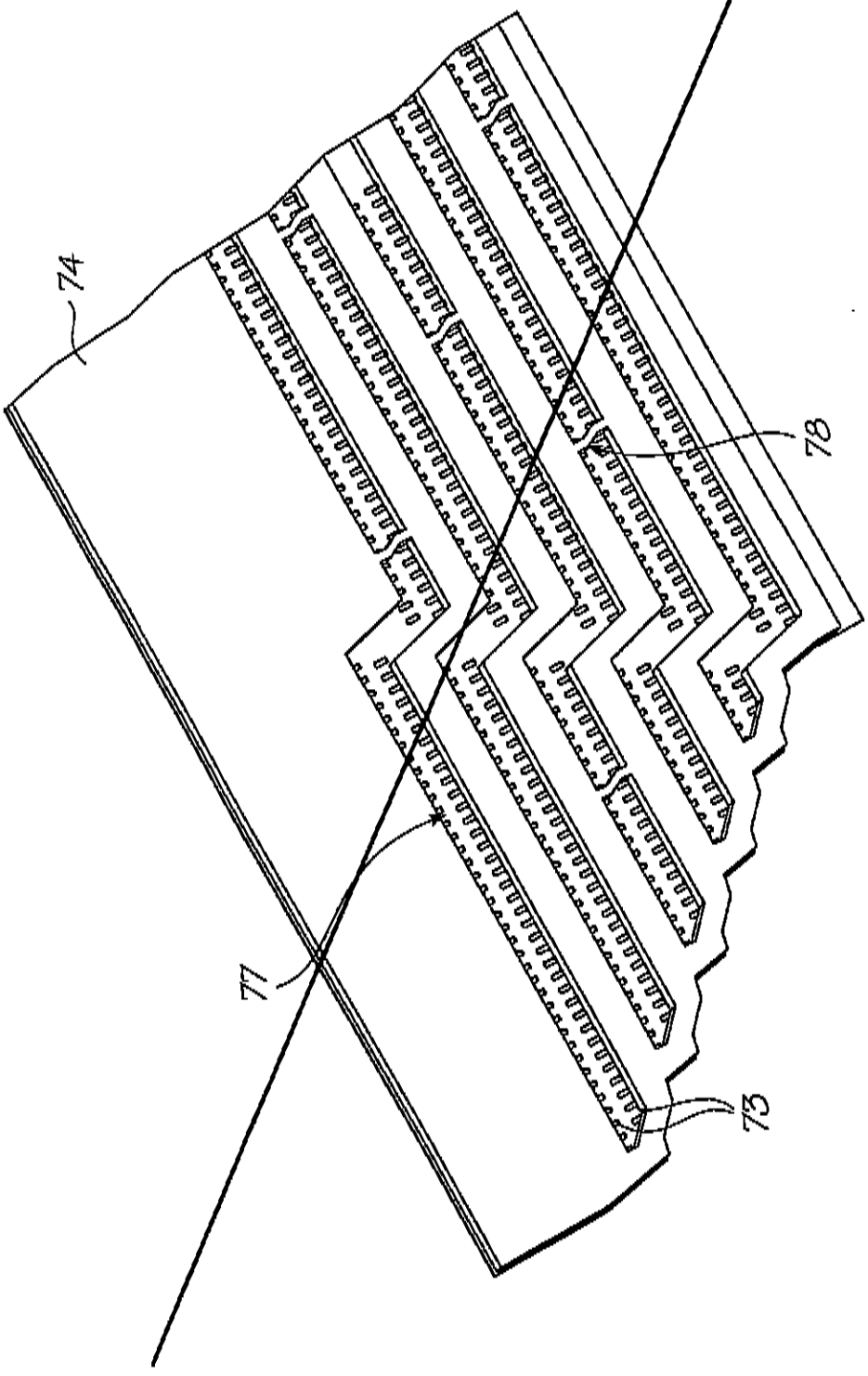


FIG. 38

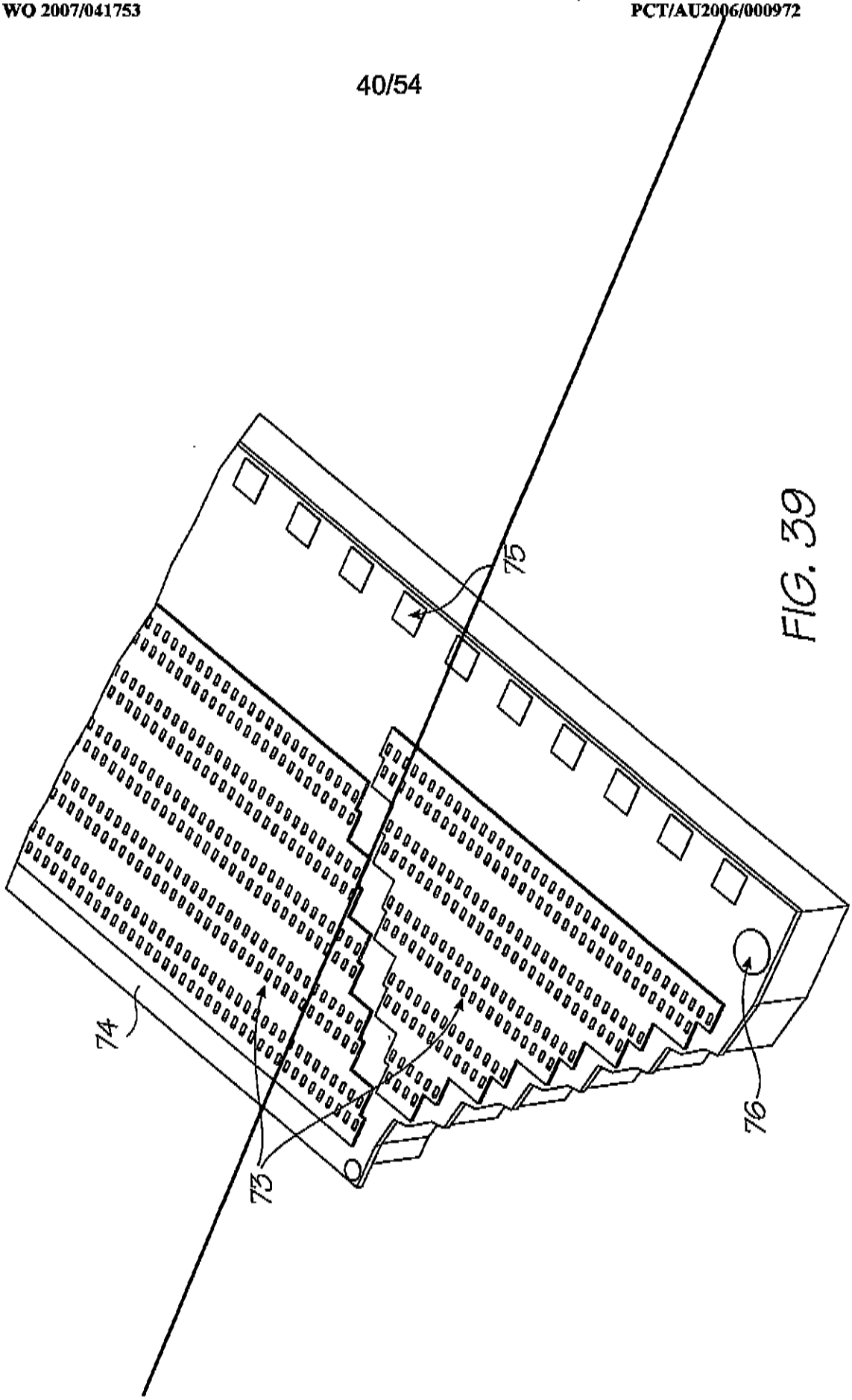


FIG. 39

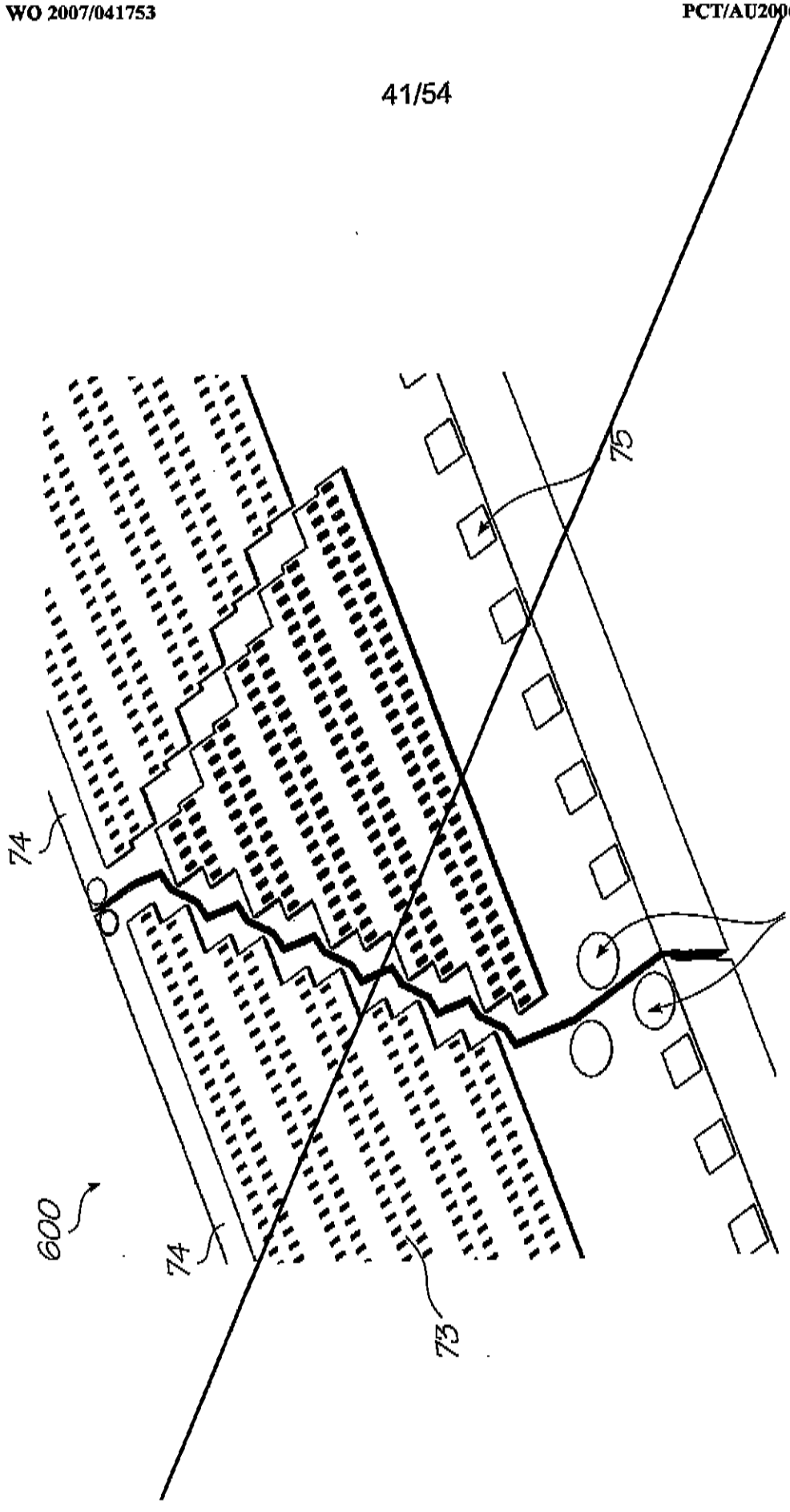


FIG. 40

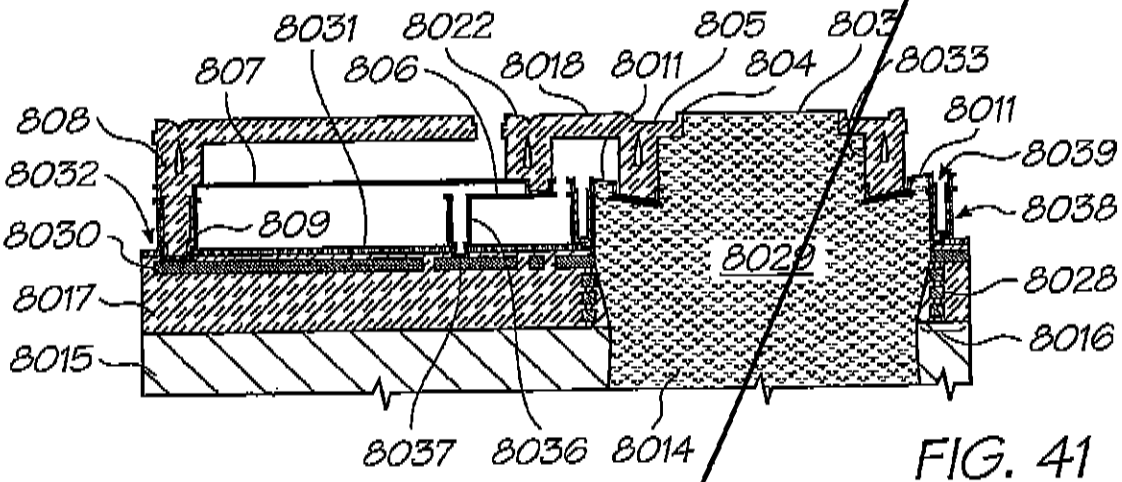


FIG. 41

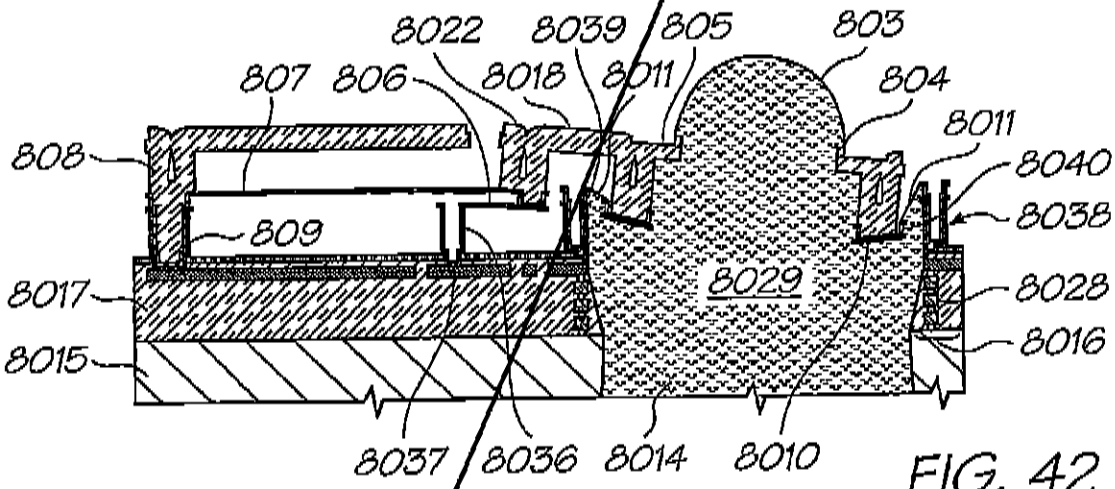


FIG. 42

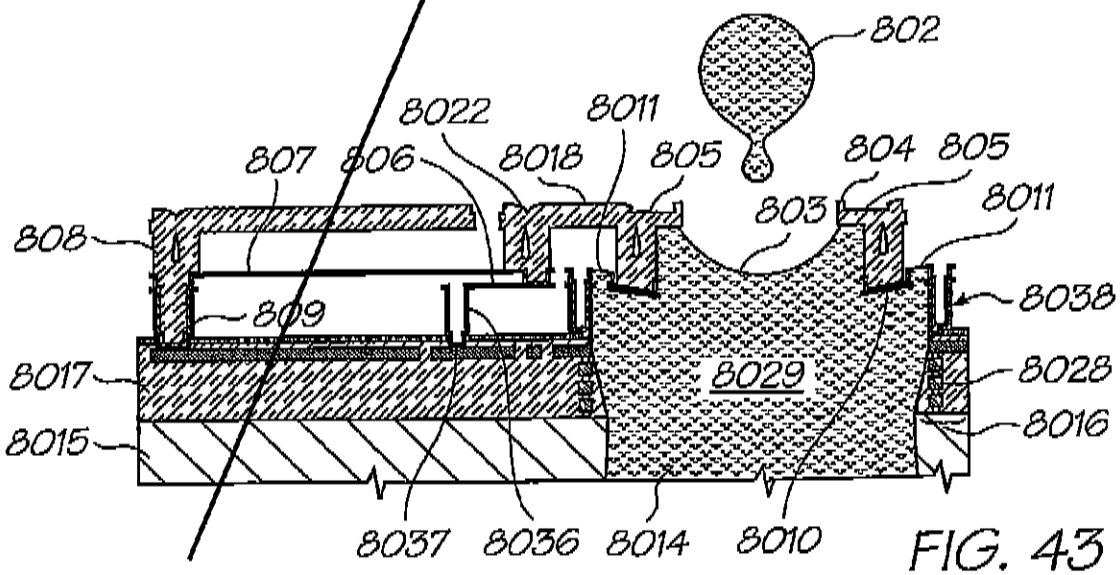


FIG. 43

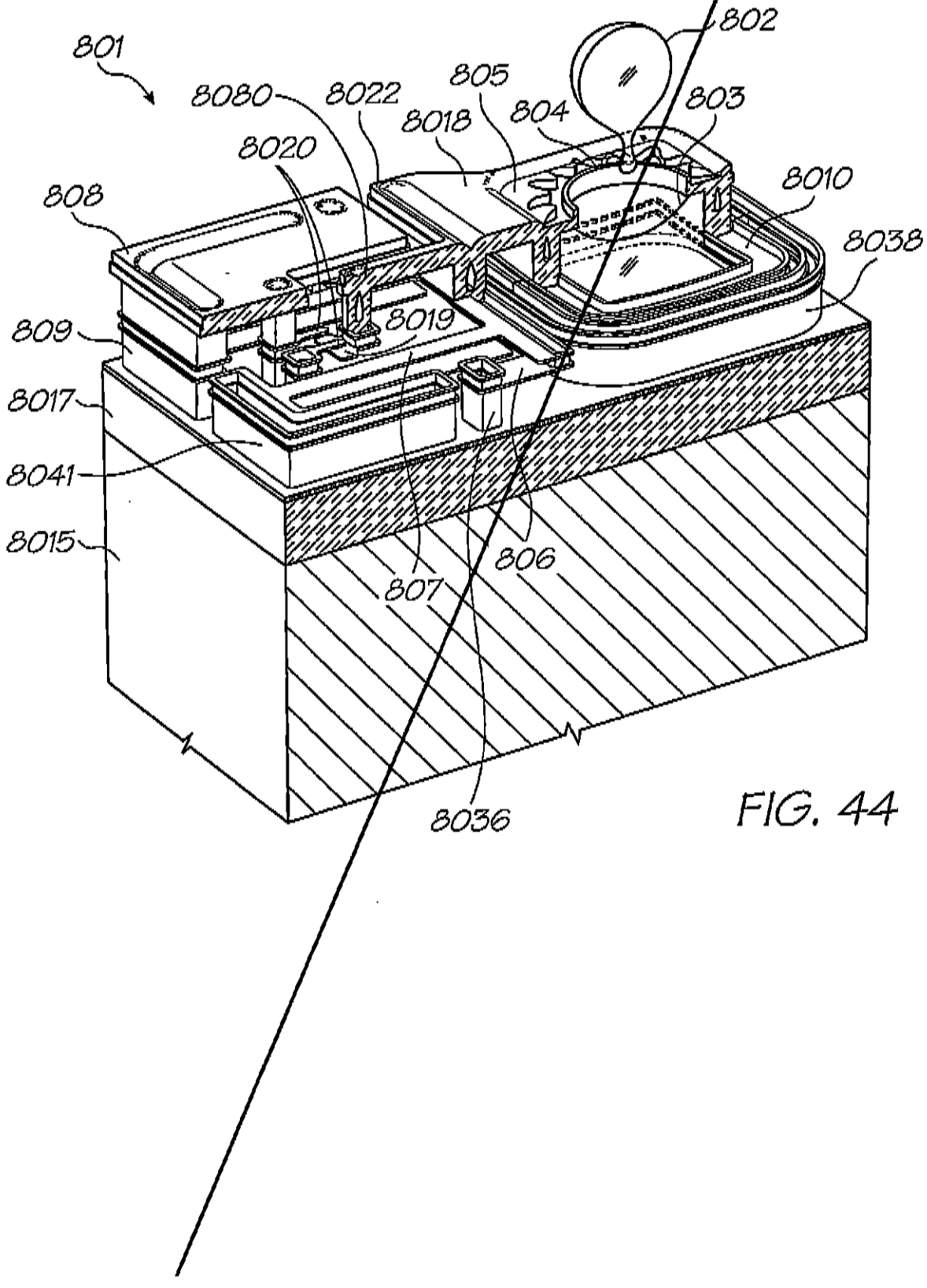

801
802
8080
8022
805
804
803
8018
8020
808
8010
8038
809
8019
8017
8041
8015
807
806
8036

FIG. 44

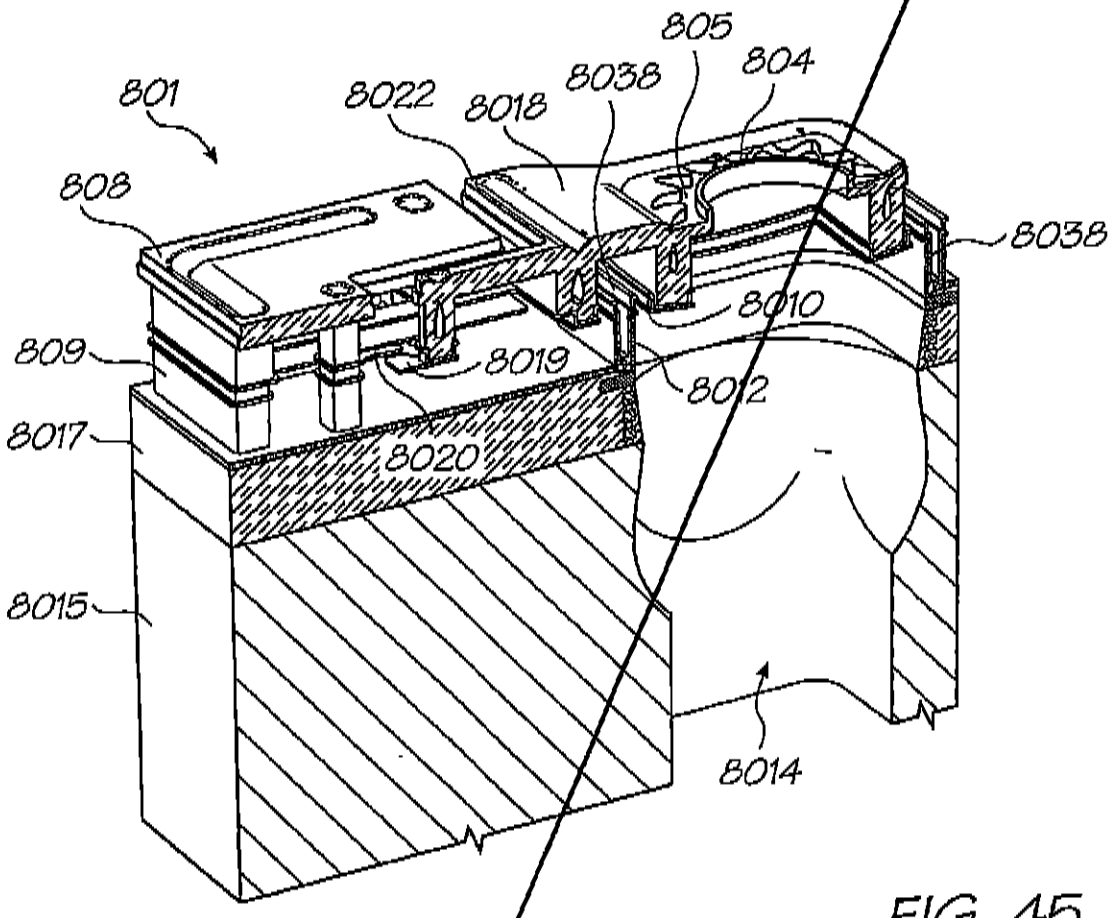

801
8022
8018
8038
805
804
808
8038
8010
809
8019
8012
8017
8020
8015
8014

FIG. 45

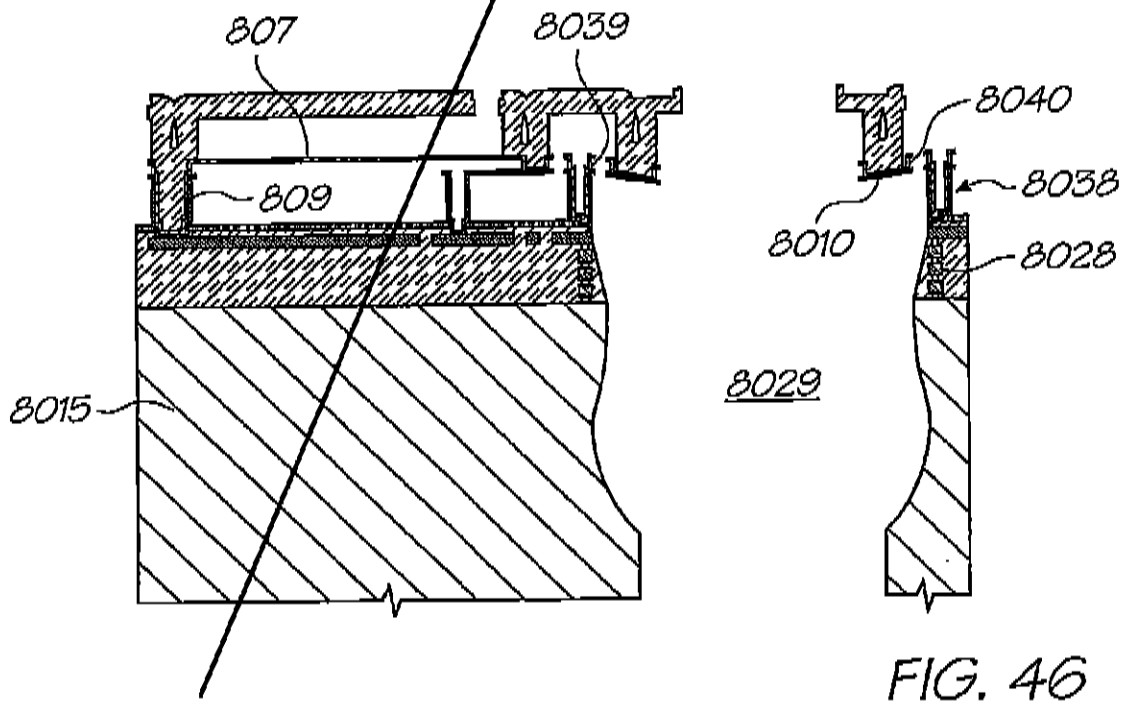

807
8039
809
8015
8040
8038
8010
8028
8029

FIG. 46

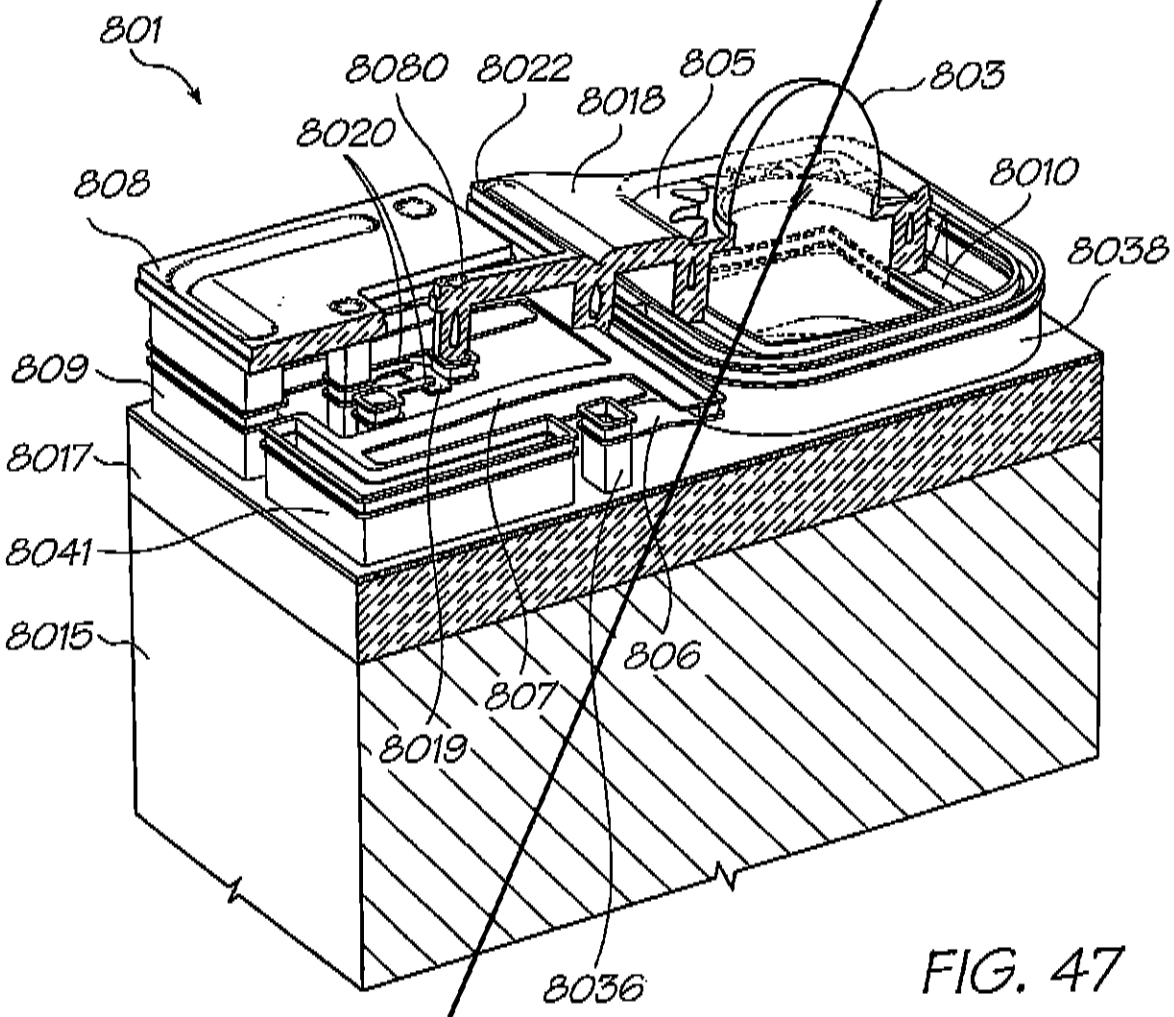

801
8080
8022
805
803
8020
8018
808
8010
8038
809
8017
8041
8015
806
807
8019
8036

FIG. 47

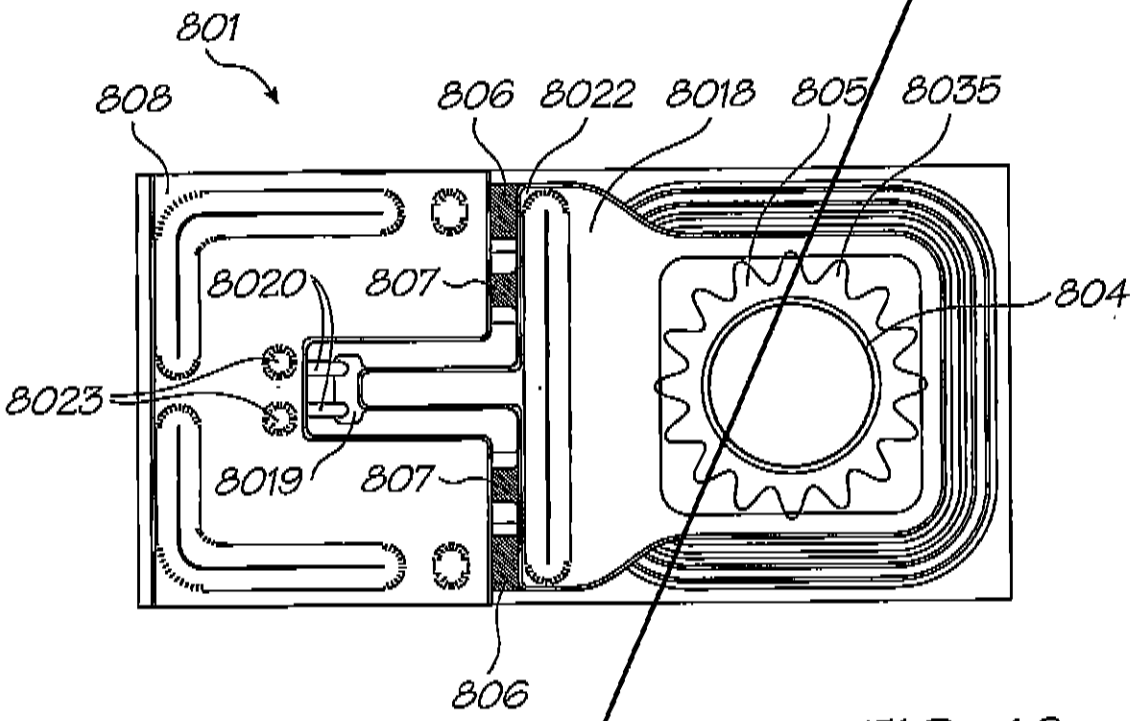

801
808
806
8022
8018
805
8035
804
8020
807
8023
8019
807
806

FIG. 48

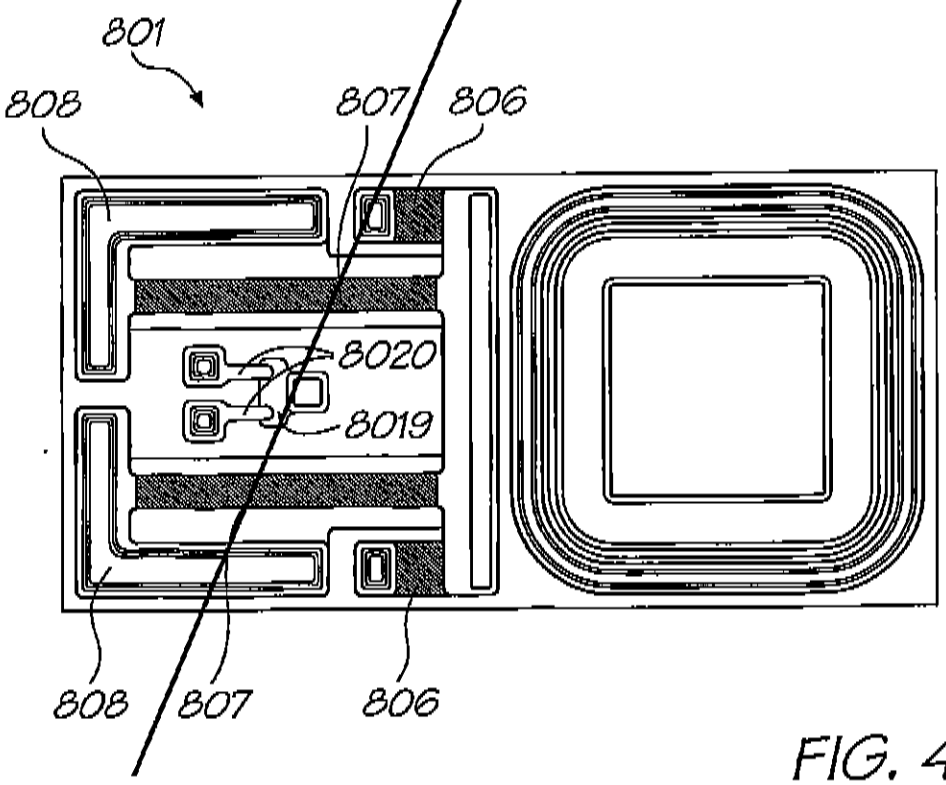

801
808
807
806
8020
8019
808
807
806

FIG. 49

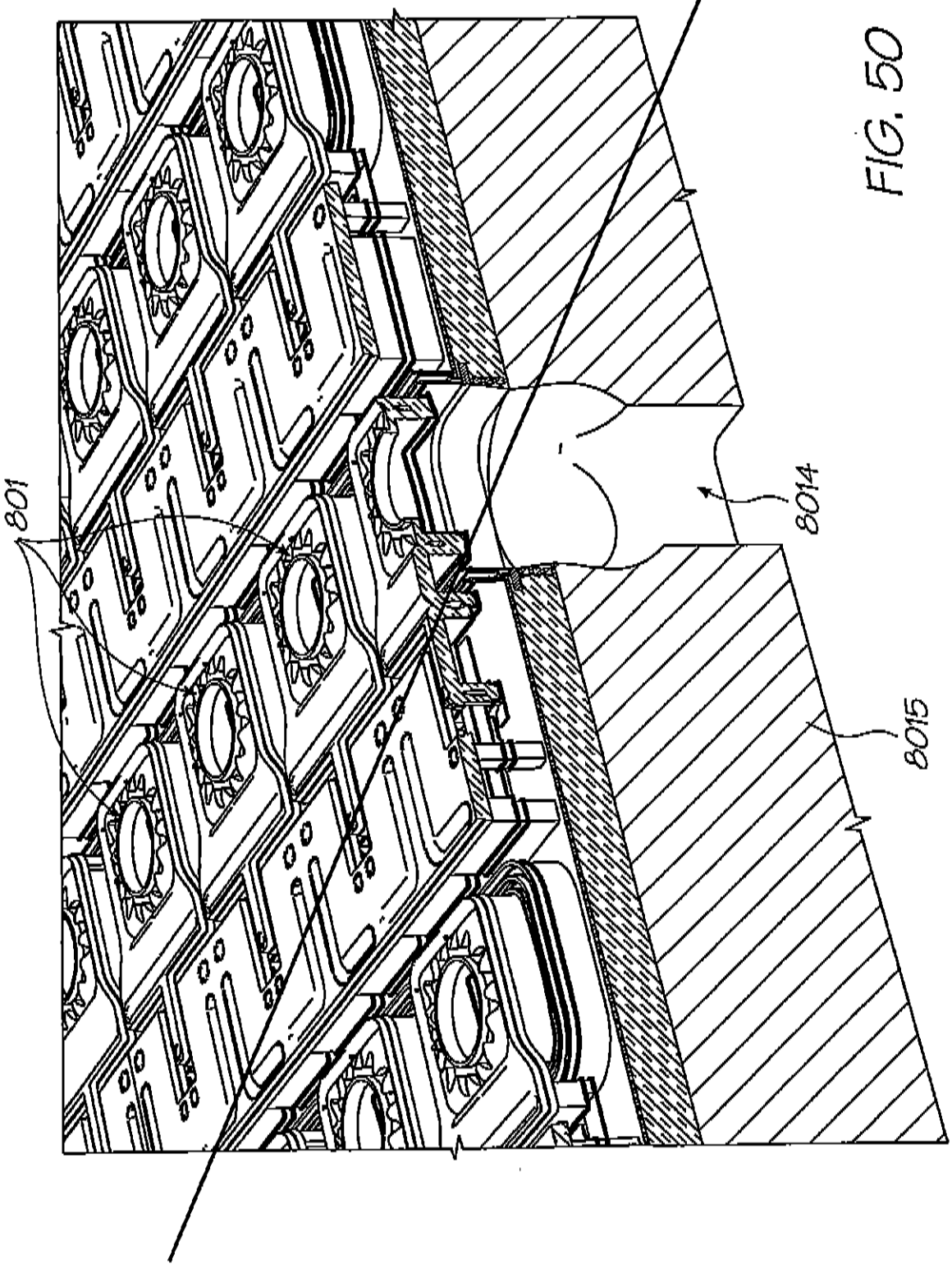


FIG. 50

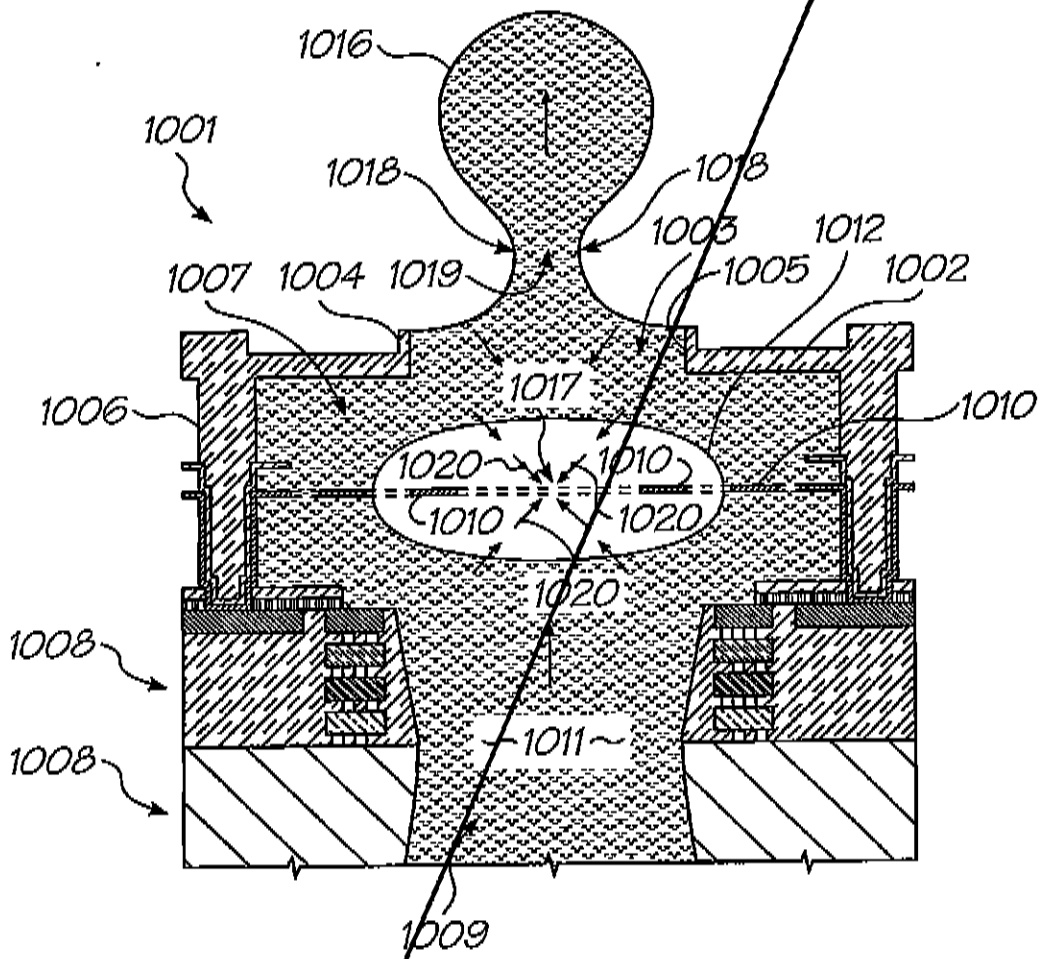

1016
1001
1018
1018
1003
1012
1007
1004
1019
1005
1002
1017
1006
1010
1020
1010
1010
1020
1020
1008
1011
1008
1009

FIG. 51

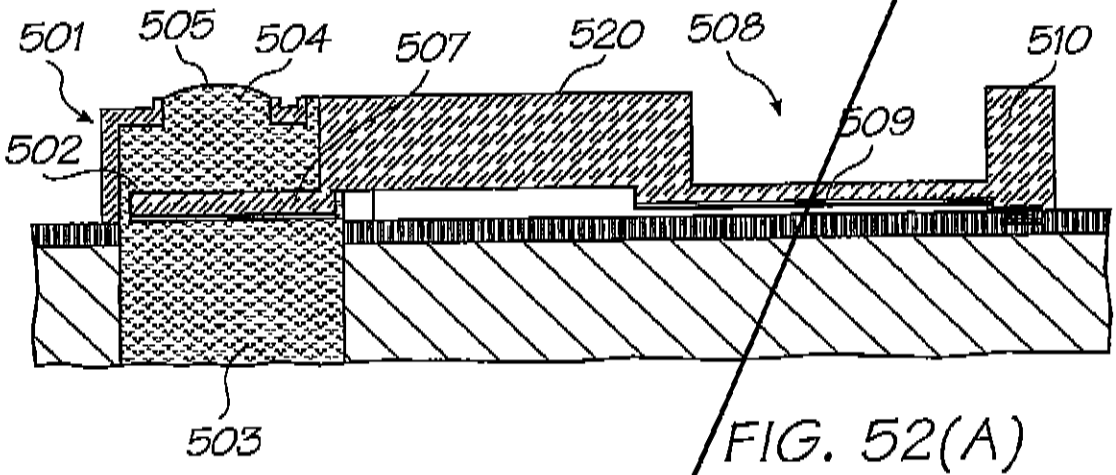


FIG. 52(A)

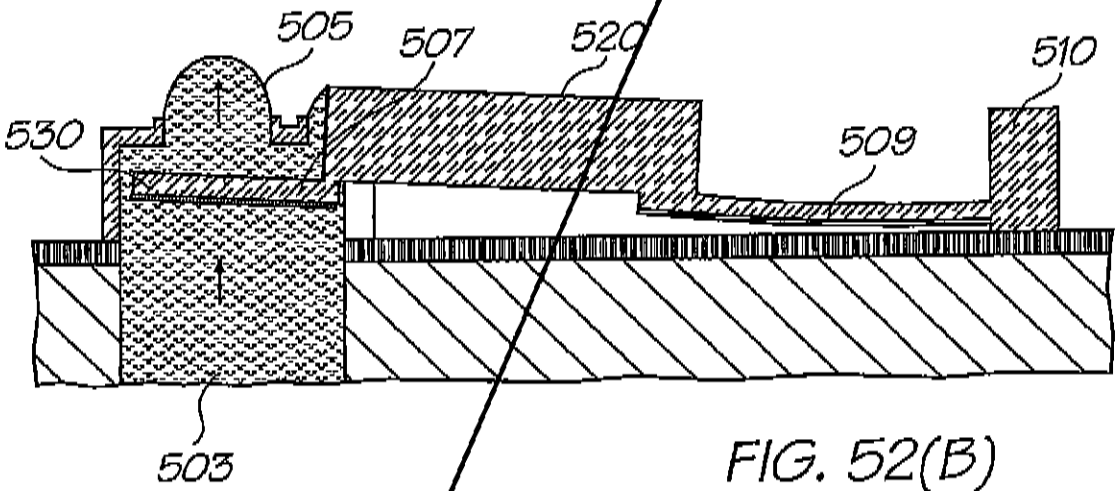


FIG. 52(B)

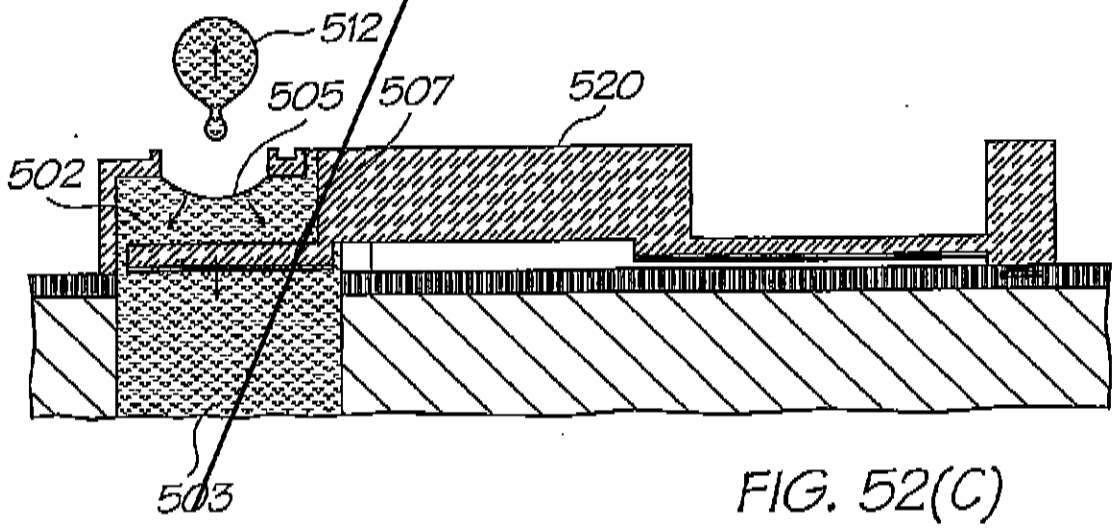


FIG. 52(C)

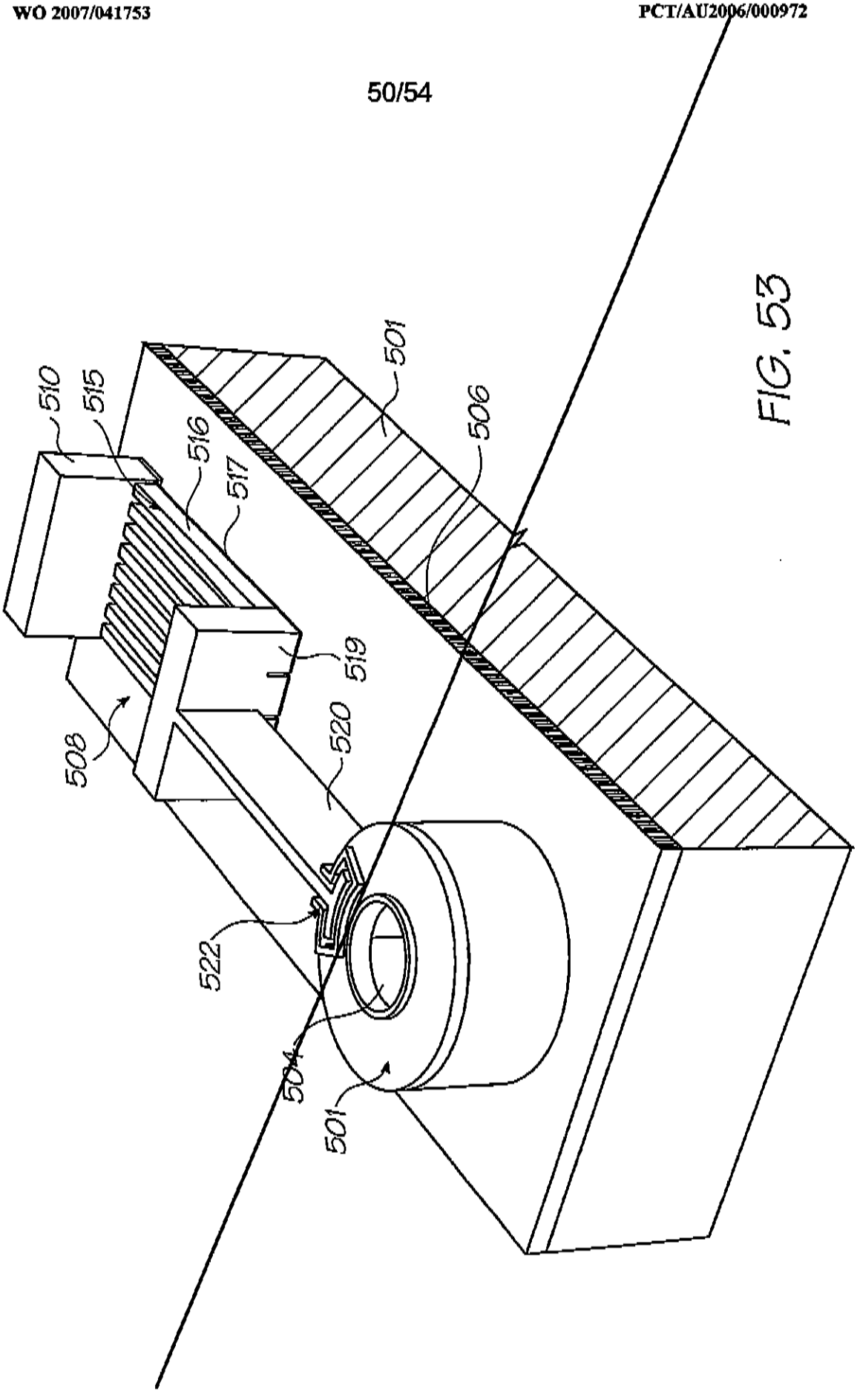


FIG. 53

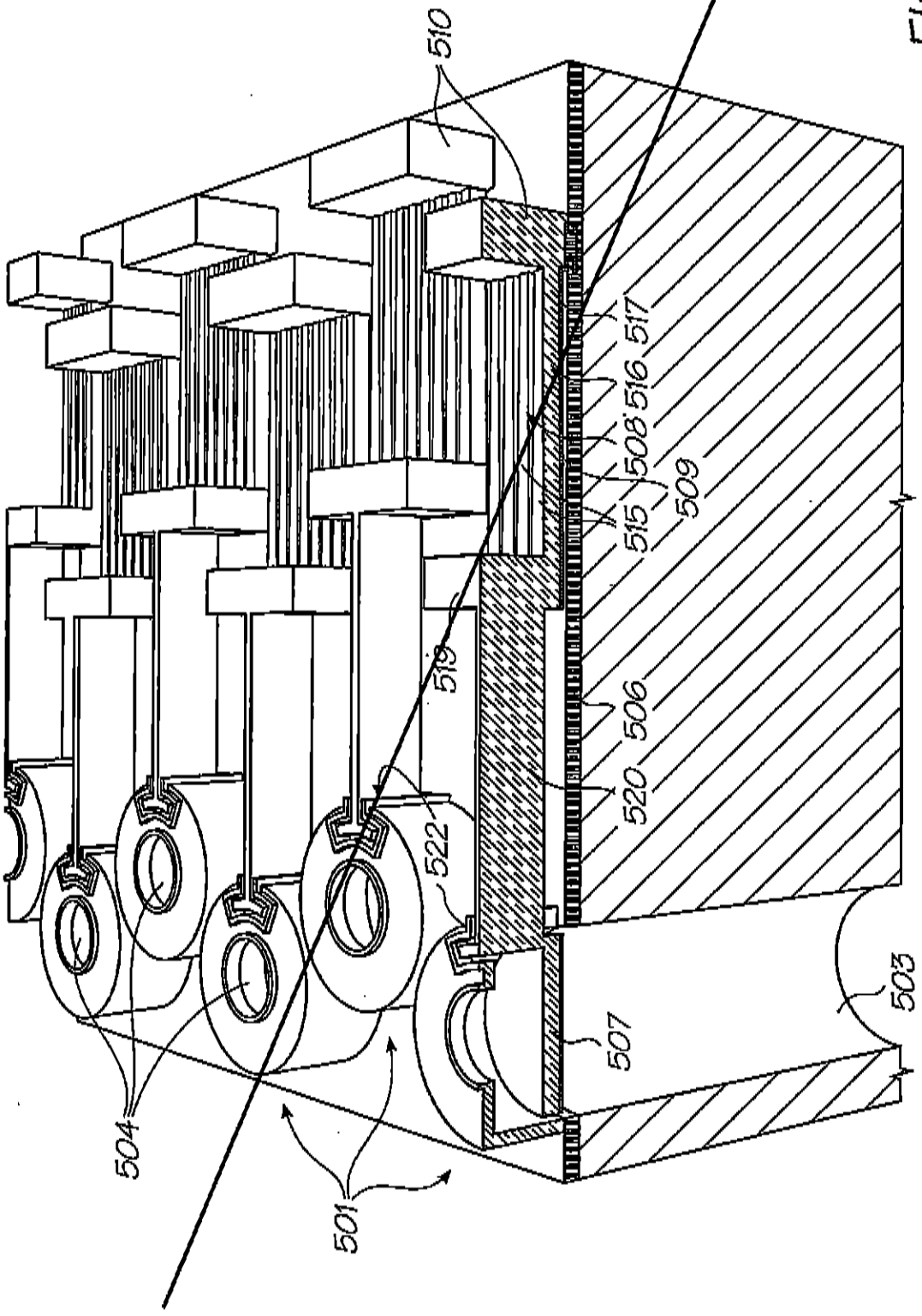


FIG. 54

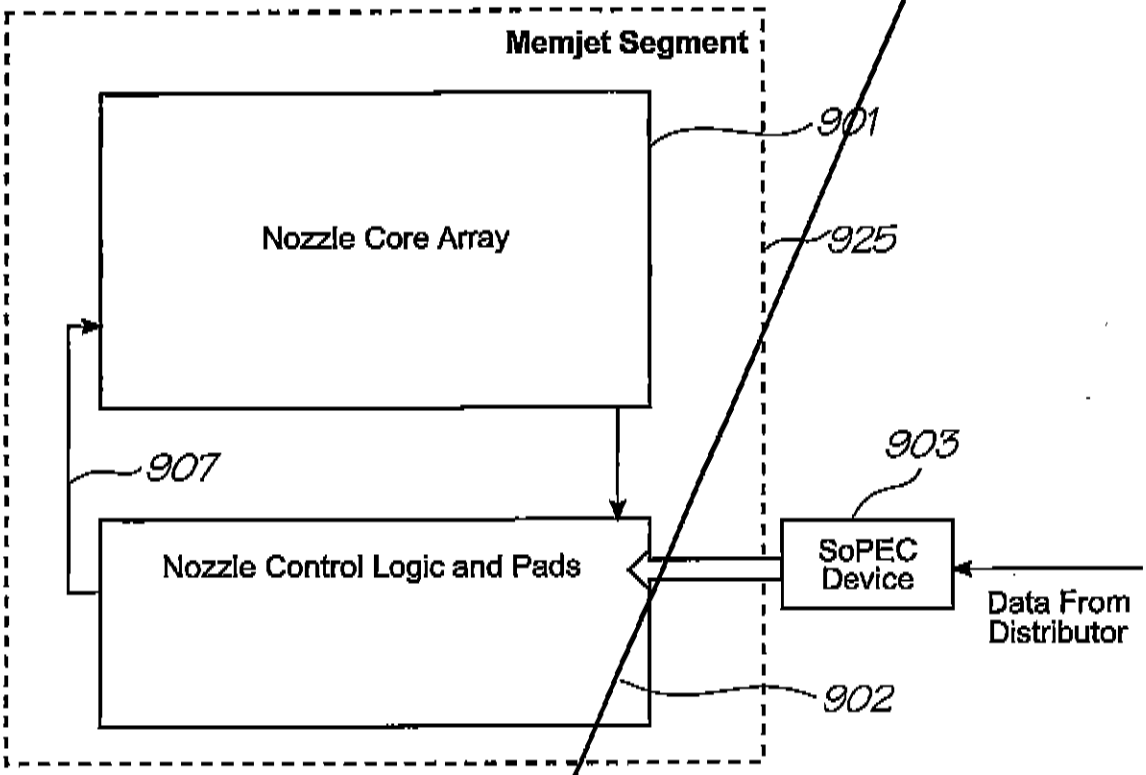

Memjet Segment
Nozzle Core Array
901
925
907
903
Nozzle Control Logic and Pads
SoPEC Device
Data From Distributor
902

FIG. 55

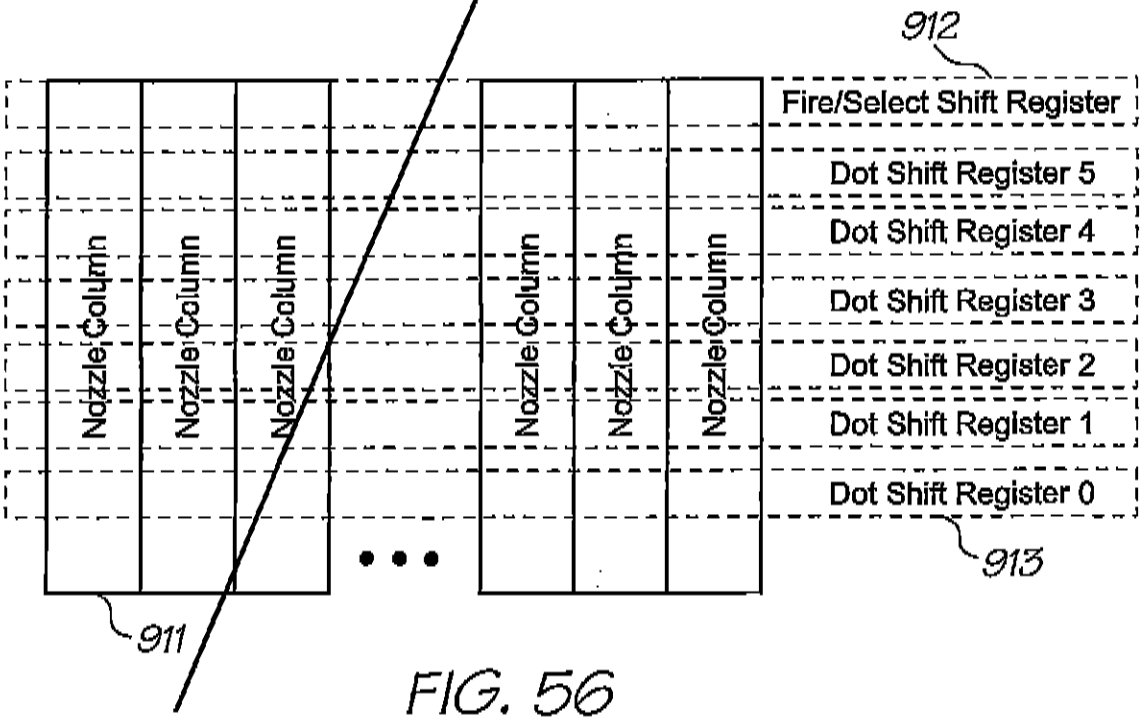

912
Fire/Select Shift Register
Dot Shift Register 5
Dot Shift Register 4
Dot Shift Register 3
Dot Shift Register 2
Dot Shift Register 1
Dot Shift Register 0
Nozzle Column
913
911

FIG. 56

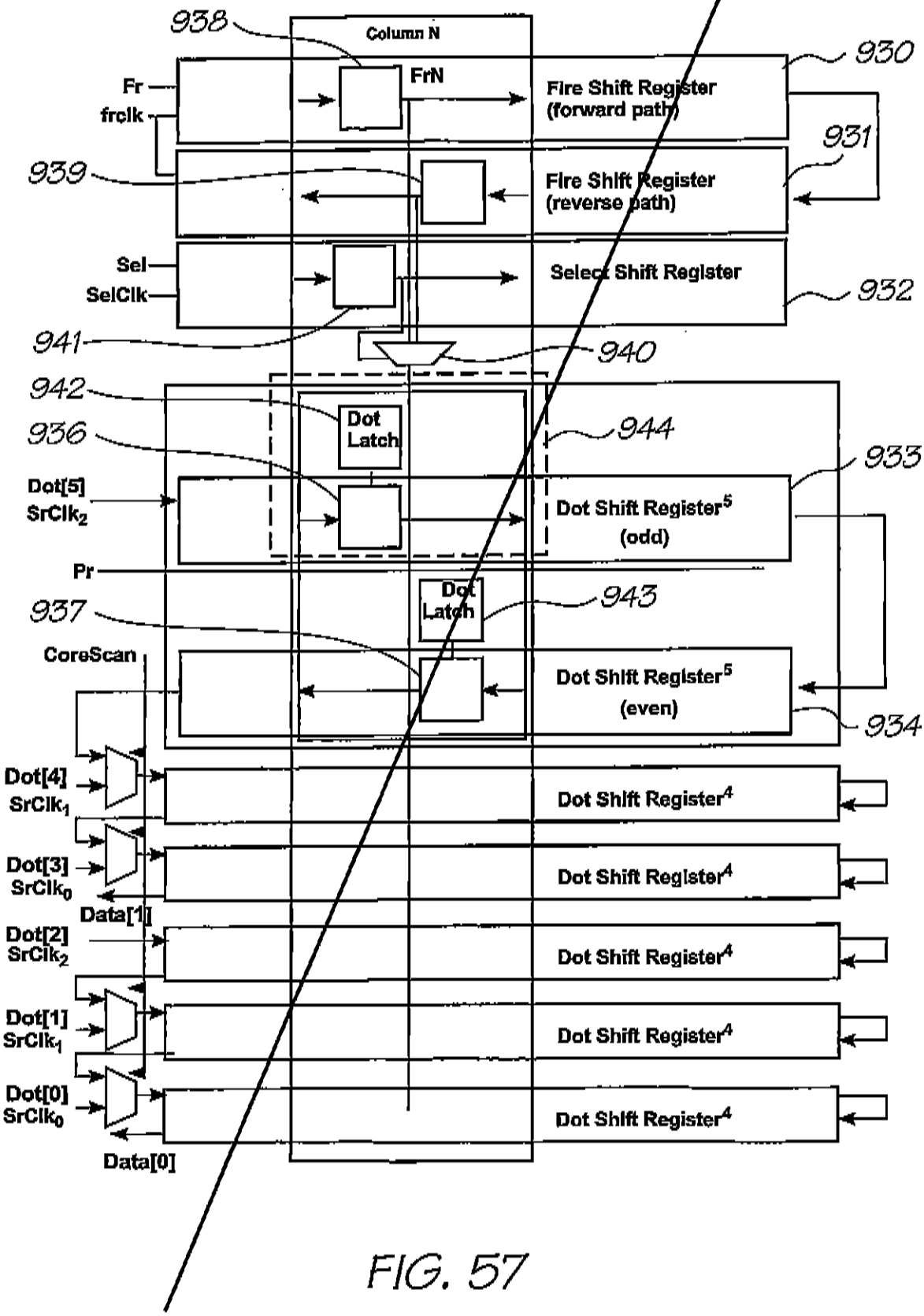

938
Column N
930
Fr
frclk
FrN
Fire Shift Register (forward path)
931
939
Fire Shift Register (reverse path)
Sel
SelClk
Select Shift Register
932
941
940
942
Dot Latch
936
944
933
Dot[5]
SrClk2
Dot Shift Register5 (odd)
Pr
Dot Latch
943
937
CoreScan
Dot Shift Register5 (even)
934
Dot[4]
SrClk1
Dot Shift Register4
Dot[3]
SrClk0
Dot Shift Register4
Data[1]
Dot[2]
SrClk2
Dot Shift Register4
Dot[1]
SrClk1
Dot Shift Register4
Dot[0]
SrClk0
Dot Shift Register4
Data[0]

FIG. 57

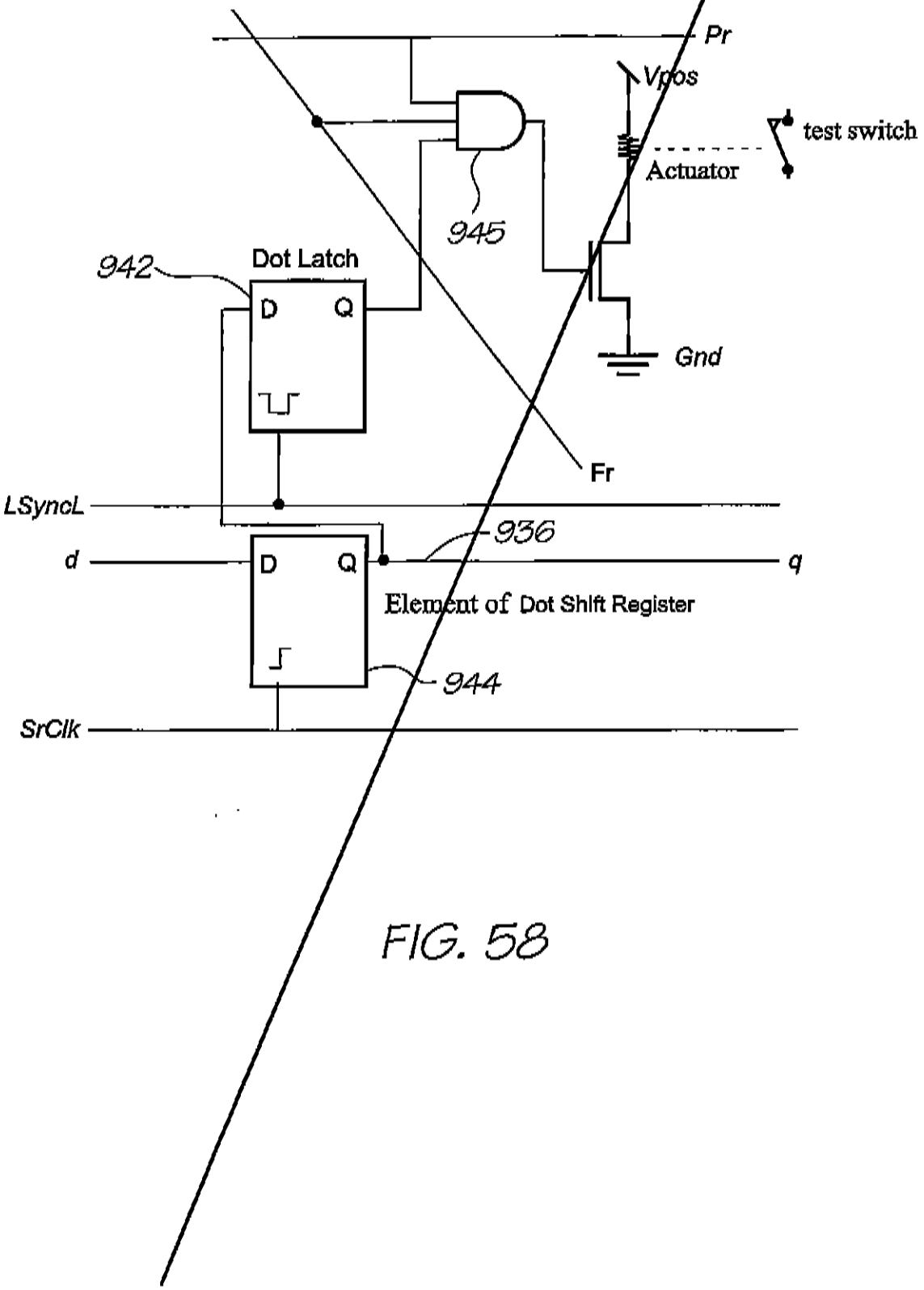

Pr
Vpos
test switch
Actuator
945
942
Dot Latch
D
Q
Gnd
Fr
LSyncL
936
d
D
Q
q
Element of Dot Shift Register
944
SrClk

FIG. 58

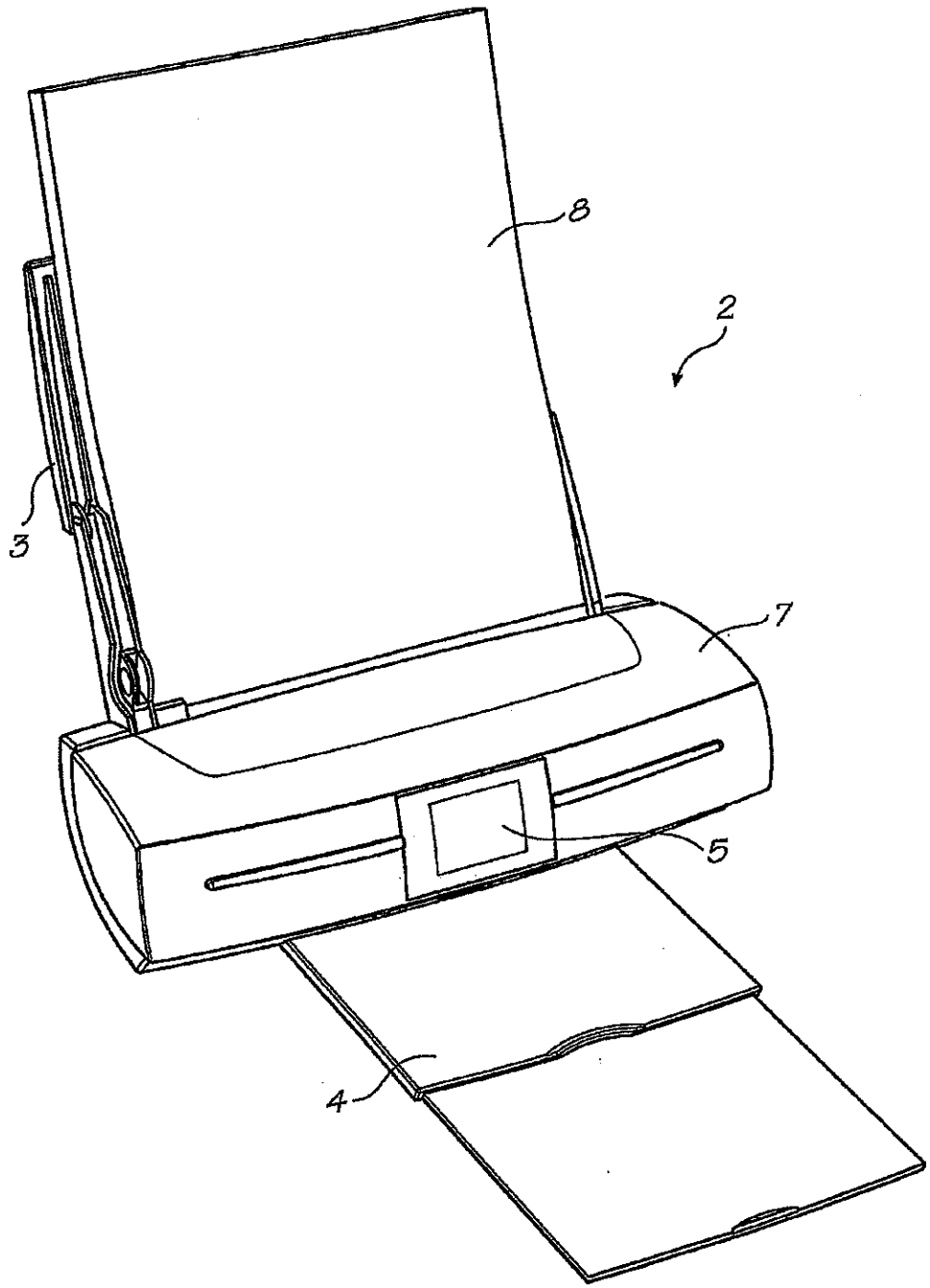


FIG. 1

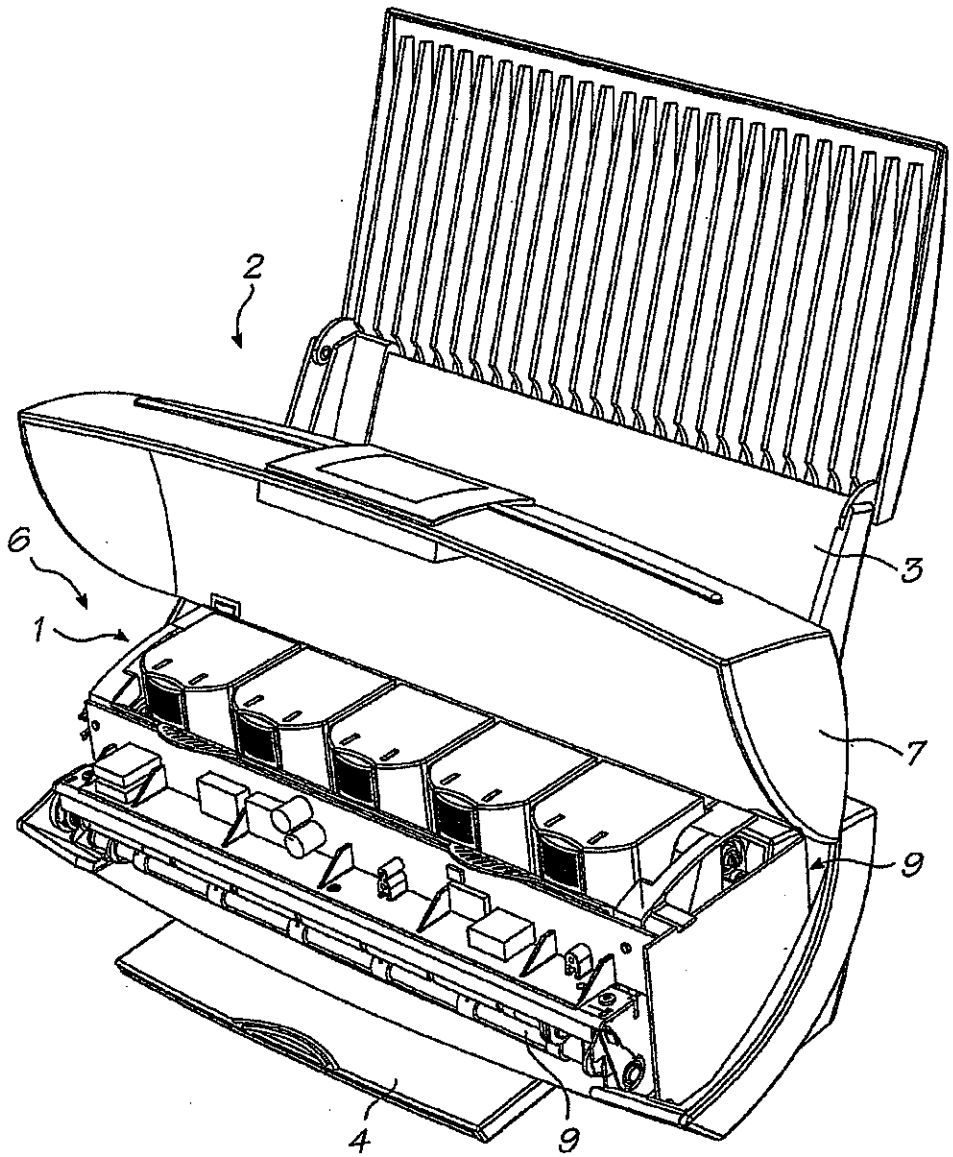


FIG. 2

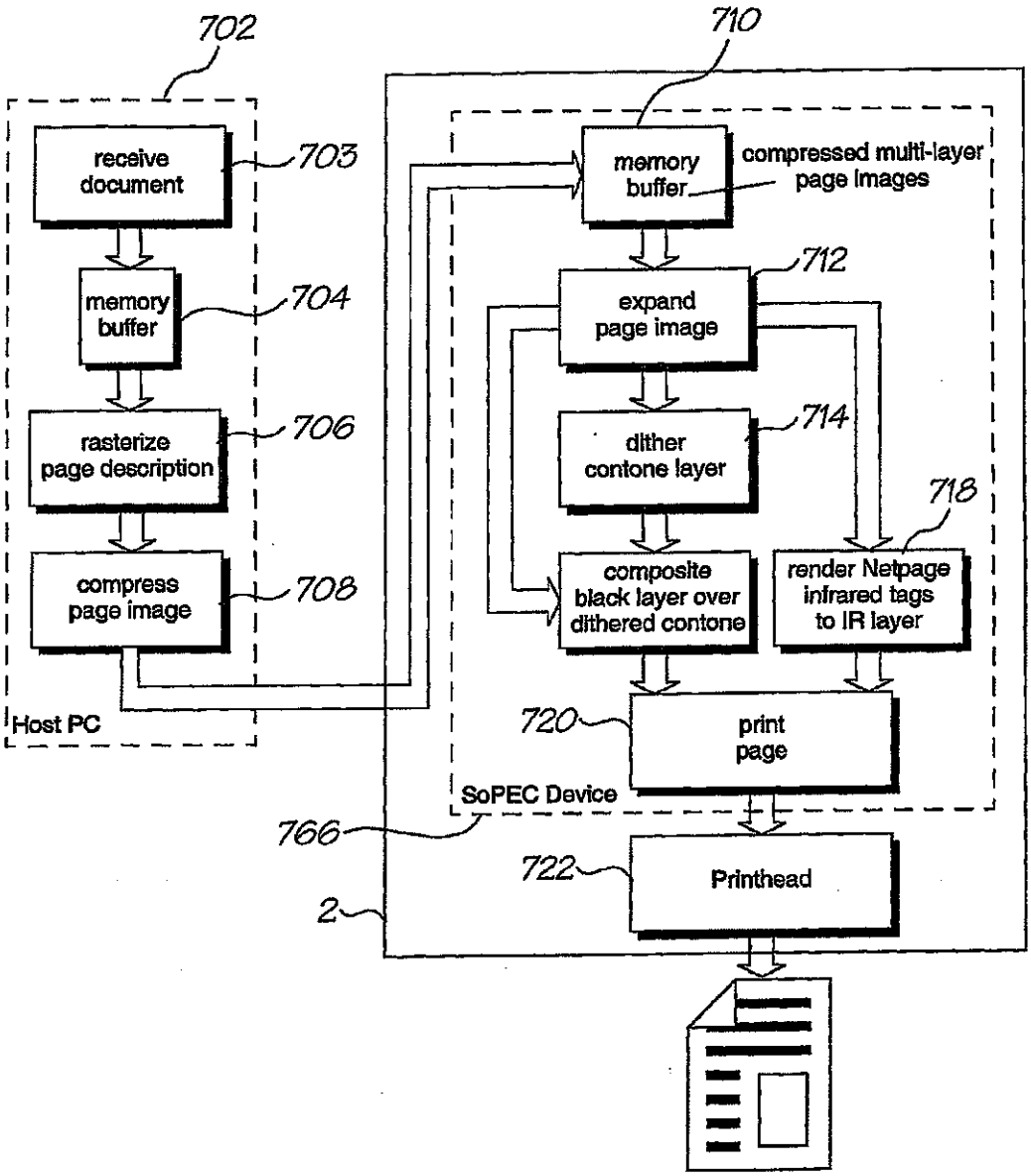

702
710
receive document
703
memory buffer
704
rasterize page description
706
compress page image
708
Host PC
memory buffer
compressed multi-layer page images
712
expand page image
714
dither contone layer
718
composite black layer over dithered contone
render Netpage infrared tags to IR layer
720
print page
SoPEC Device
766
722
Printhead
2

FIG. 3

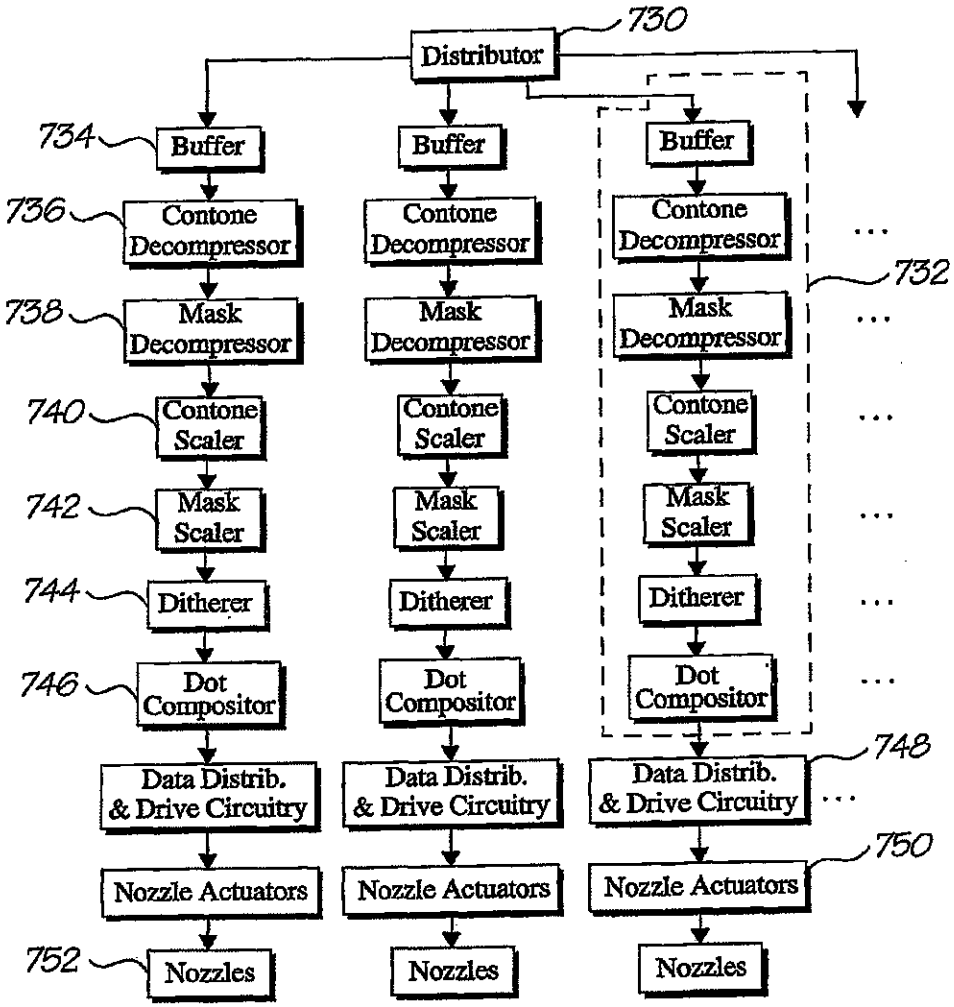

730
Distributor
734
Buffer
736
Contone Decompressor
738
Mask Decompressor
740
Contone Scaler
742
Mask Scaler
744
Ditherer
746
Dot Compositor
Data Distrib. & Drive Circuitry
Nozzle Actuators
752
Nozzles
732
748
750

FIG. 4

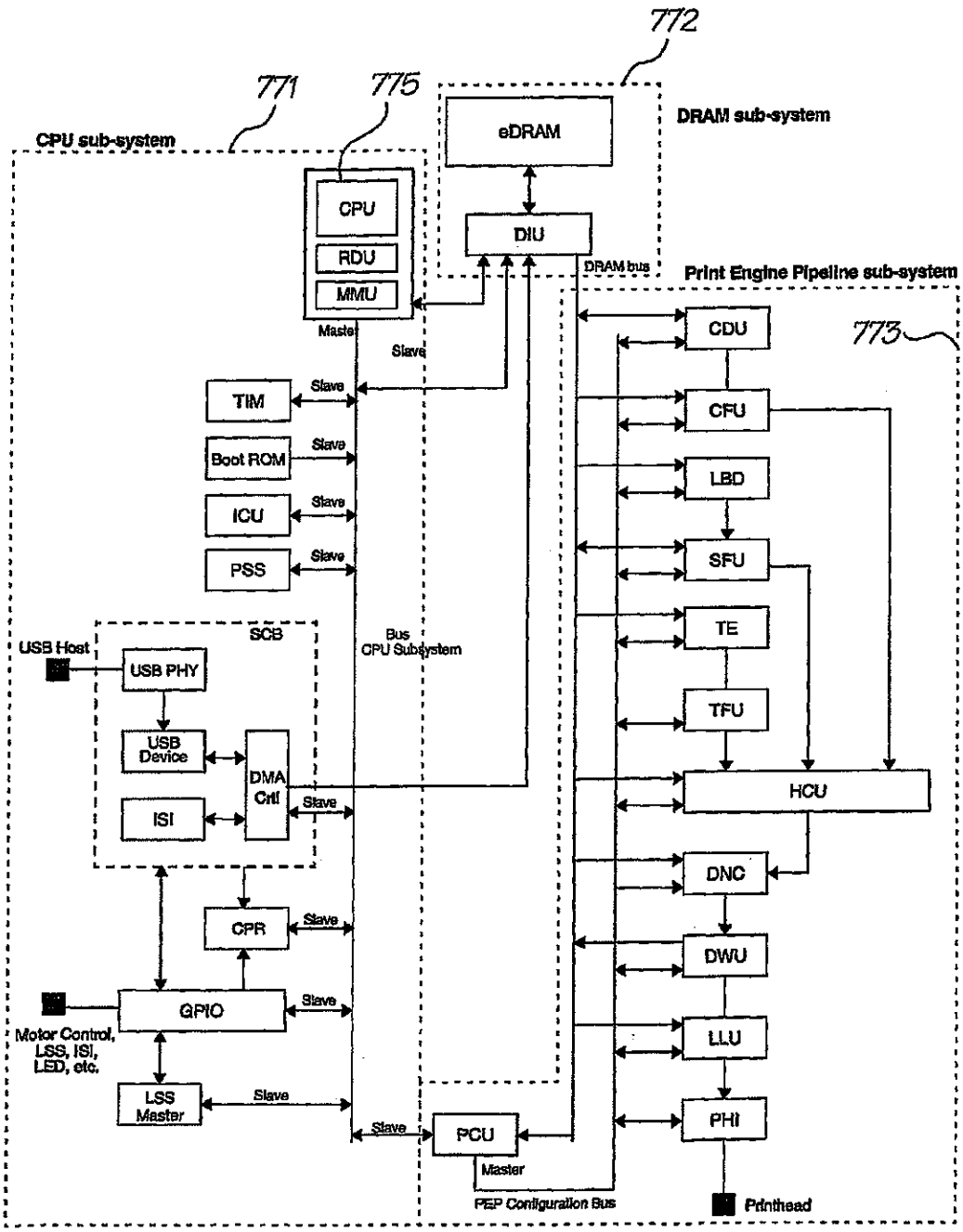

772
771
775
CPU sub-system
DRAM sub-system
eDRAM
CPU
RDU
MMU
DIU
DRAM bus
Print Engine Pipeline sub-system
Master
Slave
773
CDU
TIM
CFU
Boot ROM
LBD
ICU
SFU
PSS
TE
SCB
Bus
CPU Subsystem
USB Host
USB PHY
TFU
USB
Device
DMA
Ctrl
HCU
ISI
DNC
CPR
DWU
GPIO
LLU
Motor Control,
LSS, ISI,
LED, etc.
LSS
Master
PHI
PCU
Master
PEP Configuration Bus
Printhead

FIG. 5

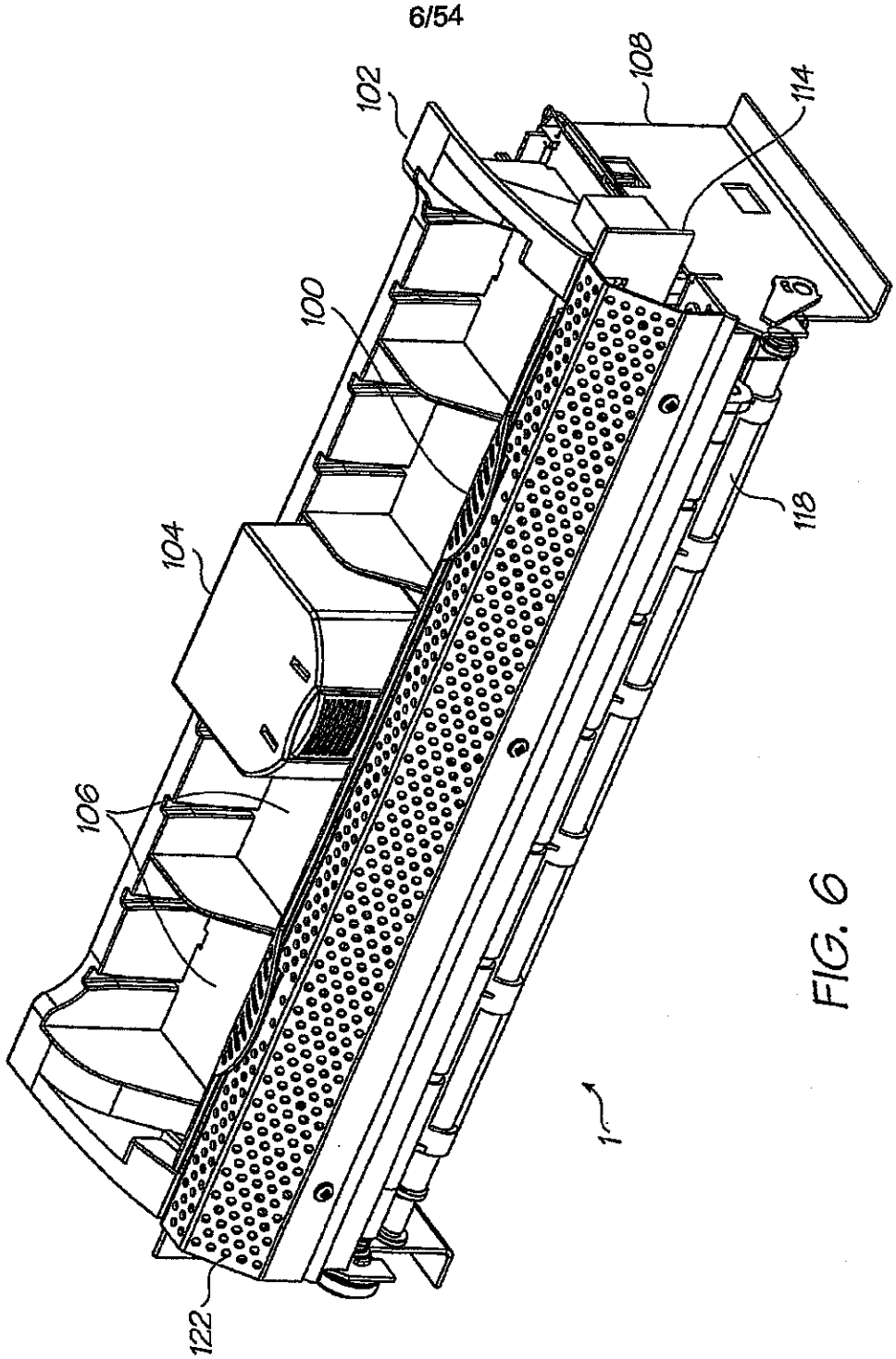


FIG. 6

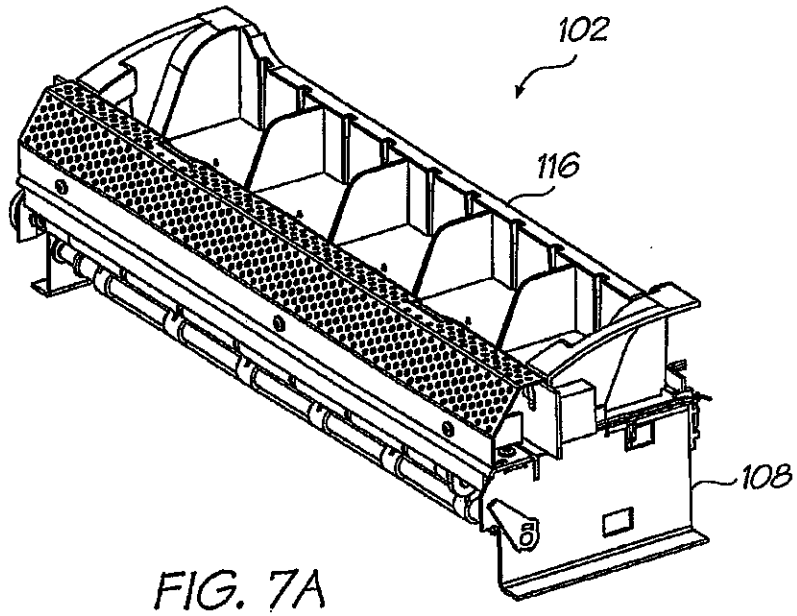


FIG. 7A

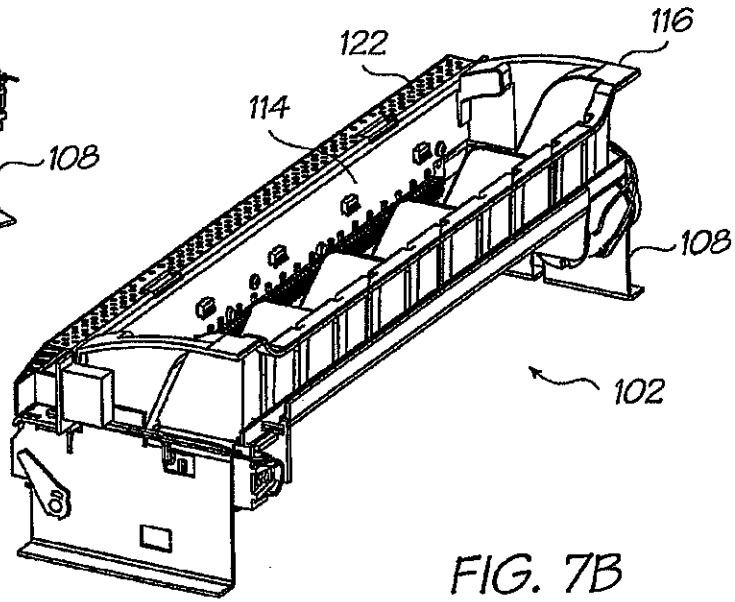


FIG. 7B

7154

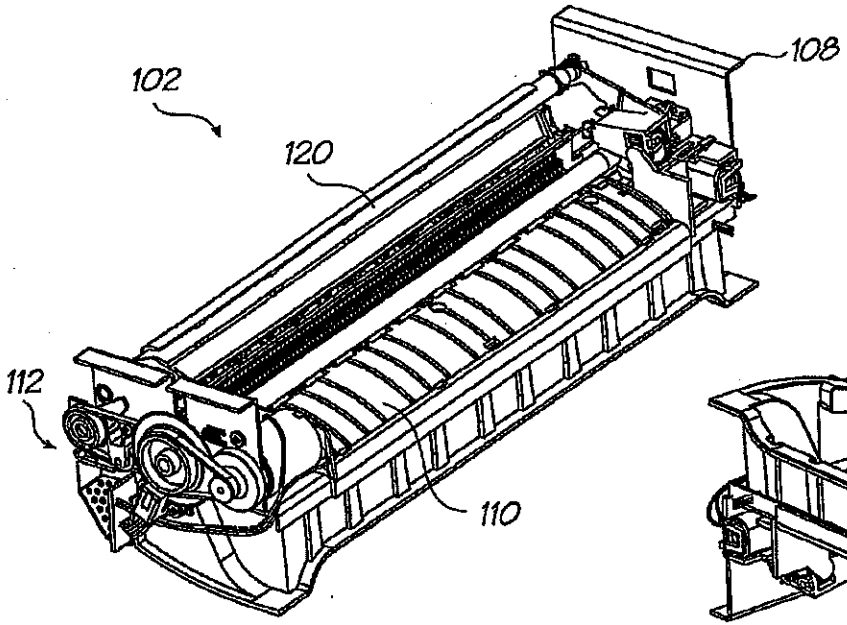


FIG. 7C

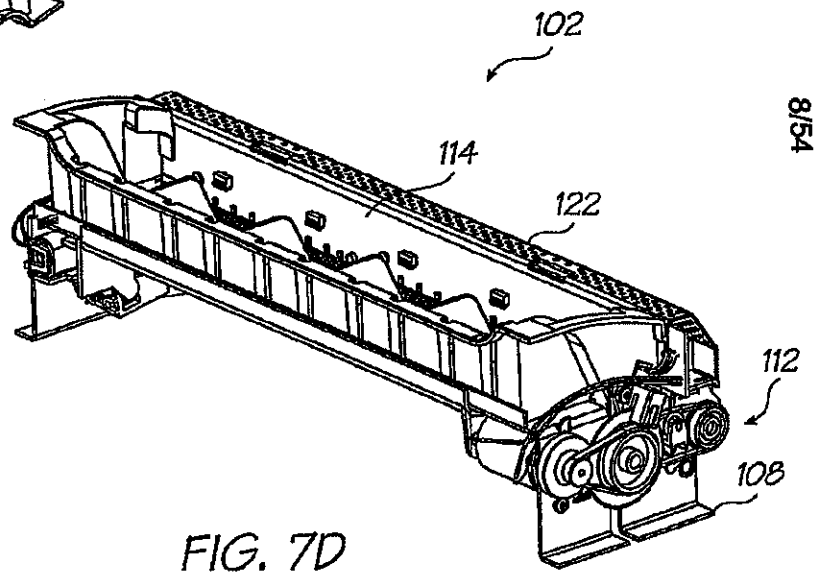


FIG. 7D

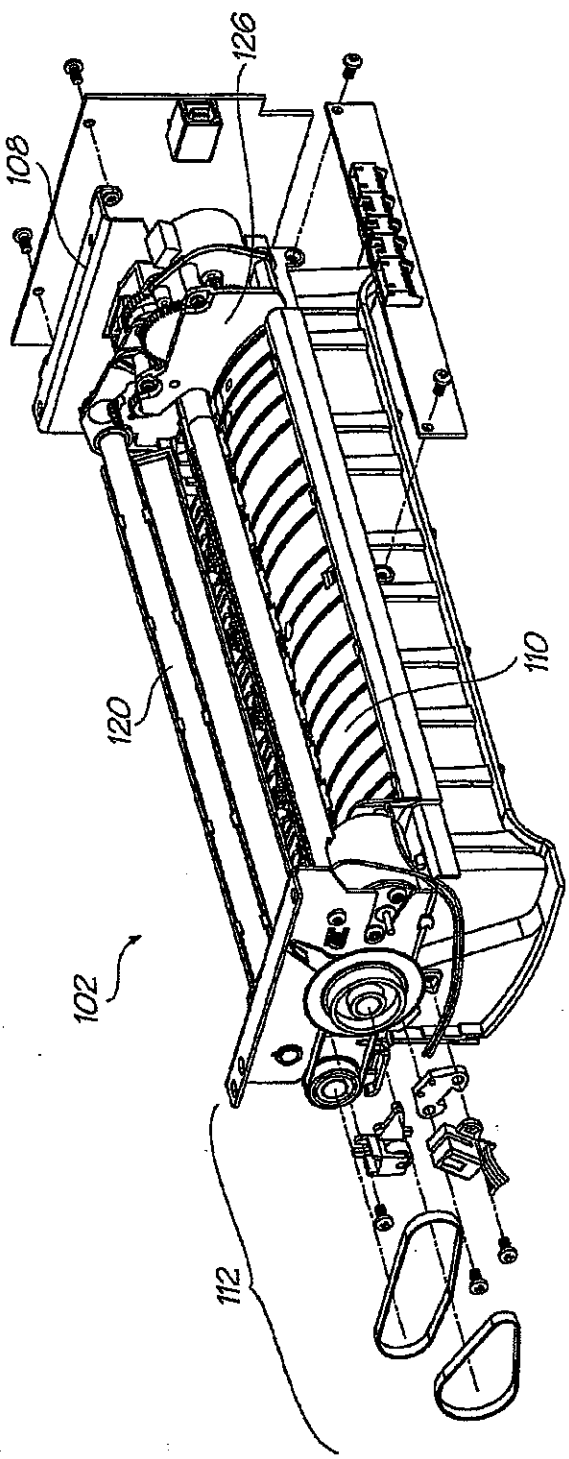


FIG. 8

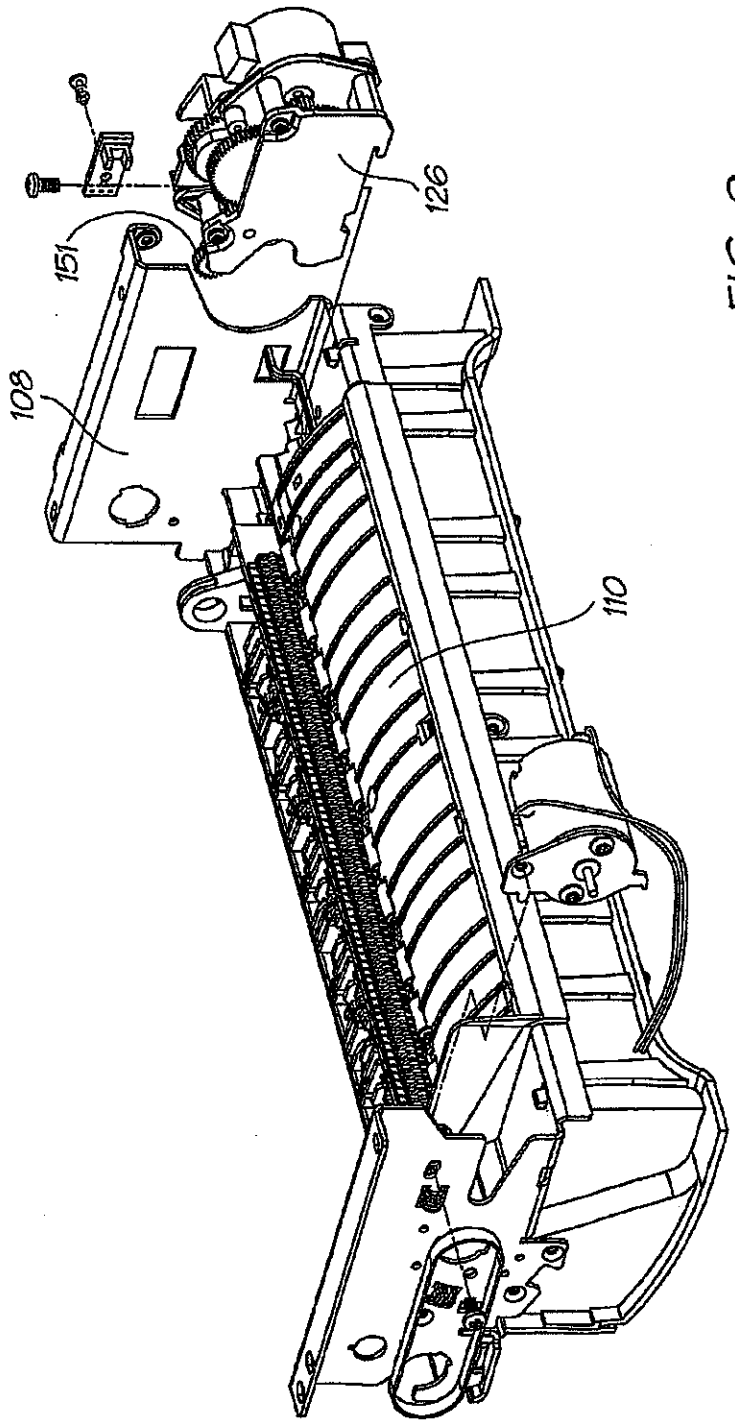


FIG. 9

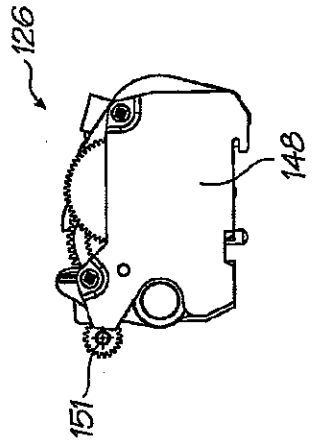


FIG. 10

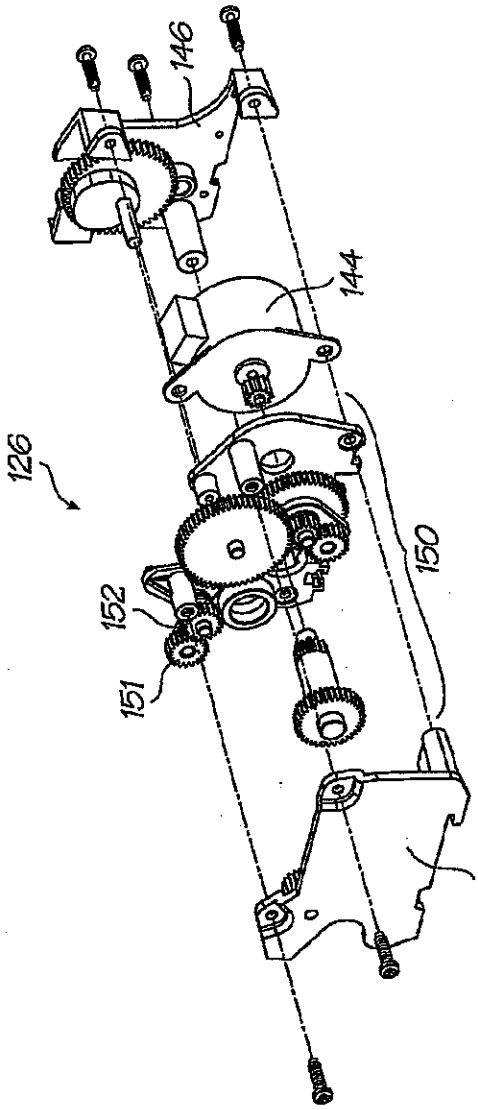


FIG. 11

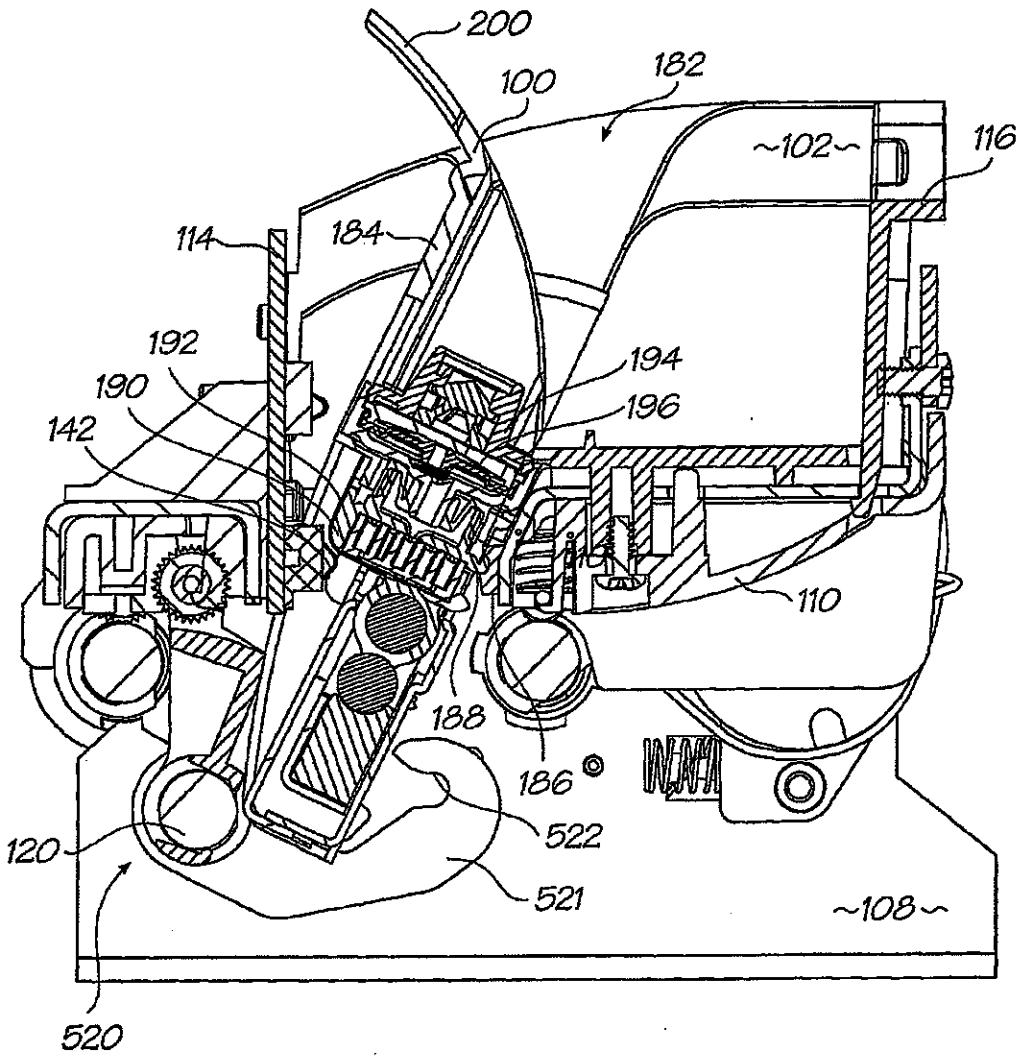

200
100
182
~102~
116
114
184
192
190
142
194
196
110
188
186
120
522
521
~108~
520

FIG. 12

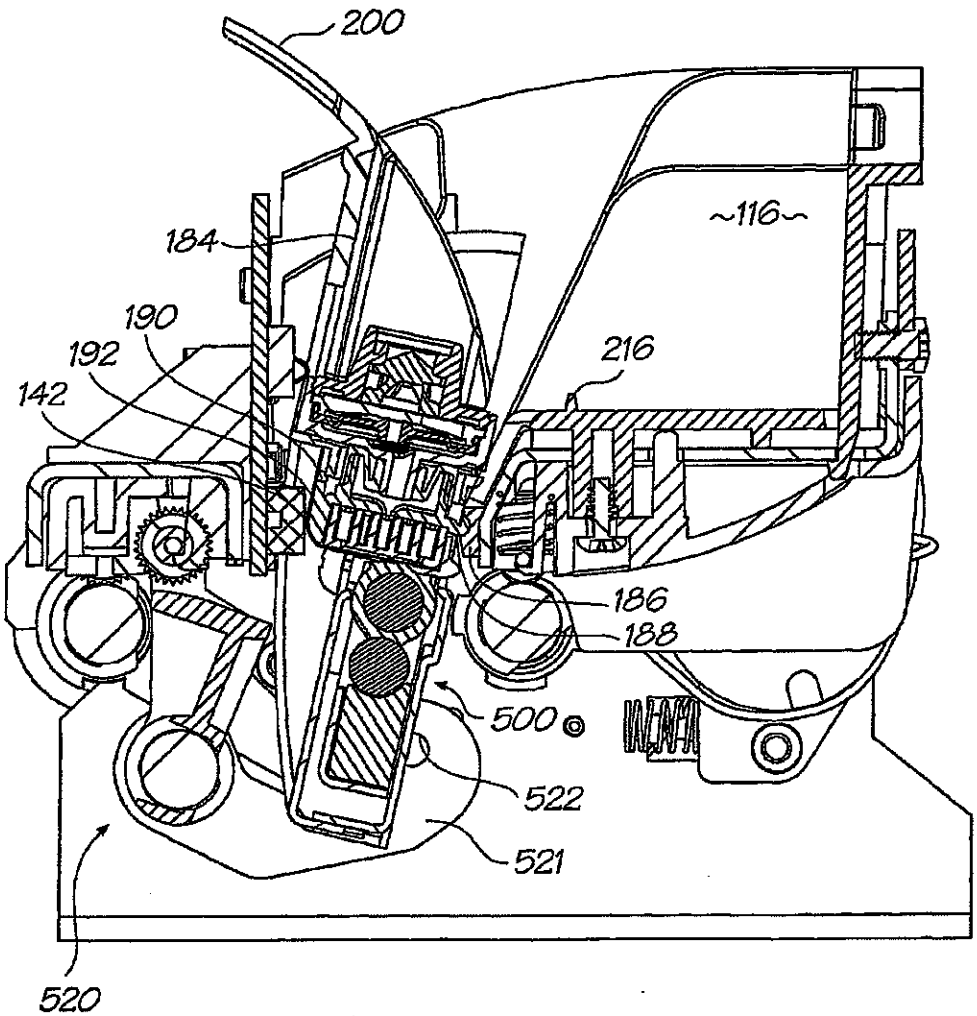


FIG. 13

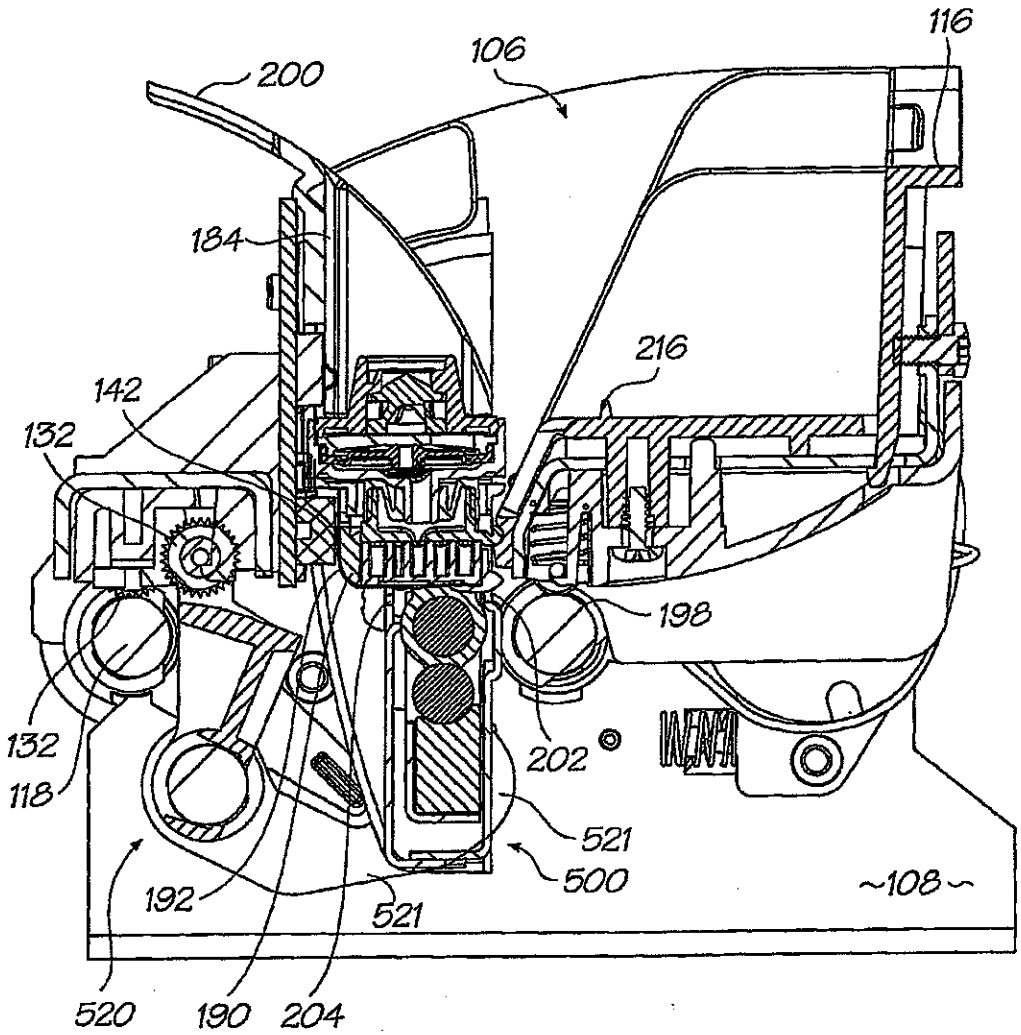

116
106
200
184
216
142
132
198
132
202
118
521
500
192
521
~108~
520
190
204

FIG. 14

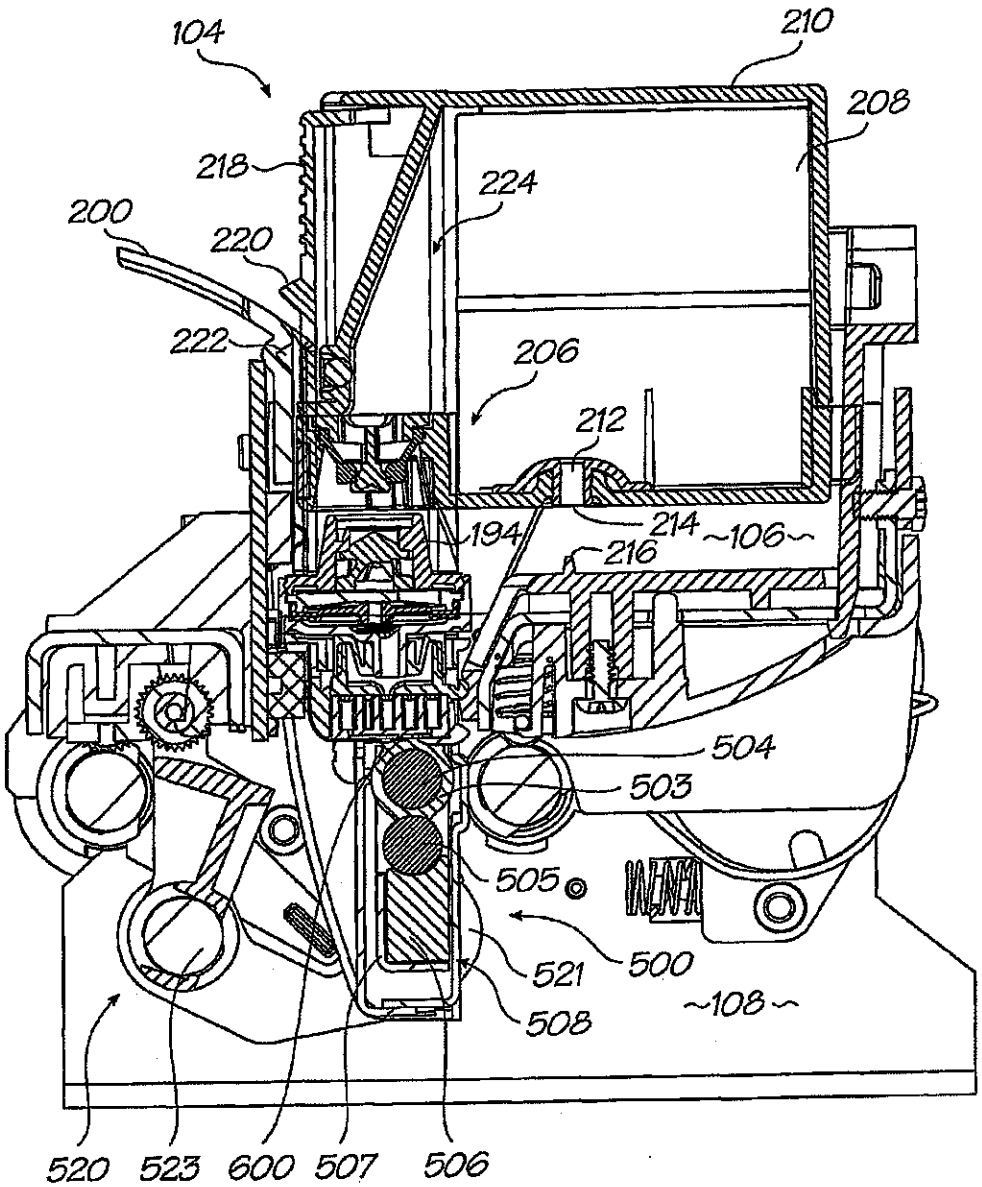

104
210
208
218
224
200
220
222
206
212
214
194
216
106
504
503
505
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521
508
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520
523
600
507
506

FIG. 15

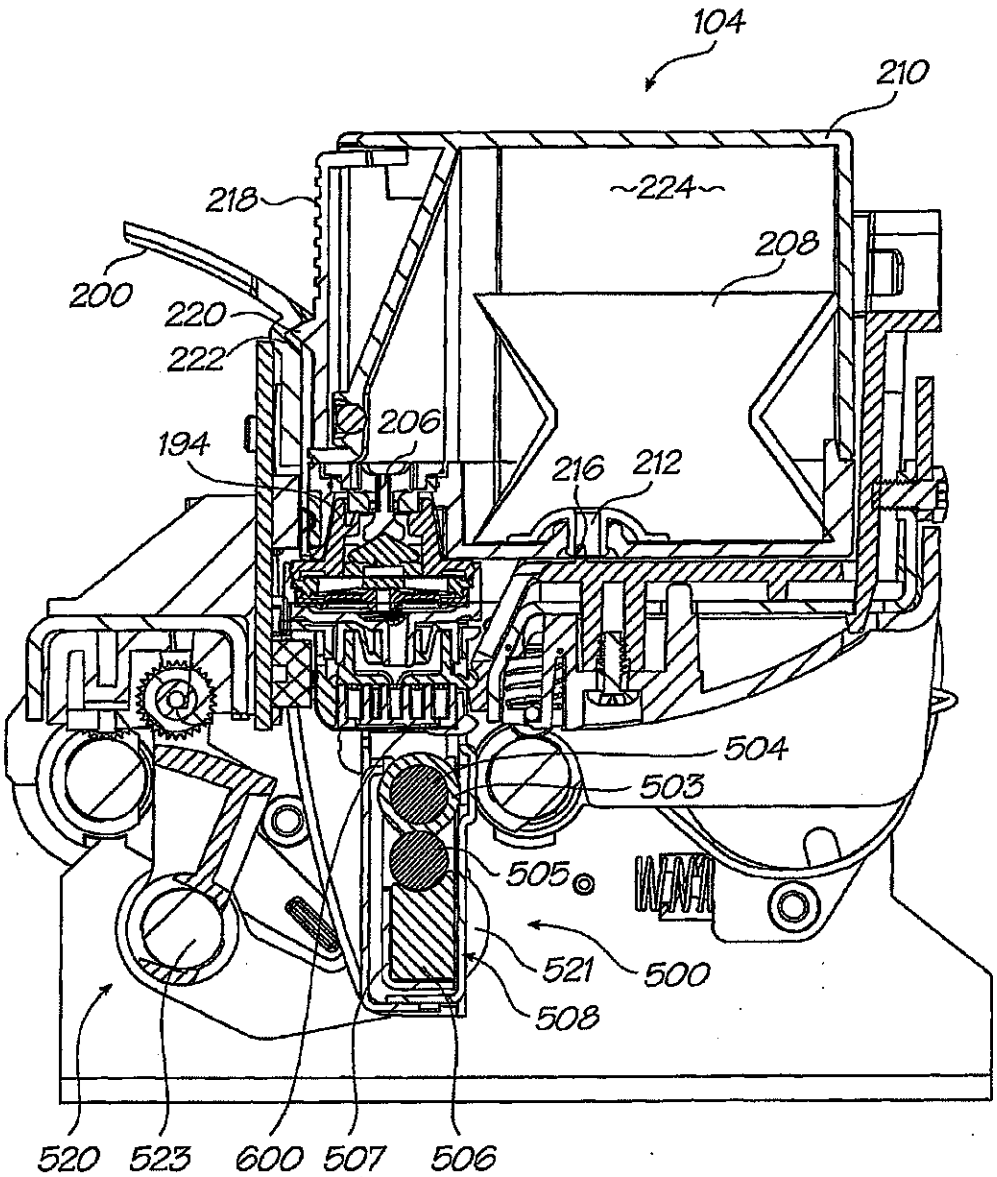

104
210
218
224
208
200
220
222
206
194
216
212
504
503
505
521
500
508
520
523
600
507
506

FIG. 16

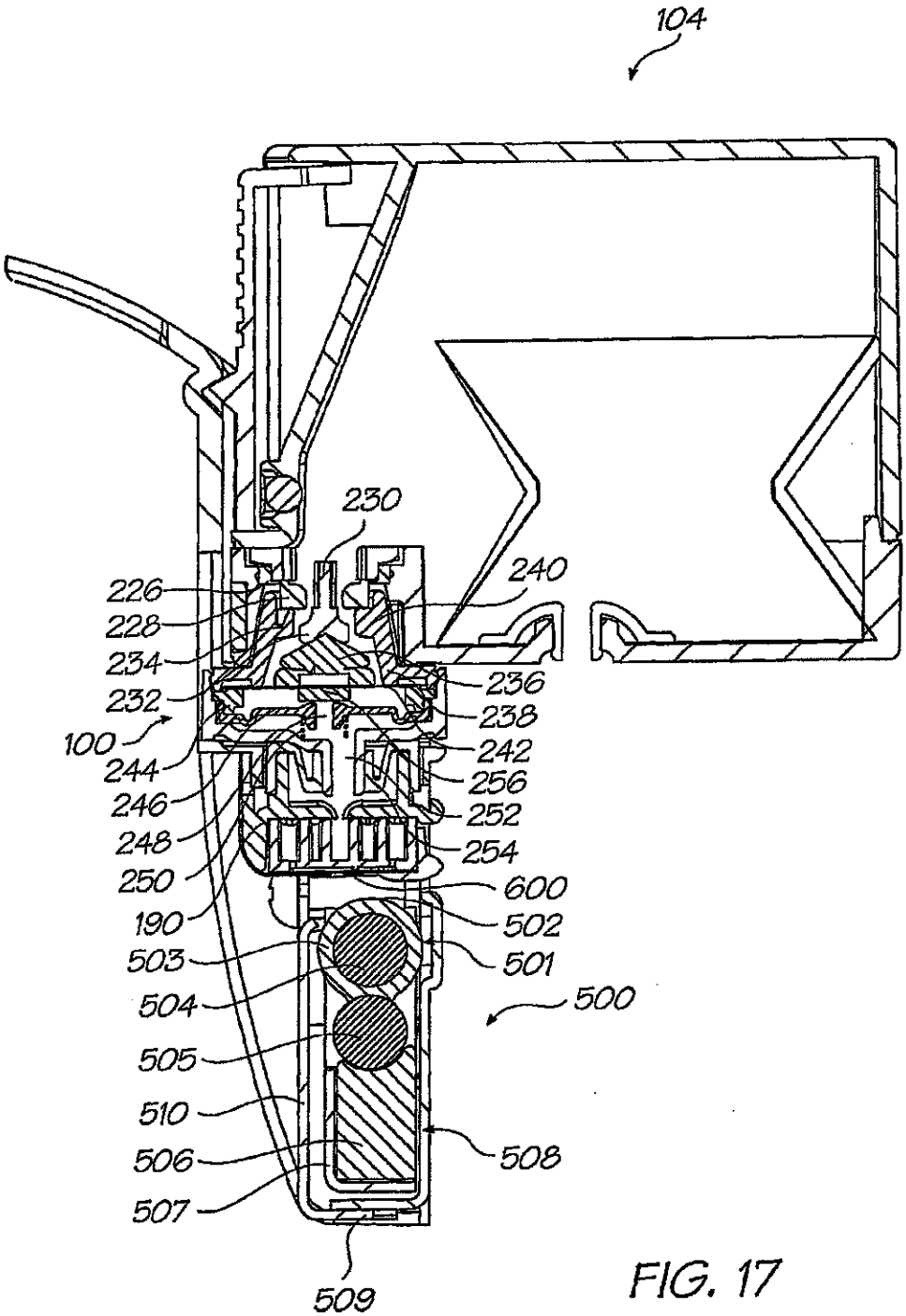

104
230
240
226
228
234
232
100
244
246
248
250
190
503
504
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510
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507
509
236
238
242
256
252
254
600
502
501
500
508

FIG. 17

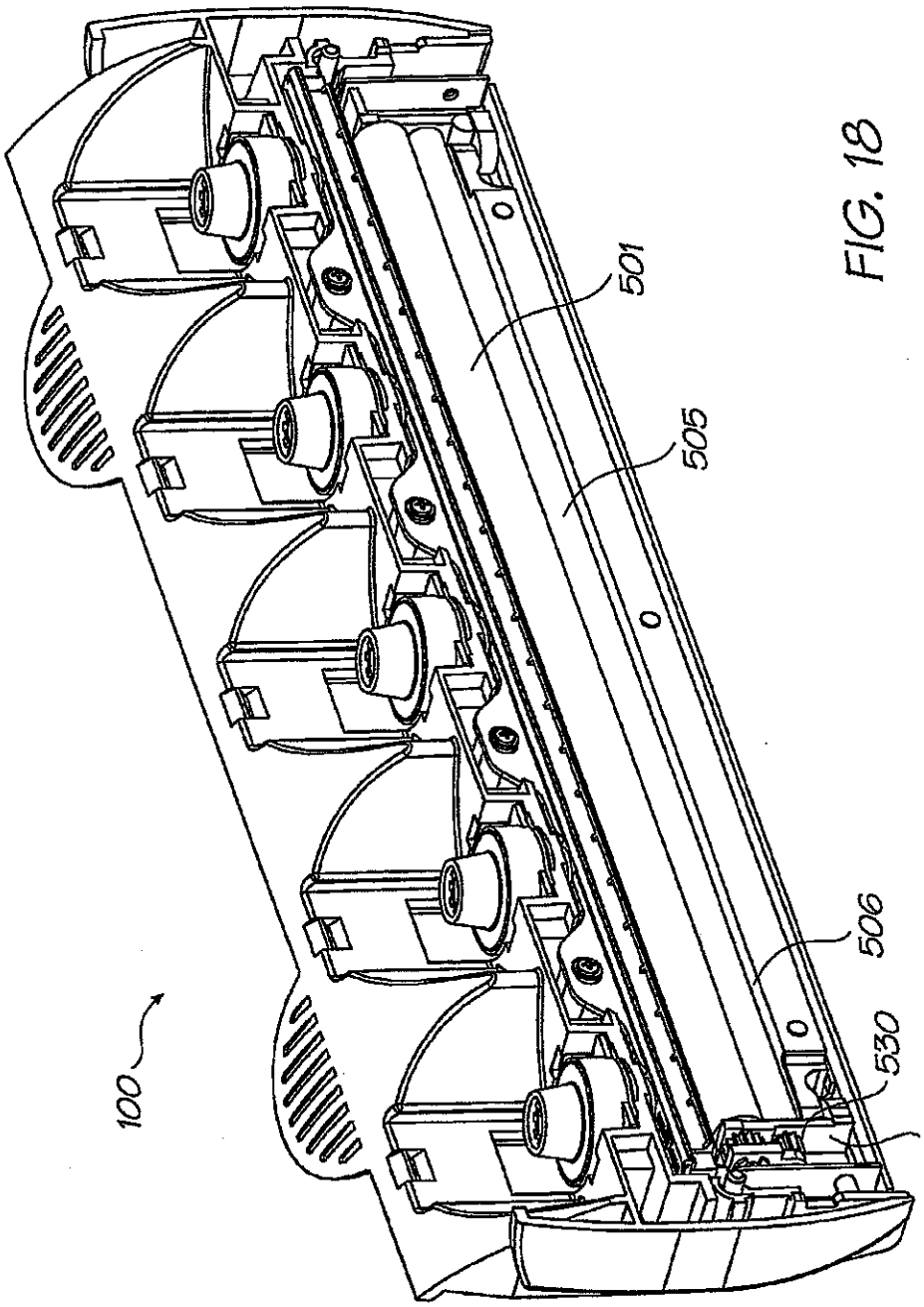


FIG. 18

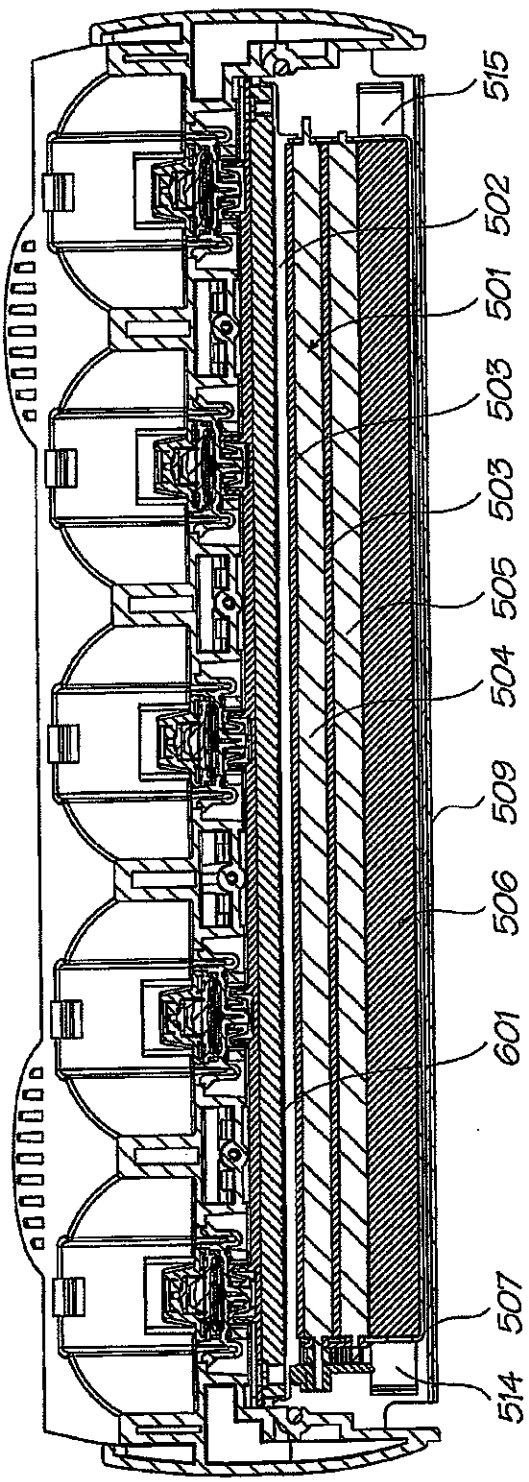


FIG. 19

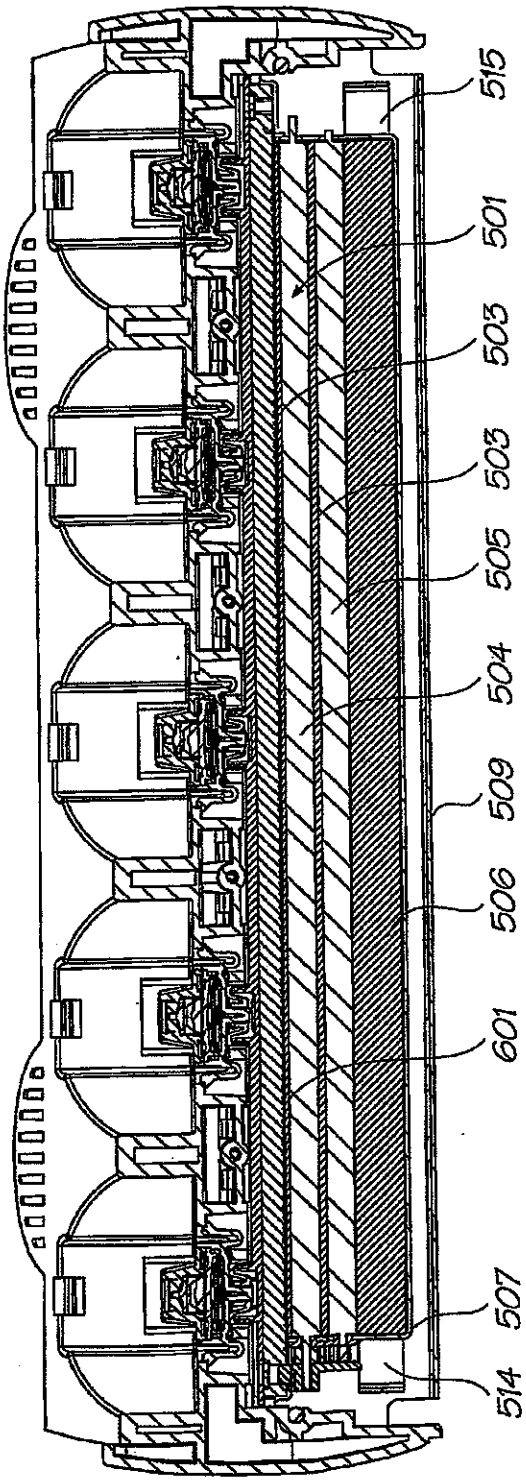


FIG. 20

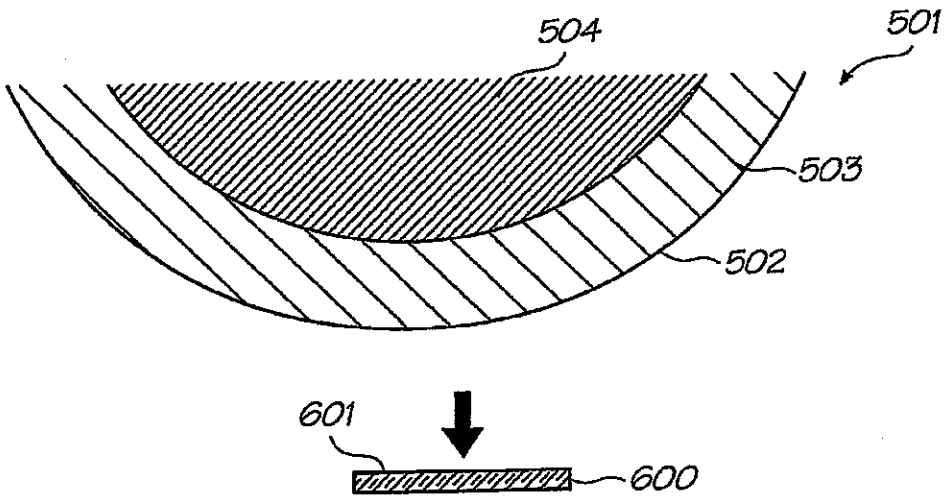


FIG. 21A

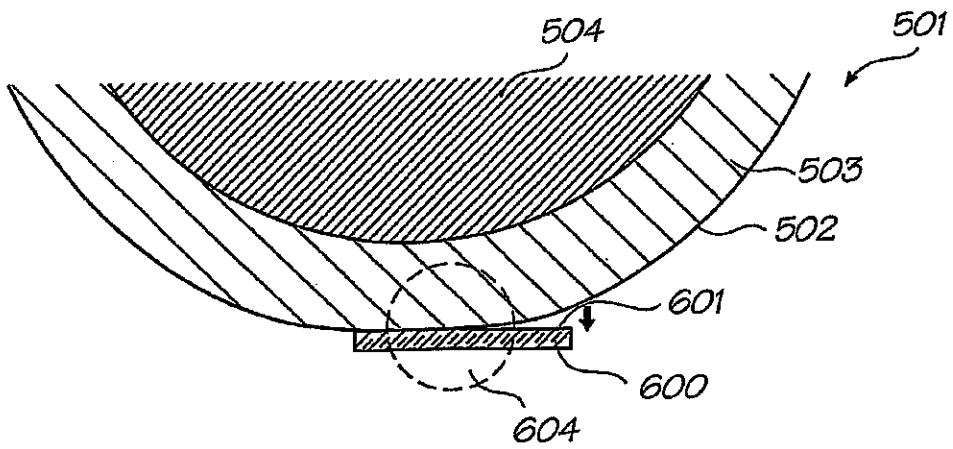


FIG. 21B

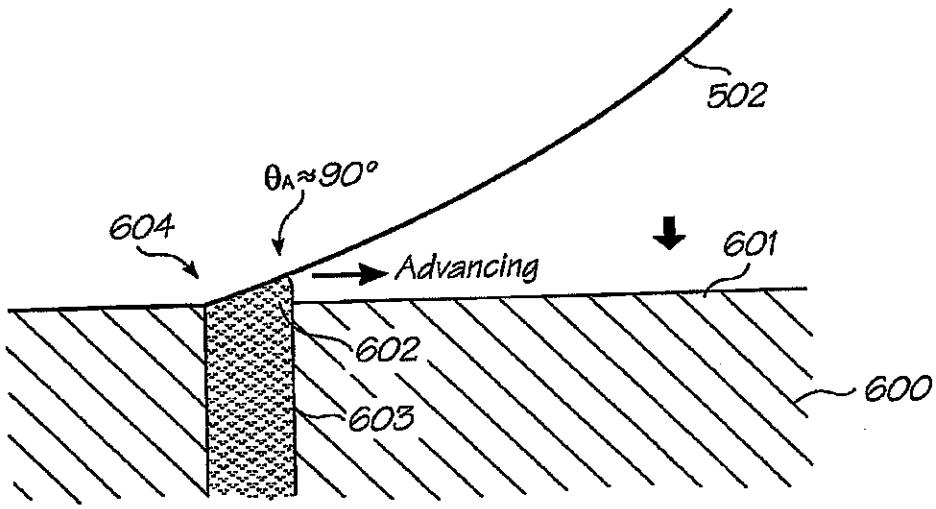


FIG. 21C

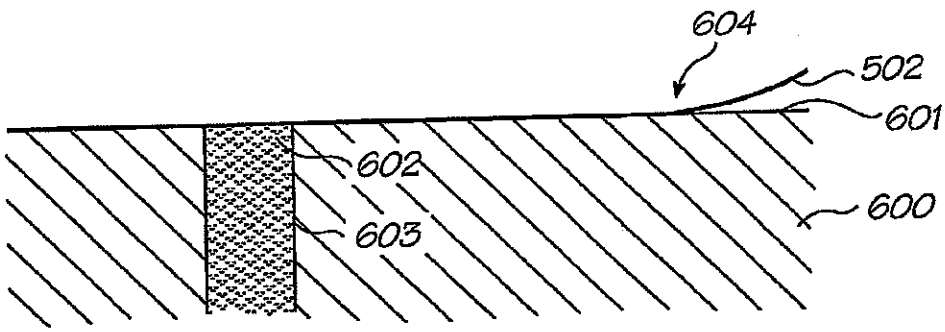


FIG. 21D

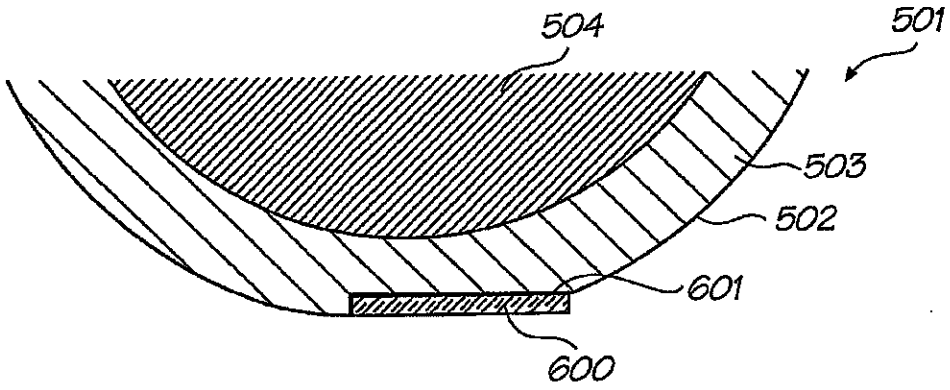


FIG. 22A

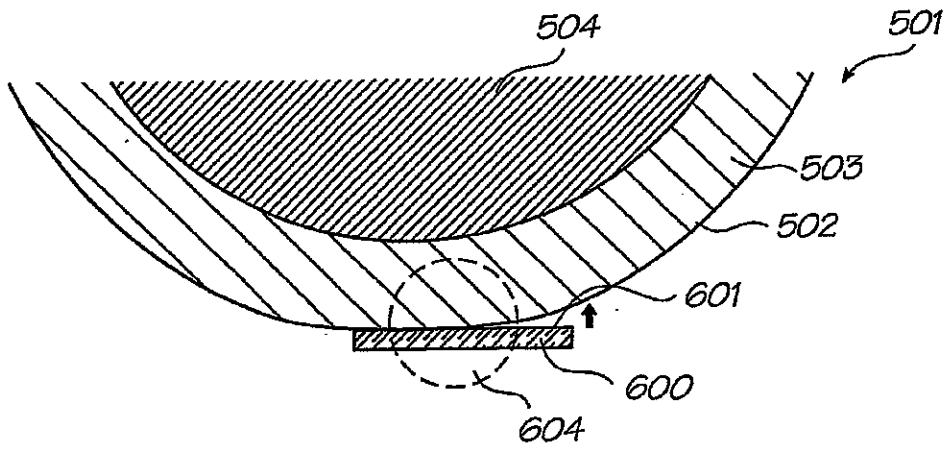


FIG. 22B

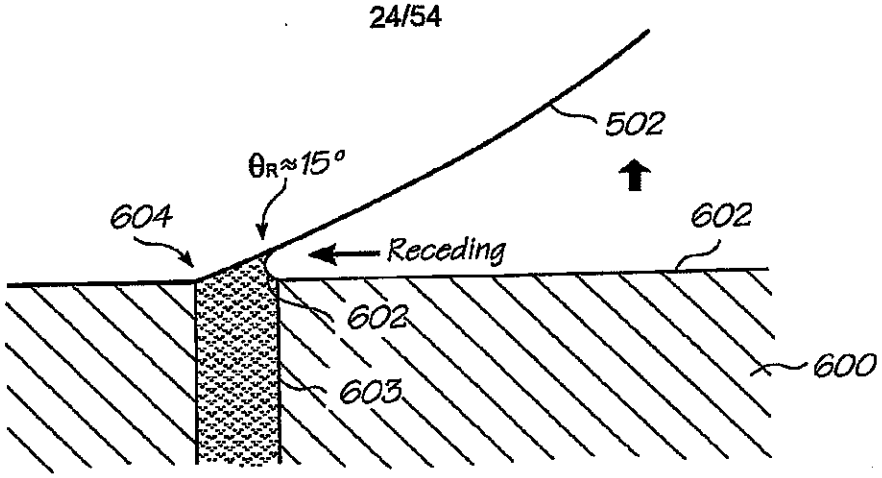


FIG. 22C

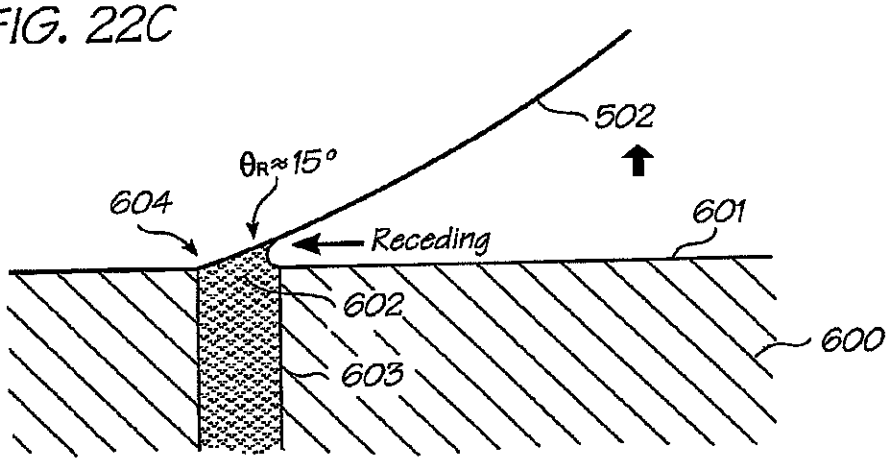


FIG. 22D

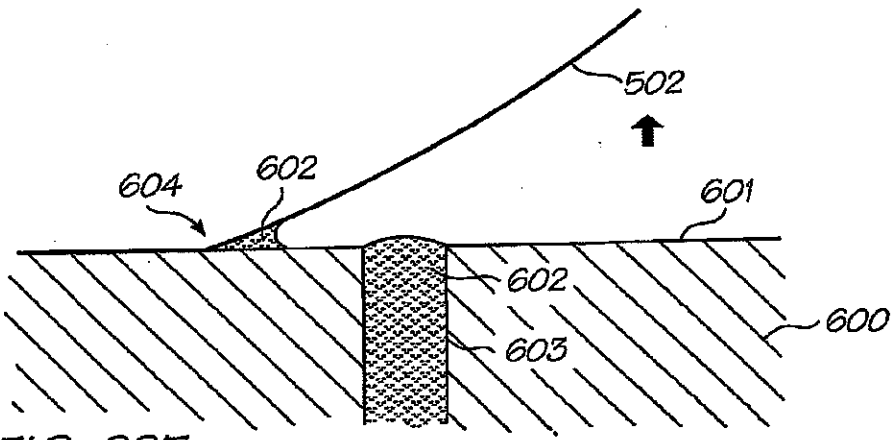


FIG. 22E

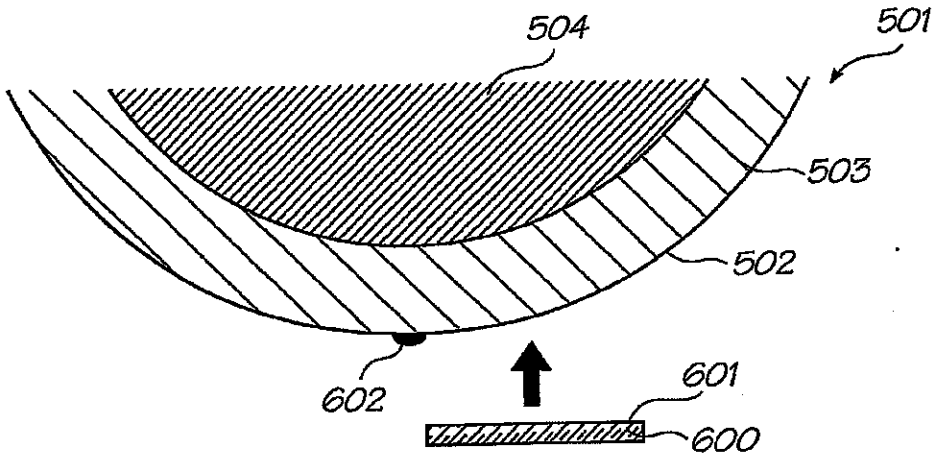


FIG. 23

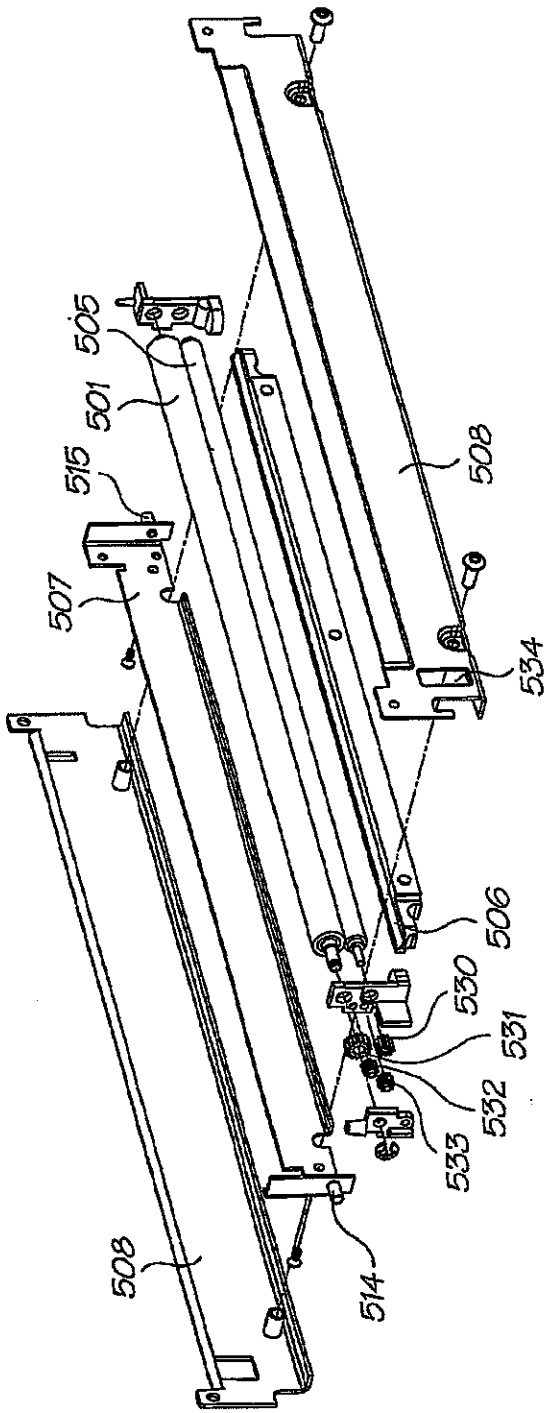


FIG. 24

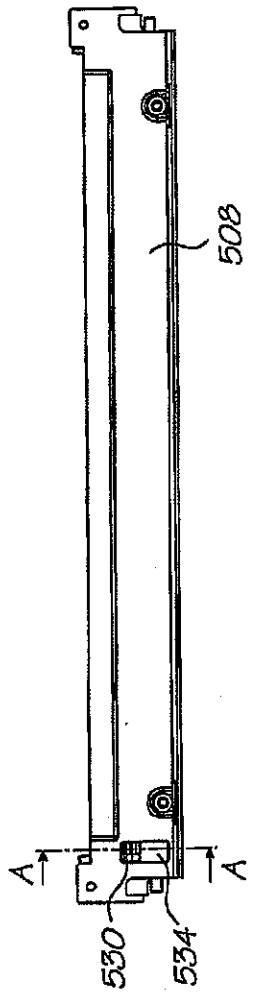


FIG. 25

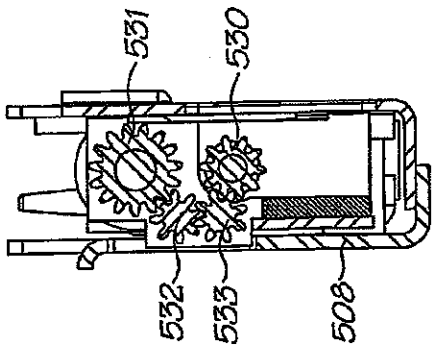


FIG. 26

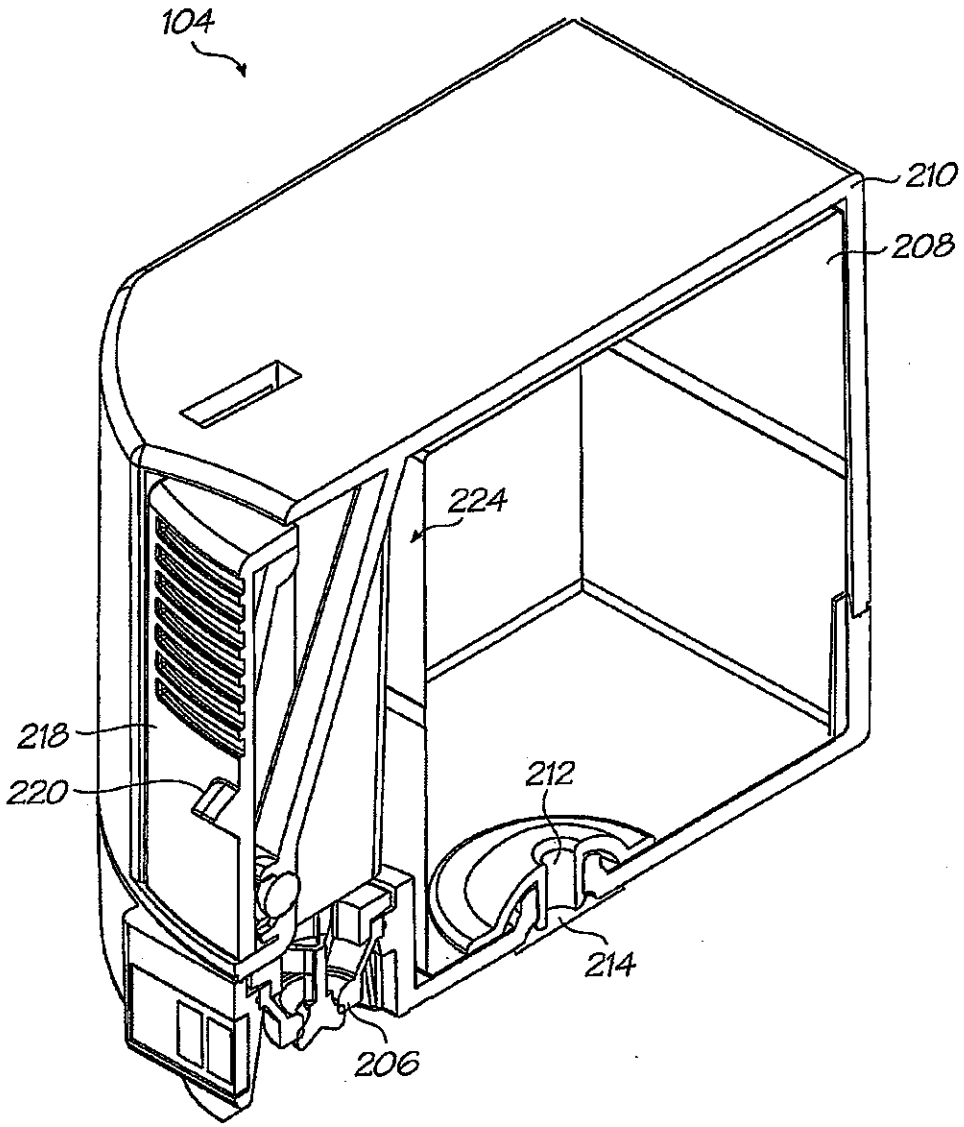


FIG. 27

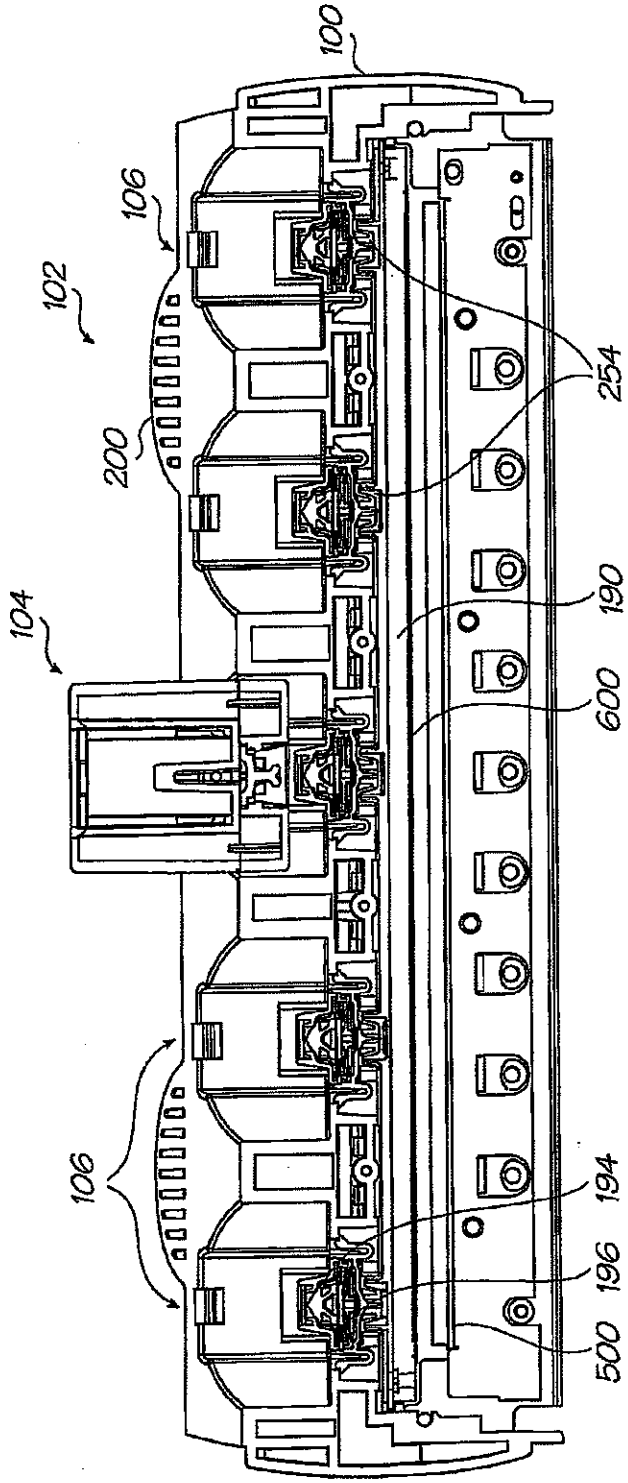


FIG. 28

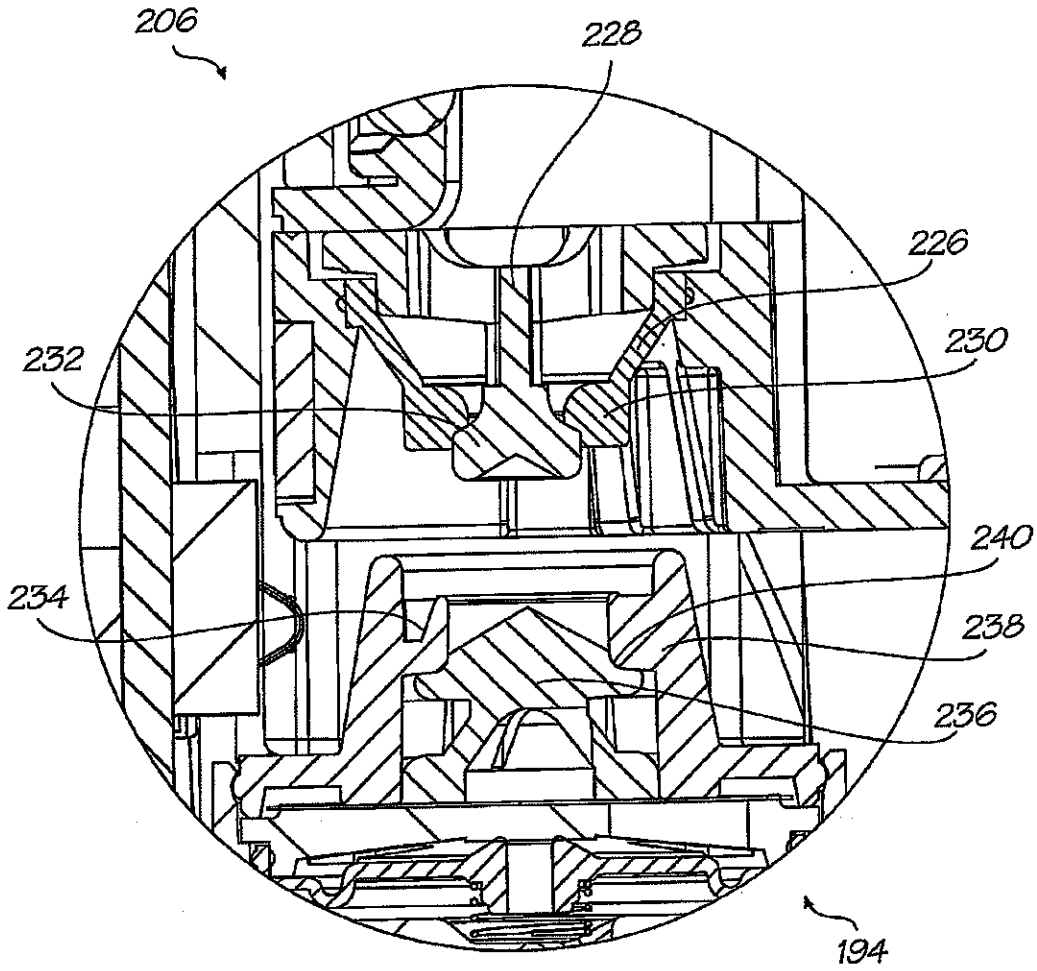


FIG. 29

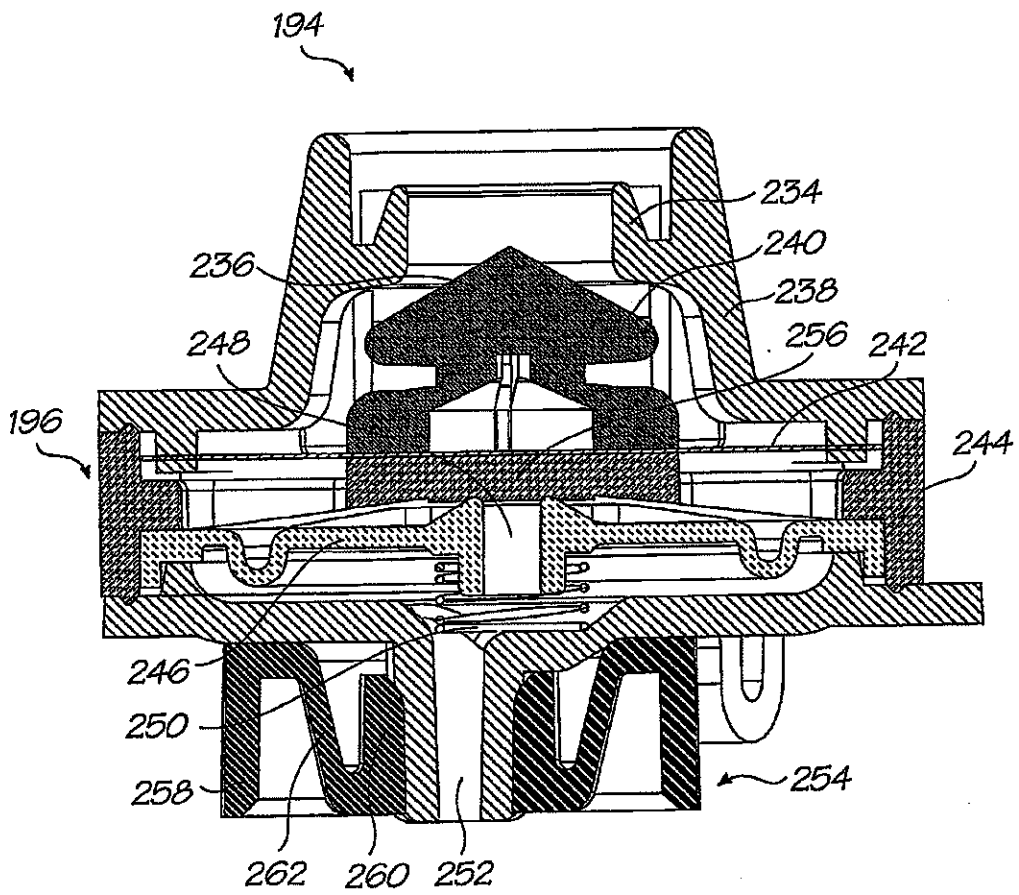

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FIG. 30A

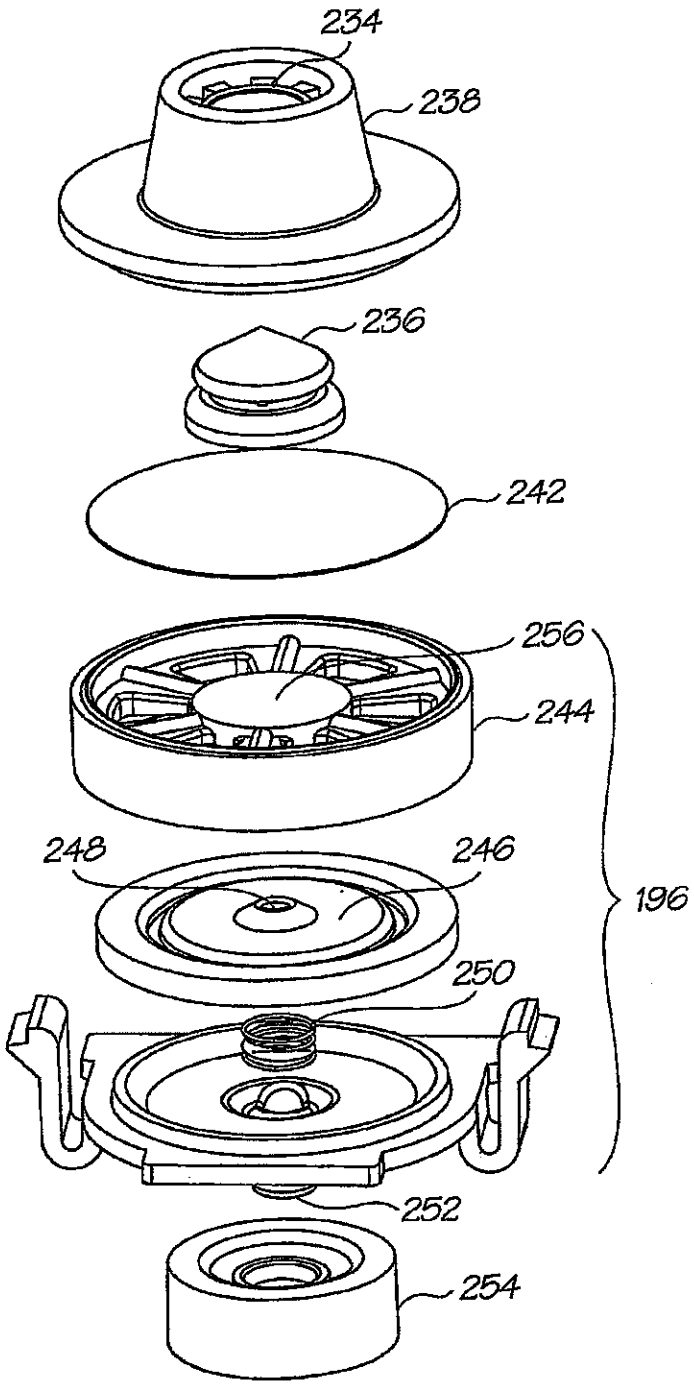


FIG. 30B

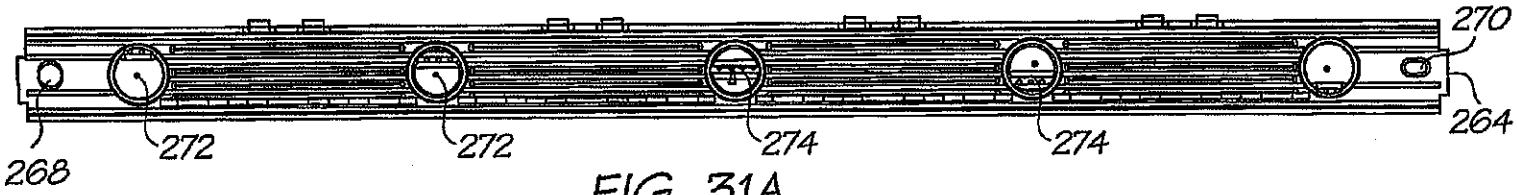


FIG. 31A

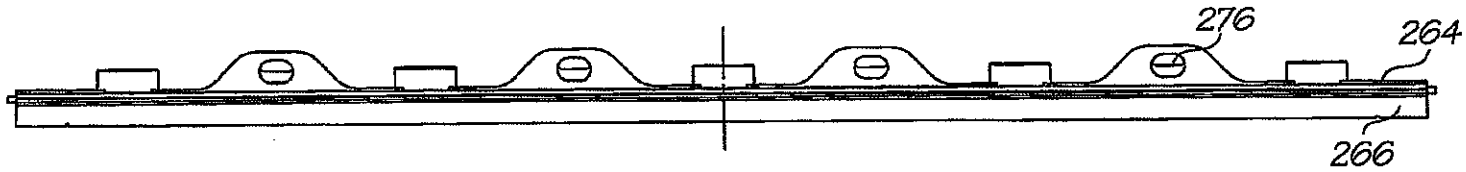


FIG. 31B

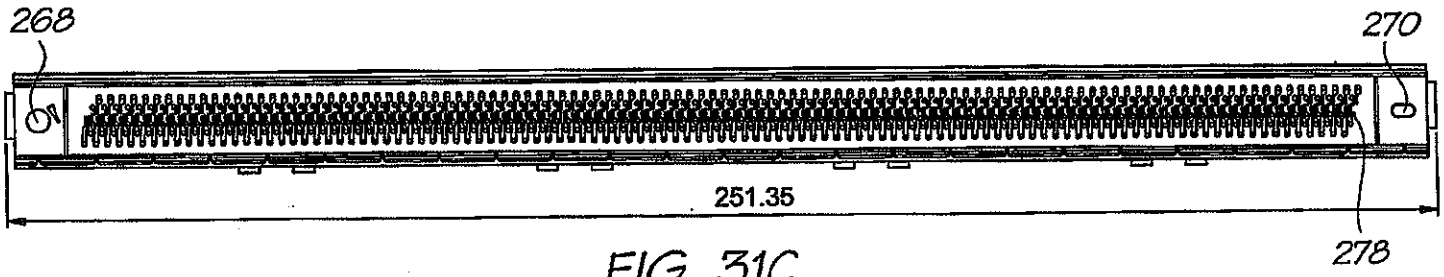


FIG. 31C

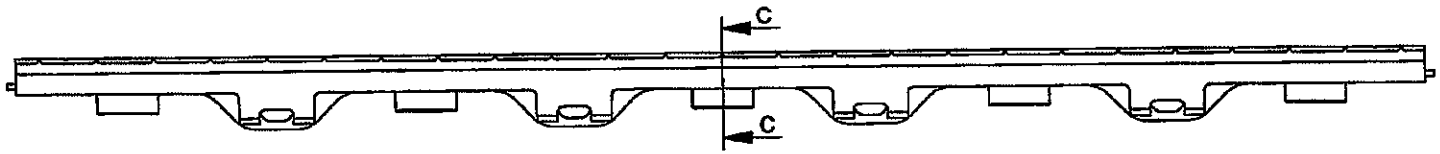


FIG. 31D

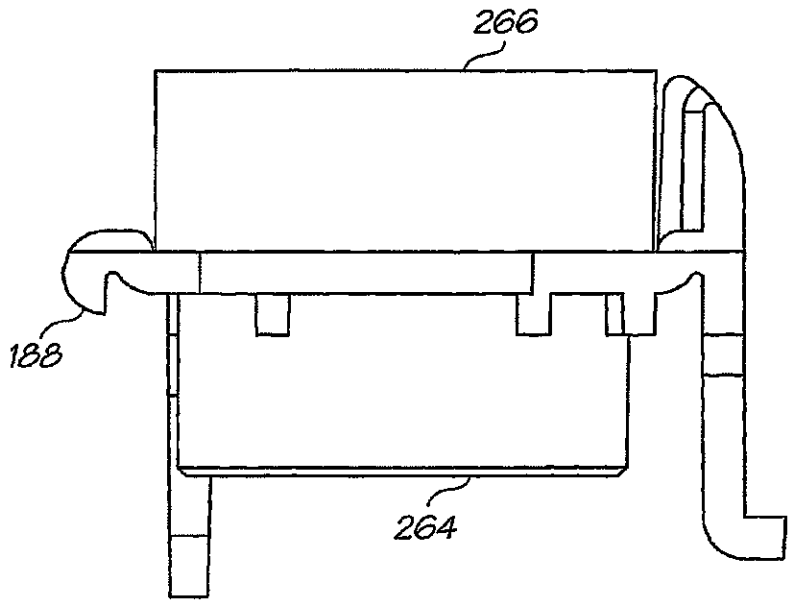


FIG. 31E

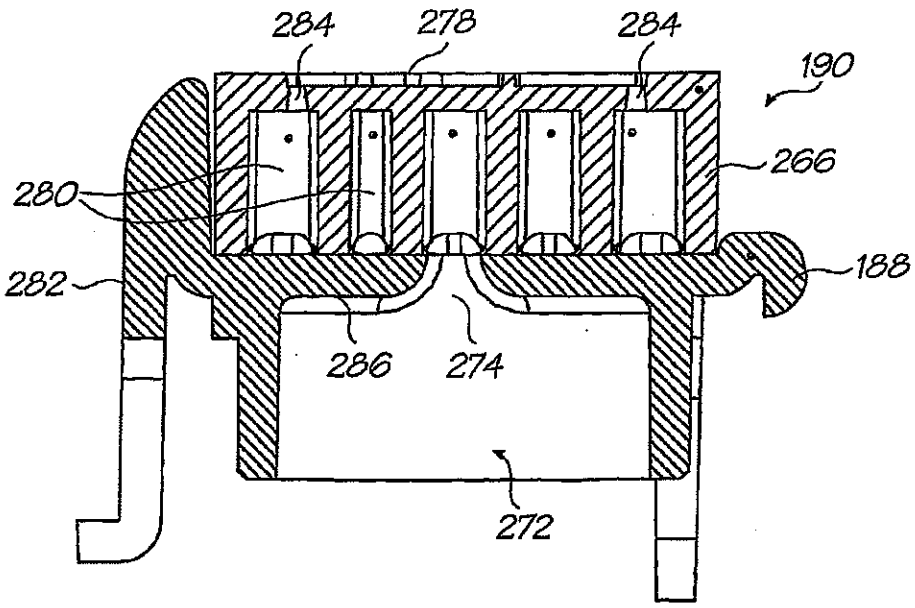


FIG. 32

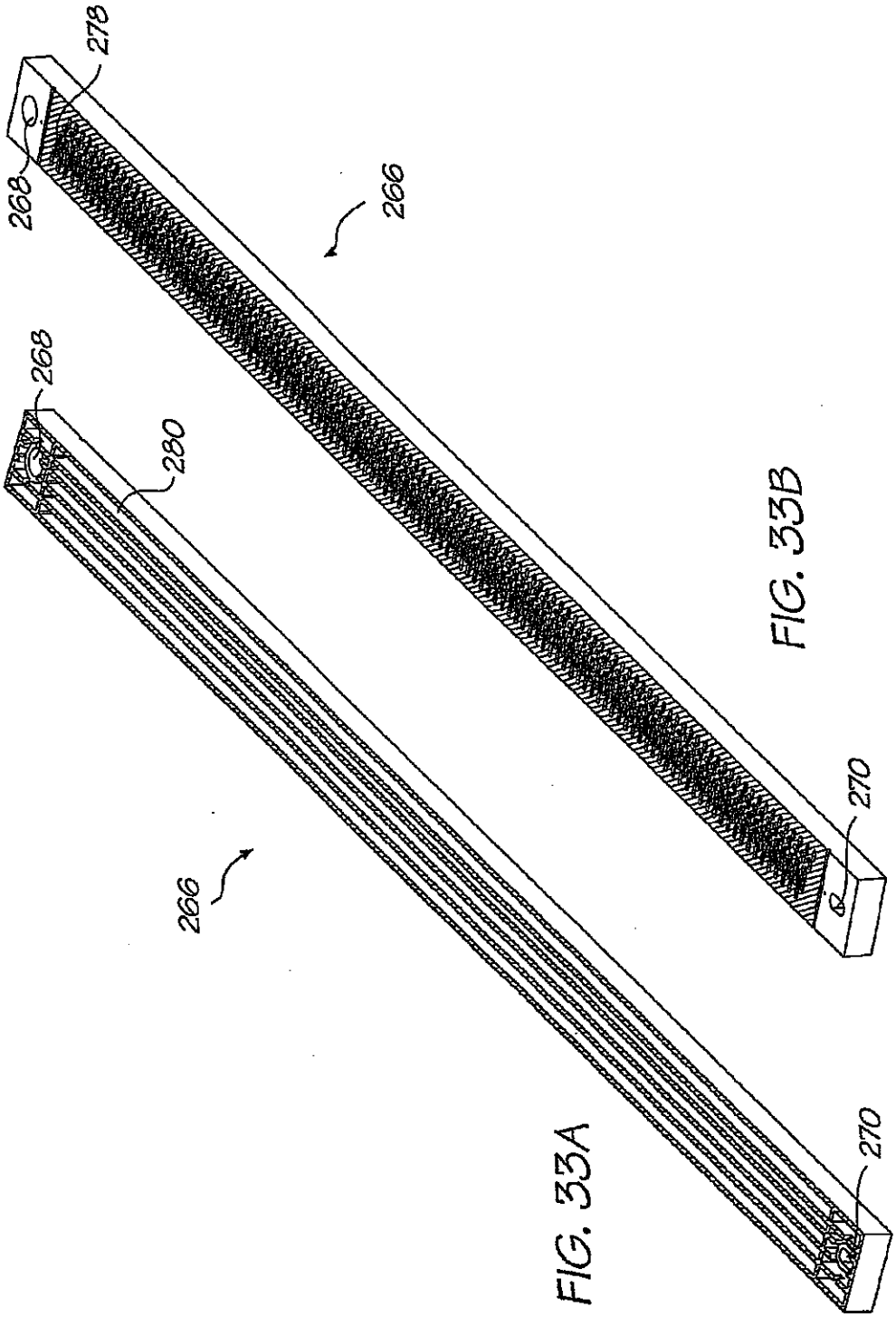


FIG. 33B

FIG. 33A

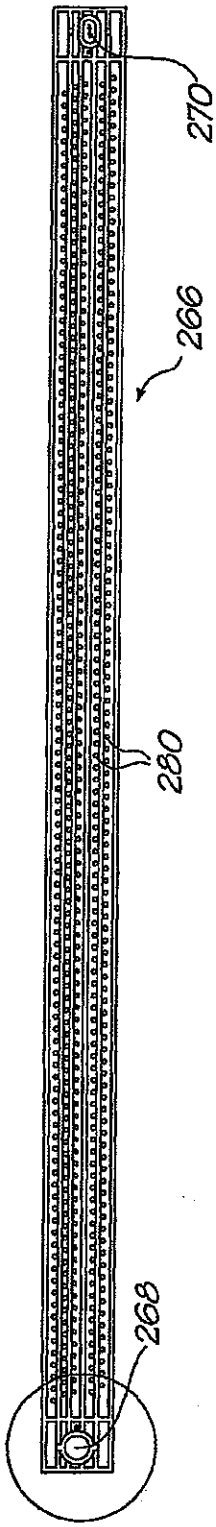


FIG. 34

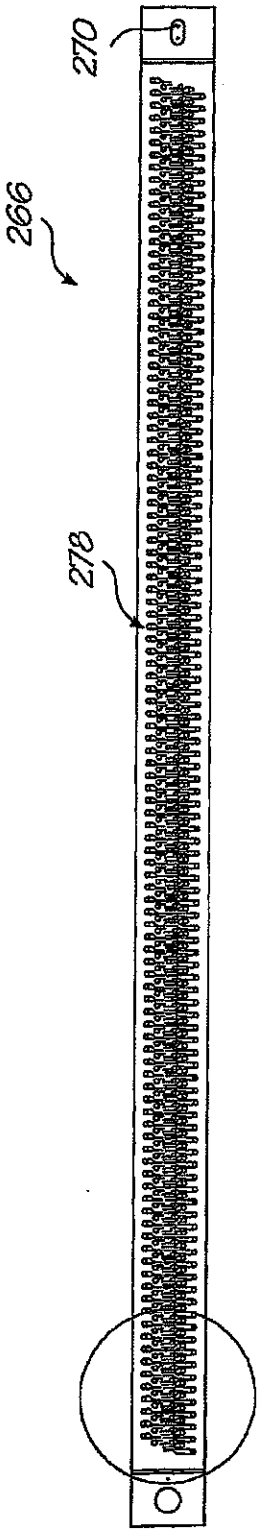


FIG. 36

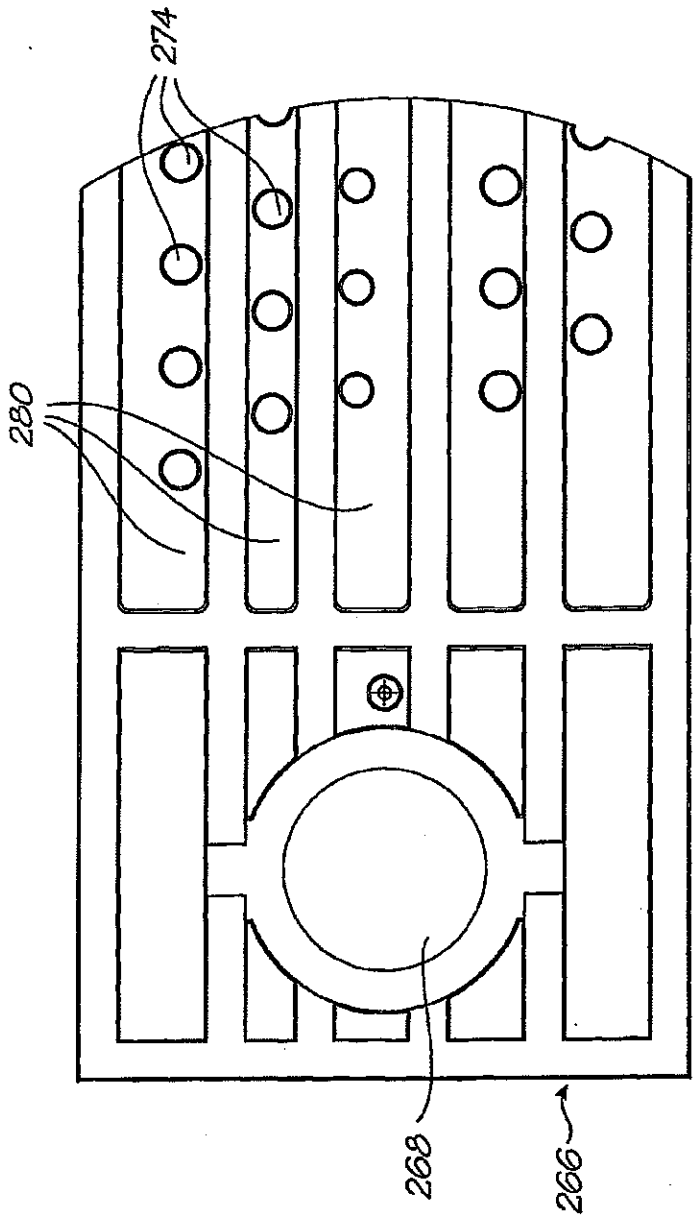


FIG. 35

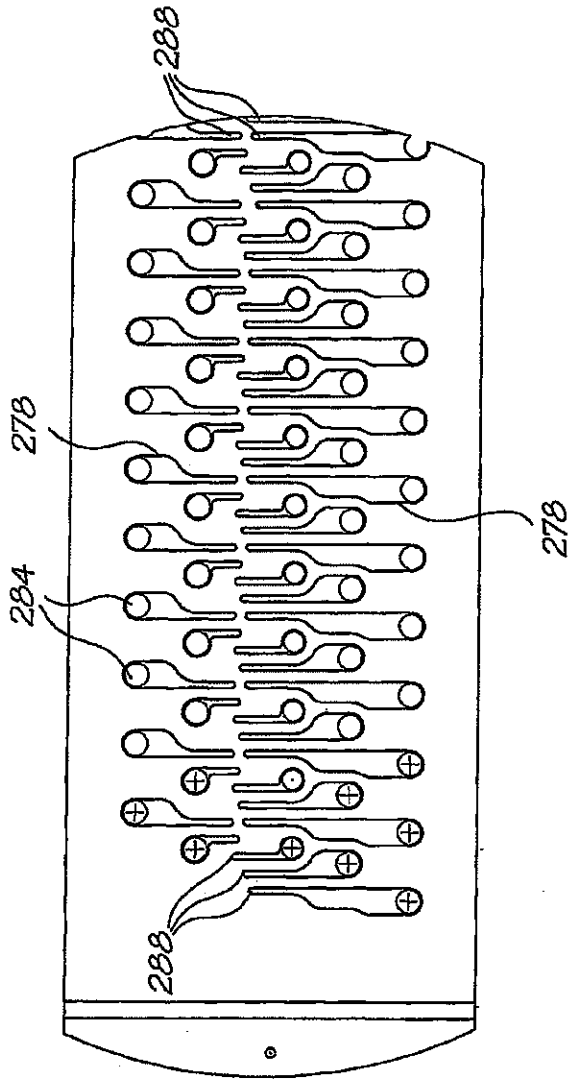


FIG. 37

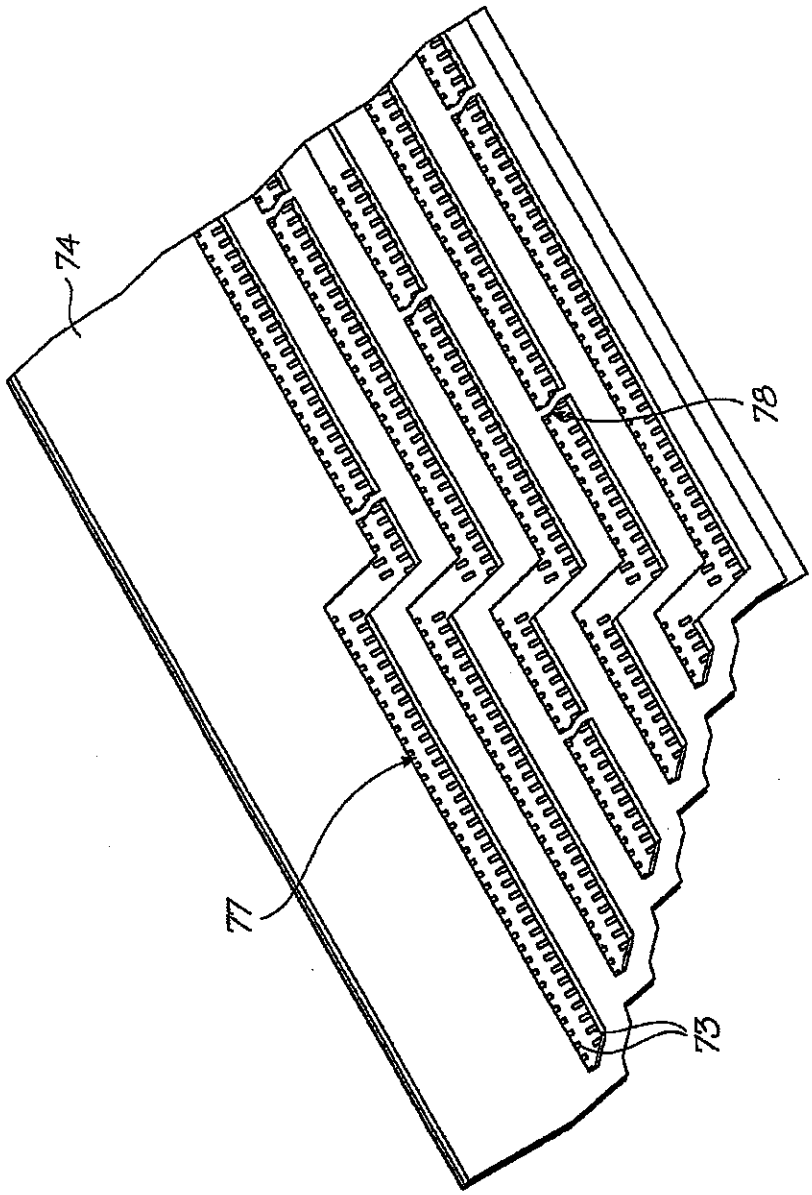


FIG. 38

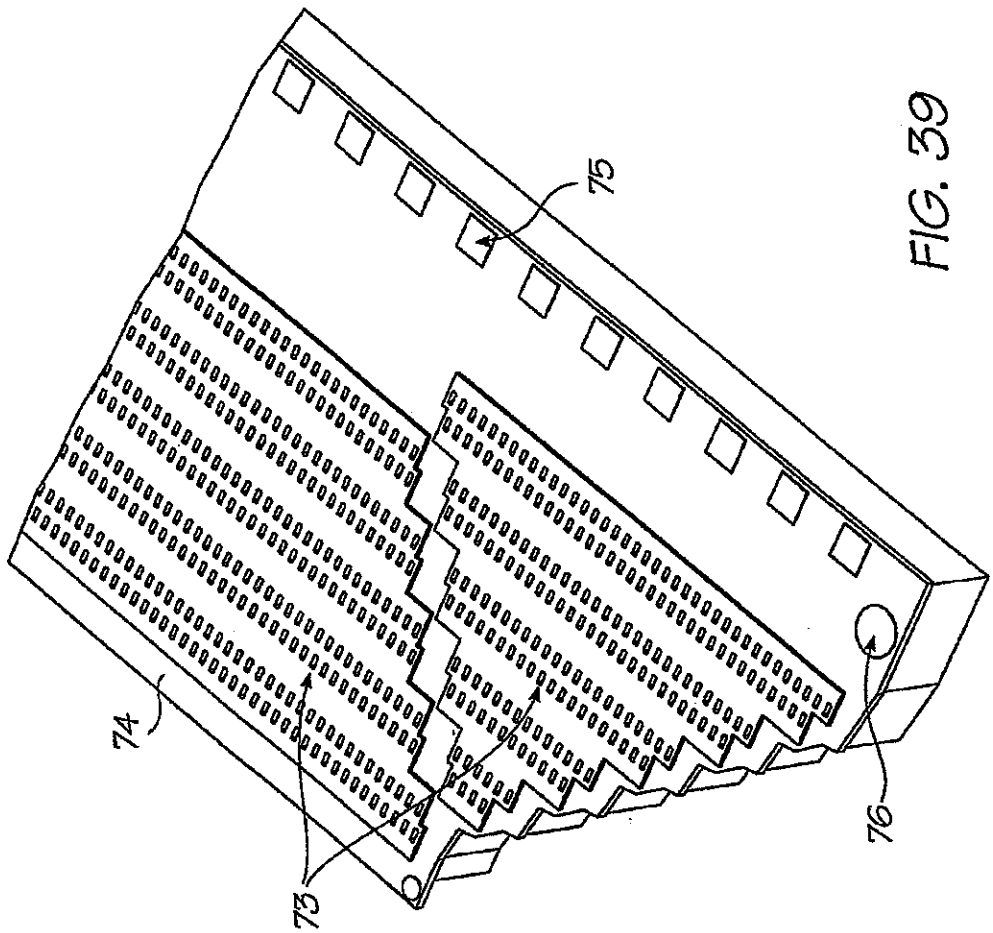


FIG. 39

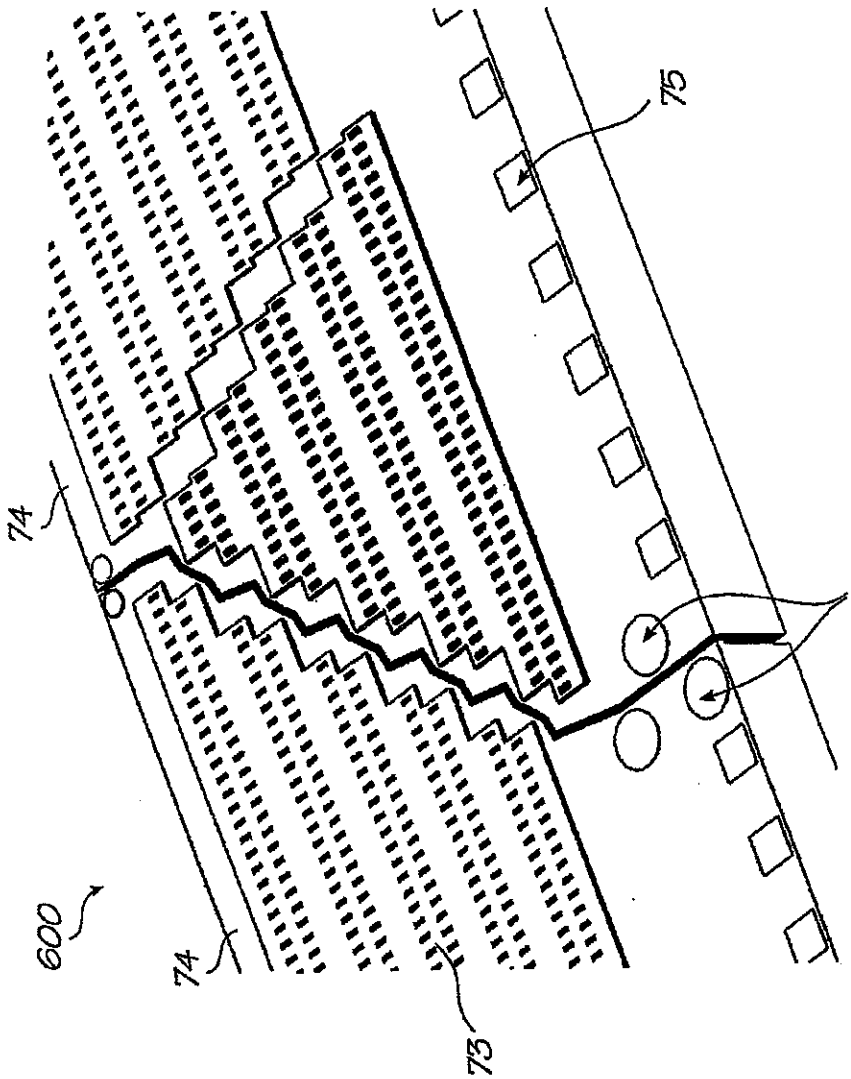


FIG. 40

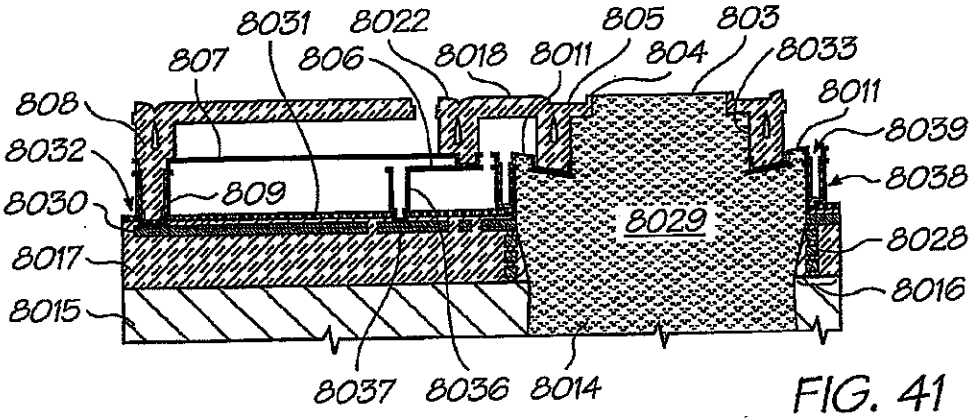


FIG. 41

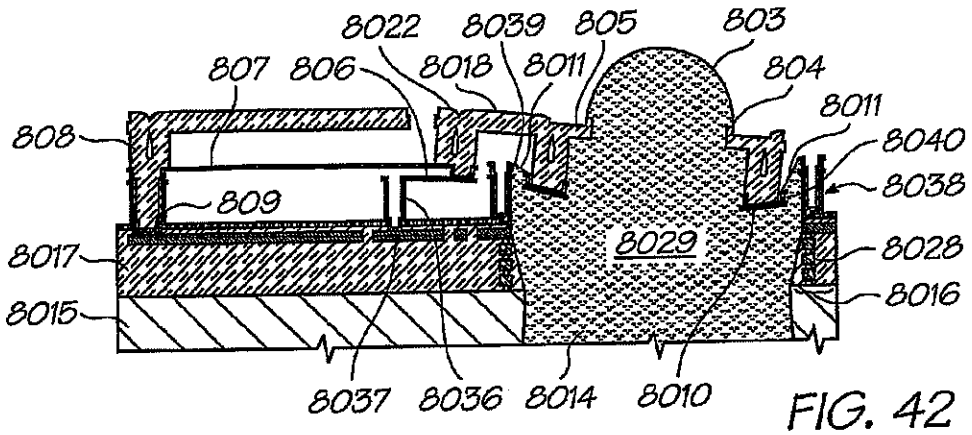


FIG. 42

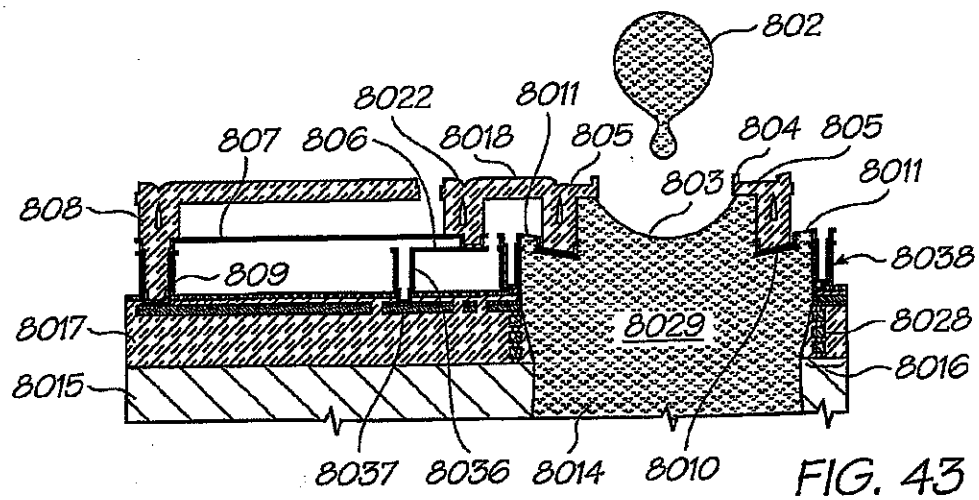


FIG. 43

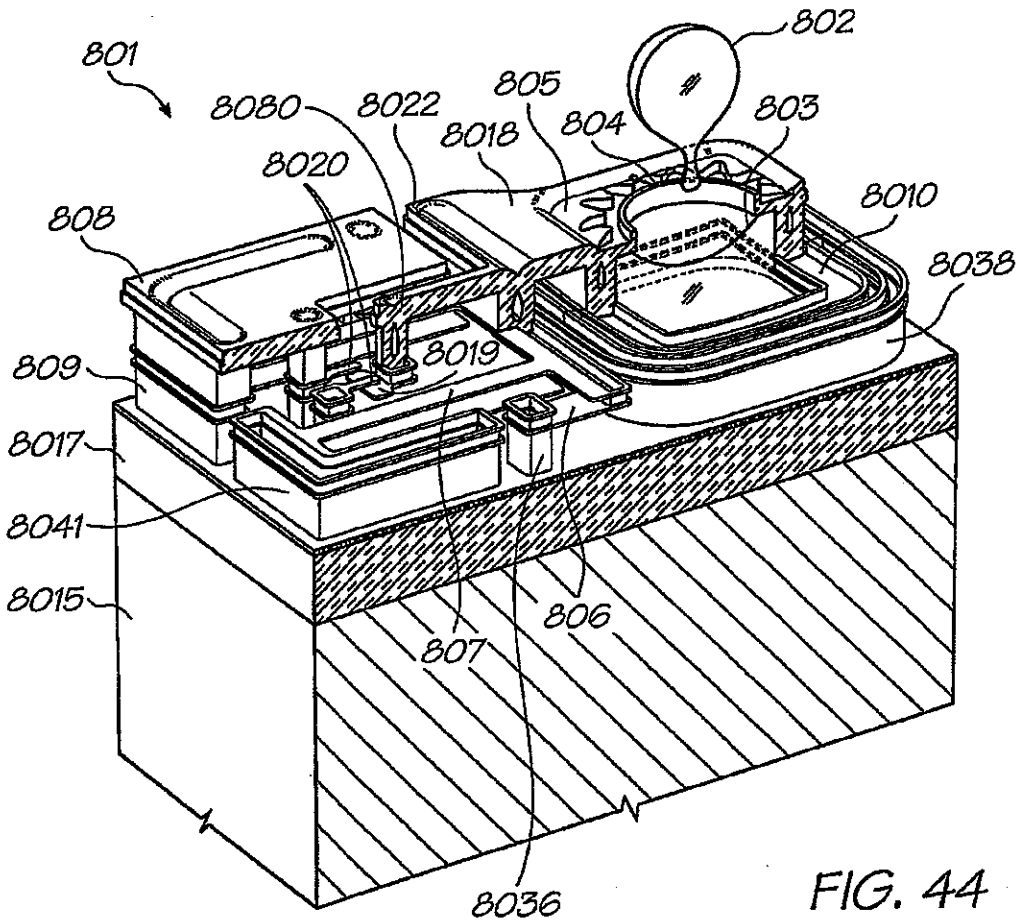

801
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8010
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8019
8017
8041
8015
807
806
8036

FIG. 44

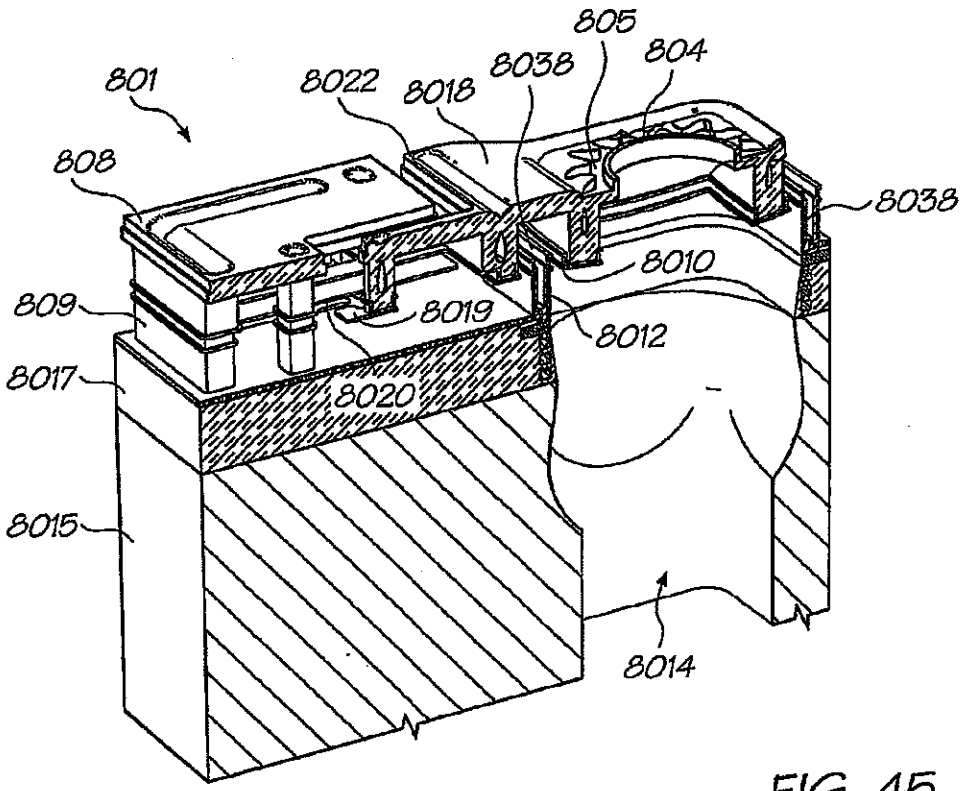

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8020
8015
8014

FIG. 45

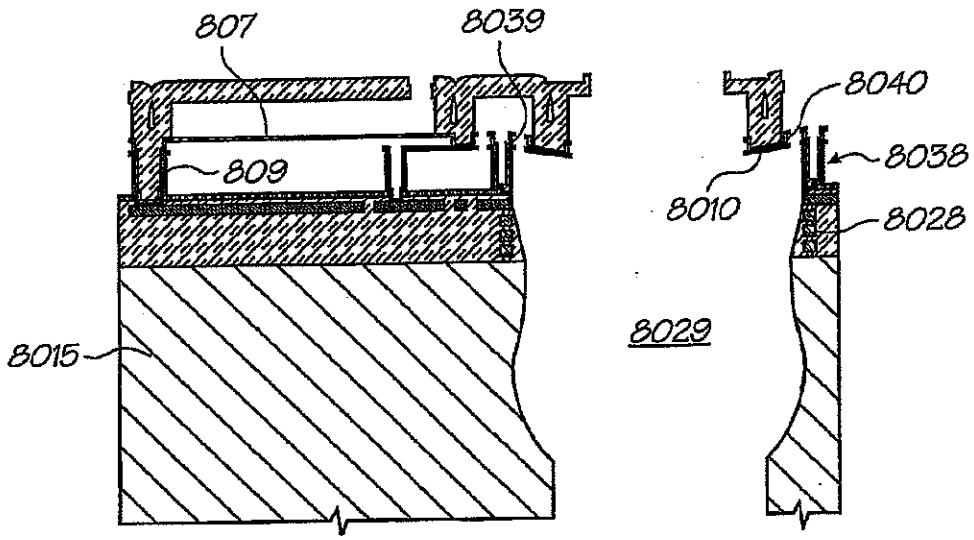

807
8039
809
8015
8040
8038
8010
8028
8029

FIG. 46

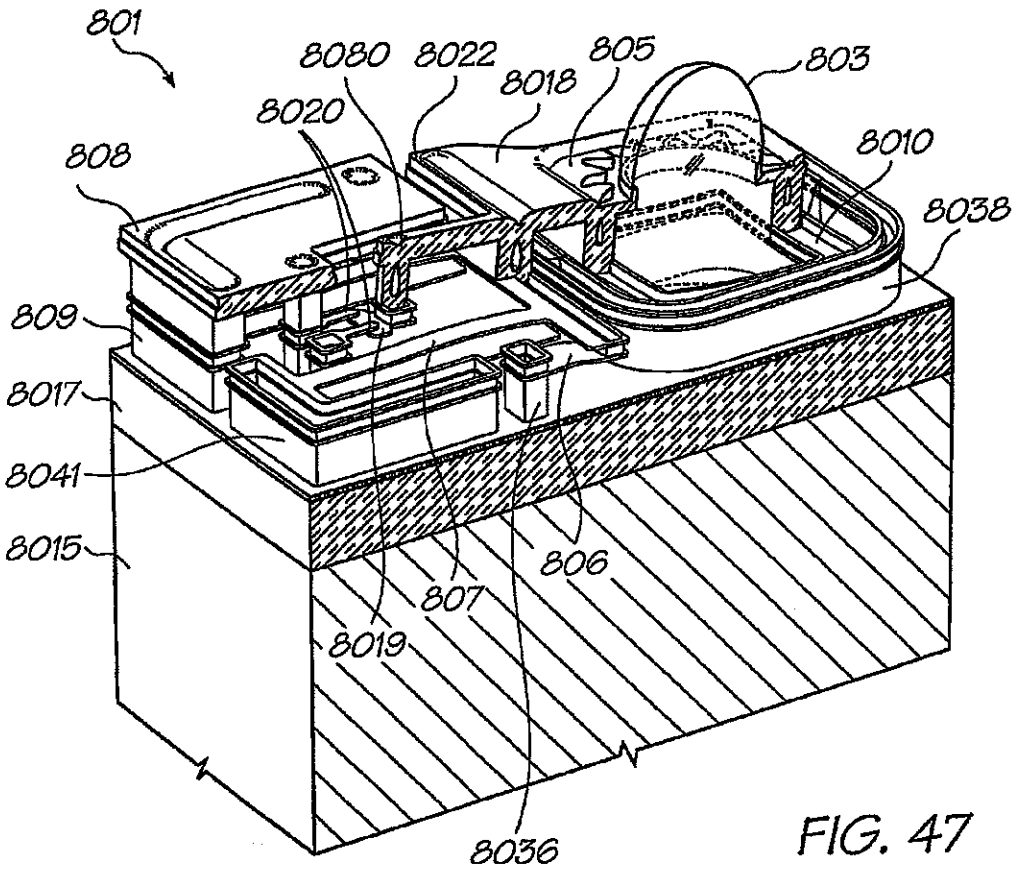

801
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FIG. 47

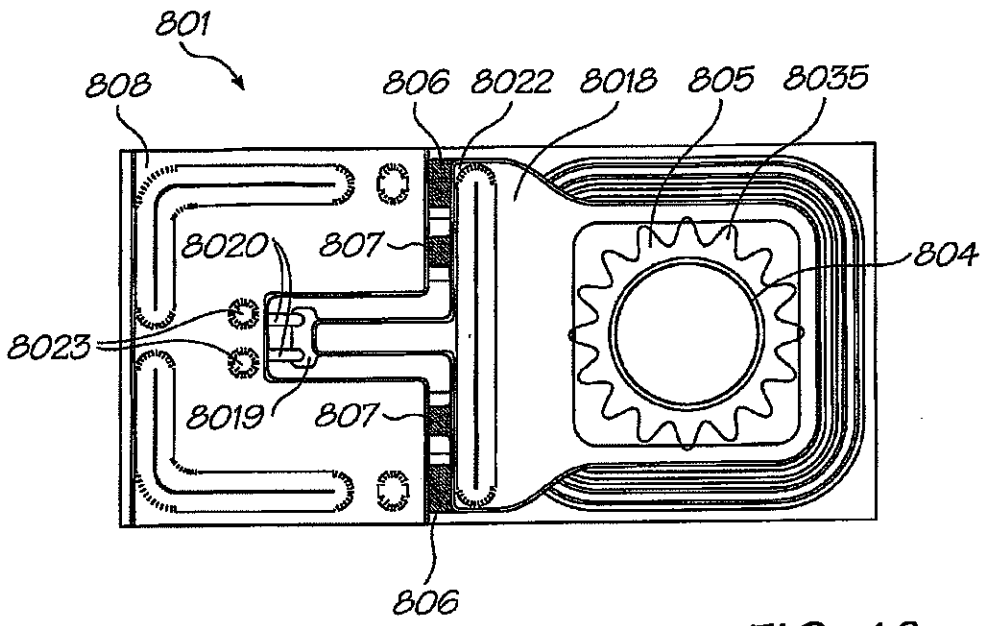

801
808
806
8022
8018
805
8035
804
8020
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8023
8019
807
806

FIG. 48

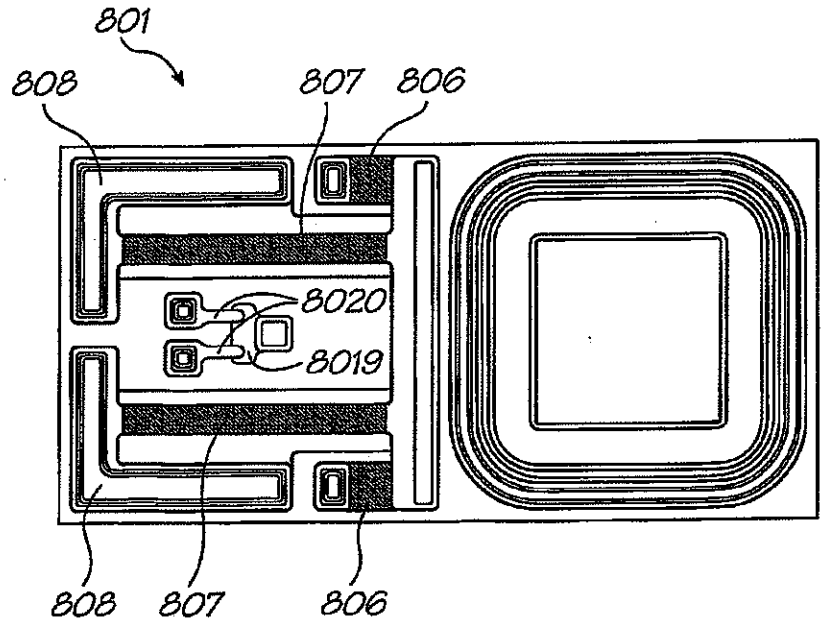

801
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8019
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807
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FIG. 49

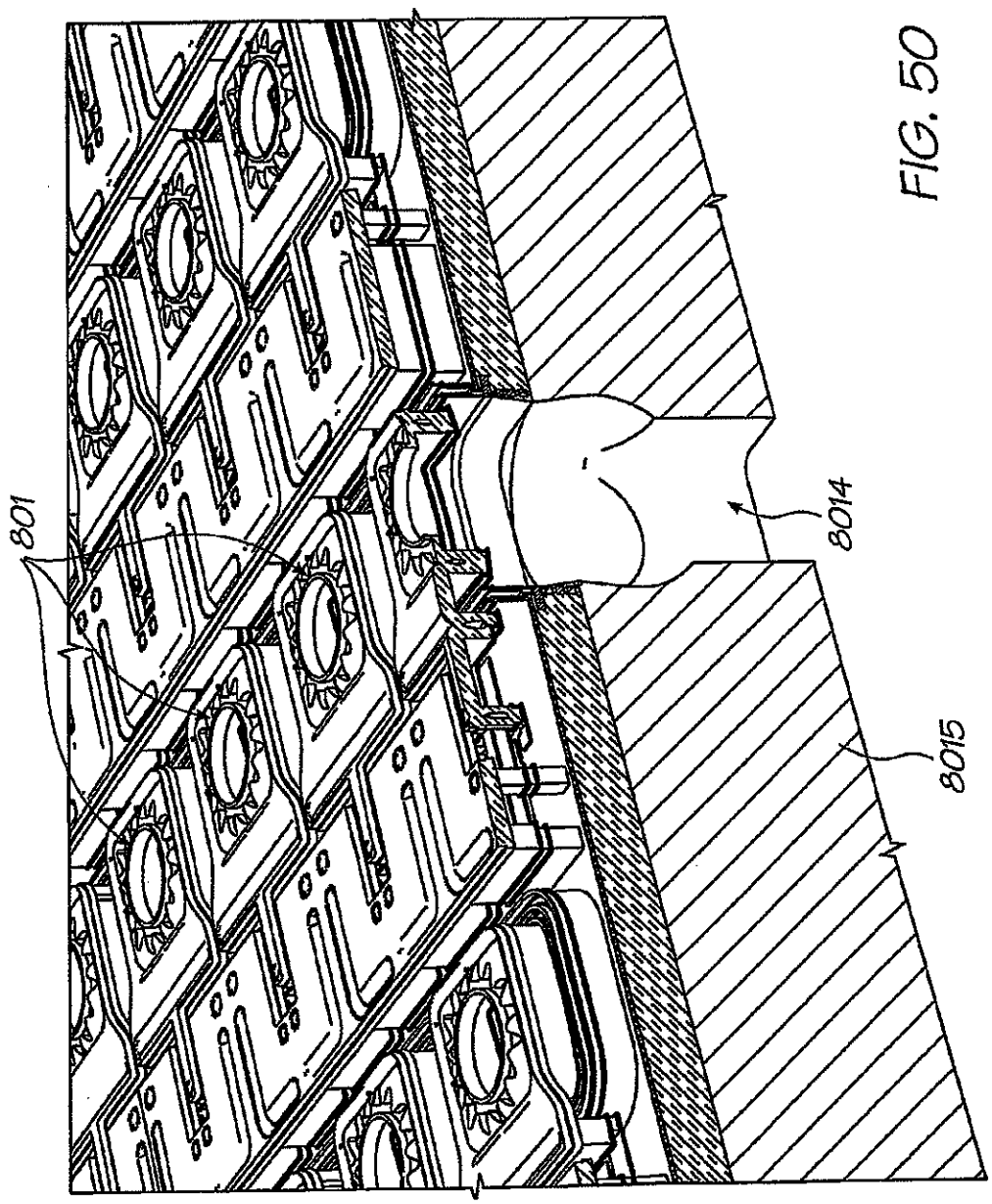


FIG. 50

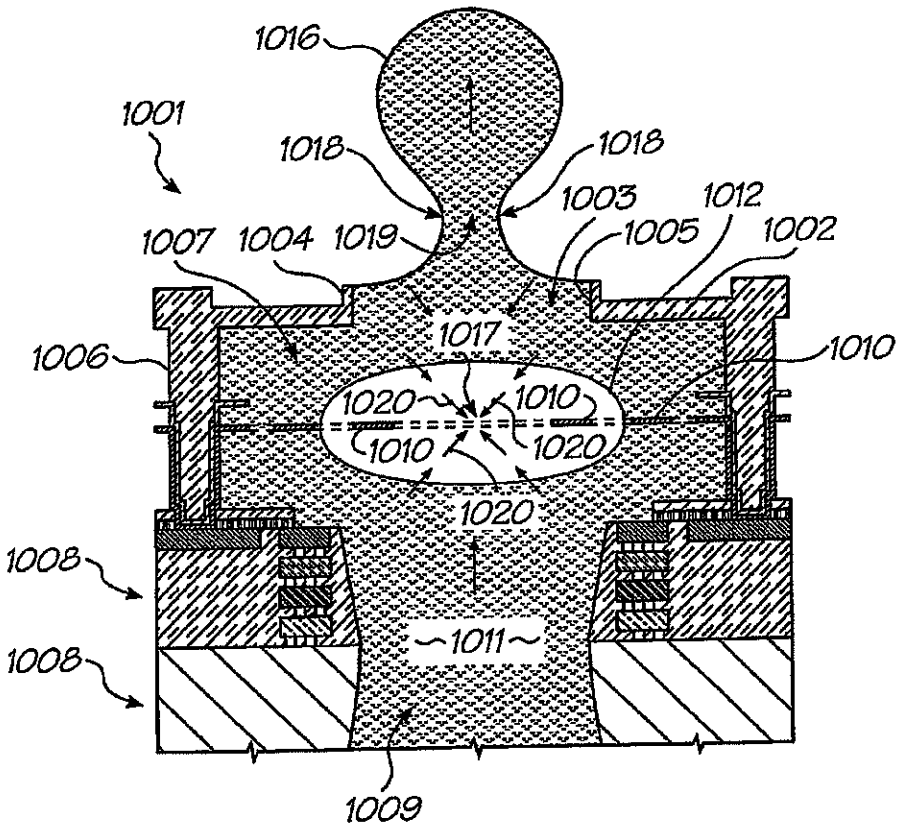

1016
1001
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1018
1003
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1008
1009

FIG. 51

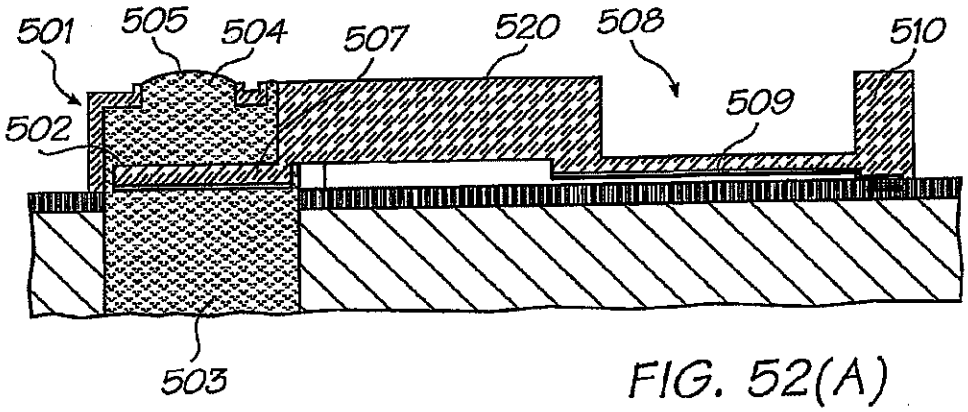


FIG. 52(A)

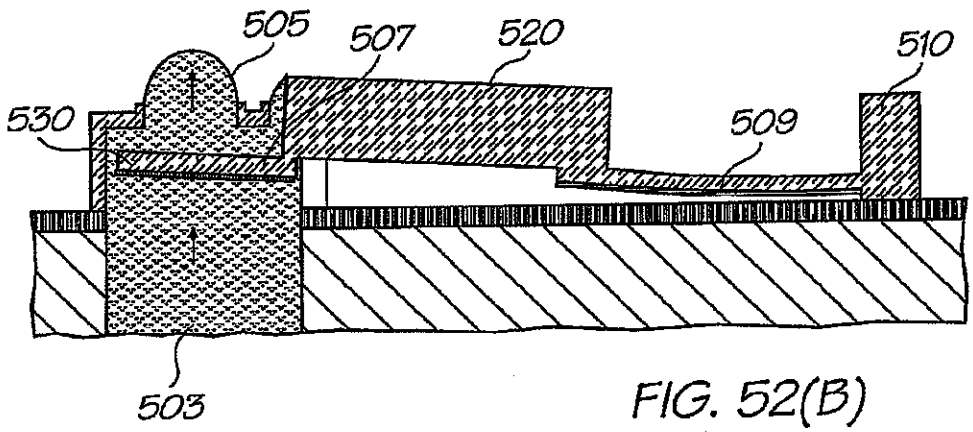


FIG. 52(B)

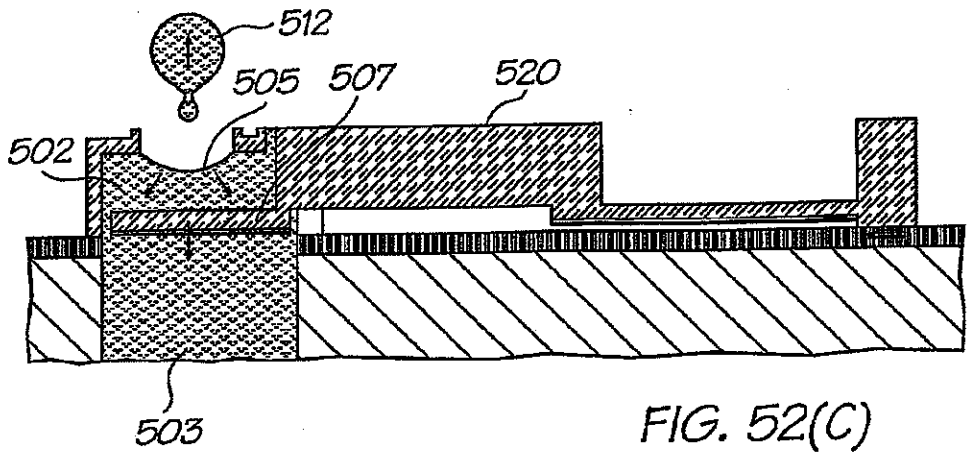


FIG. 52(C)

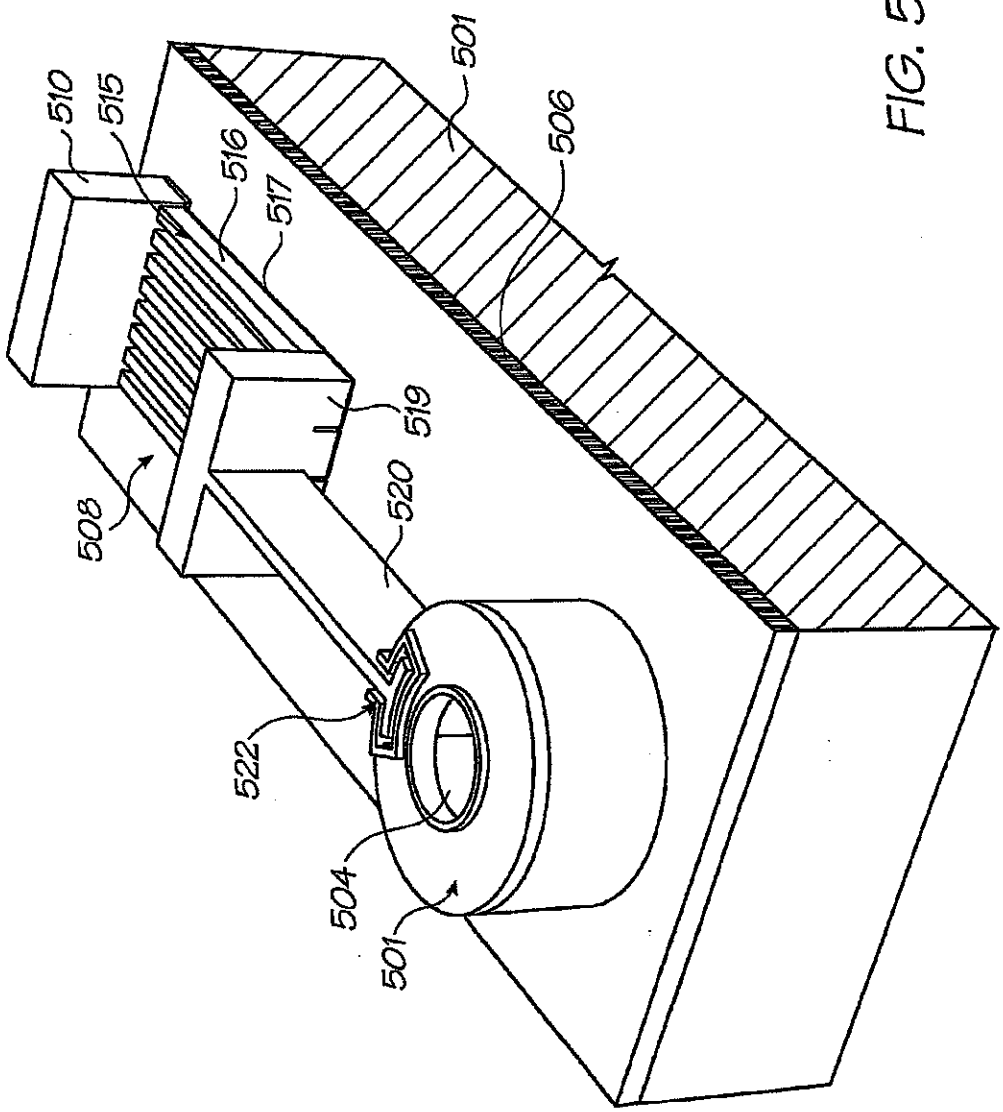


FIG. 53

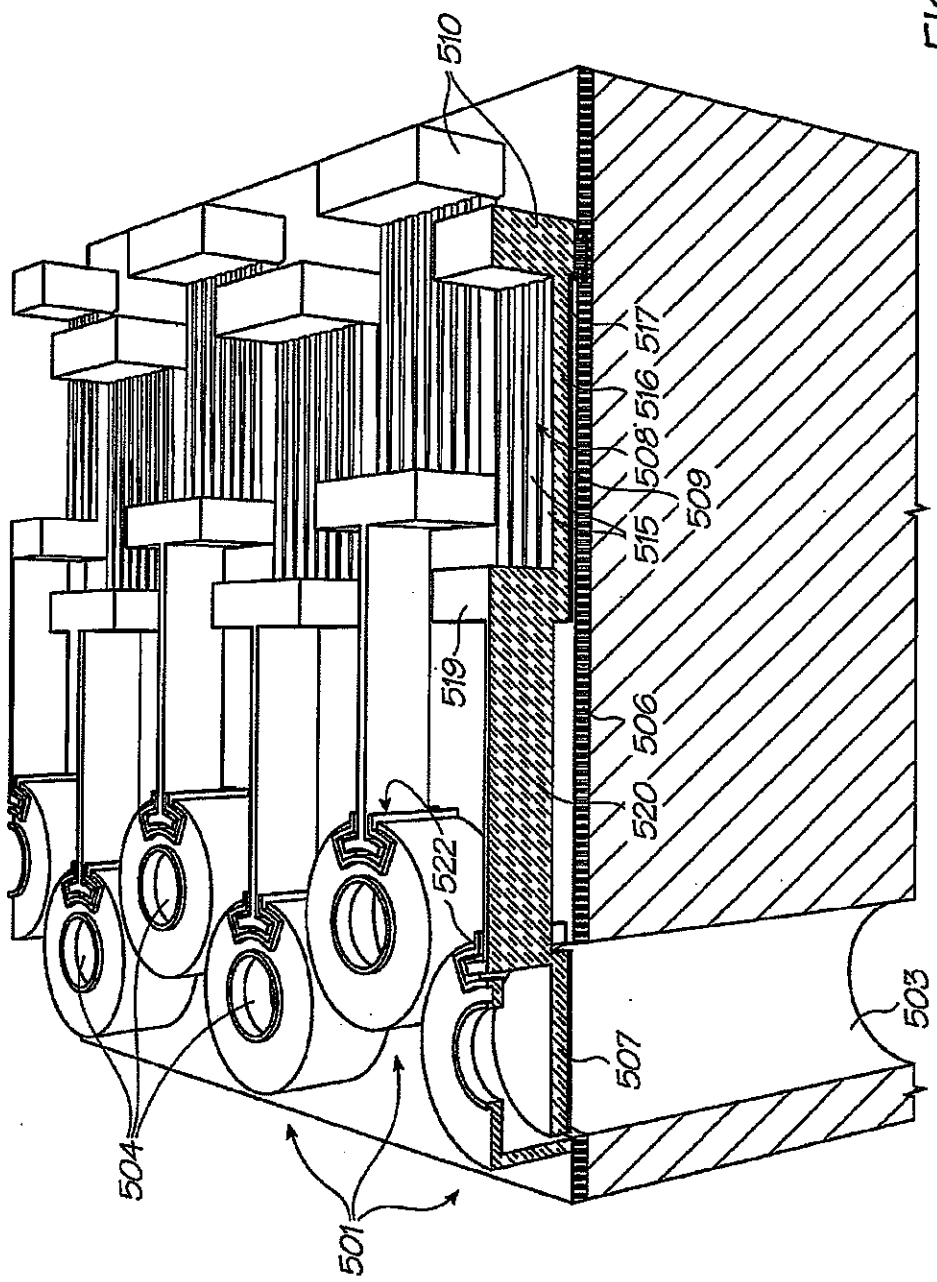


FIG. 54

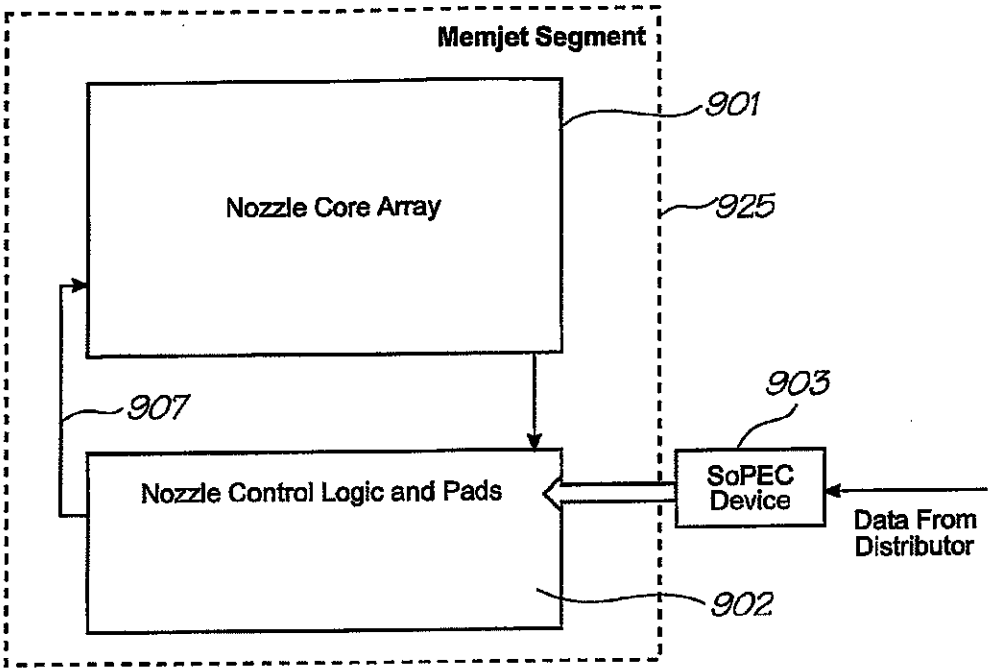

Memjet Segment
901
Nozzle Core Array
925
903
907
SoPEC Device
Nozzle Control Logic and Pads
Data From Distributor
902

FIG. 55

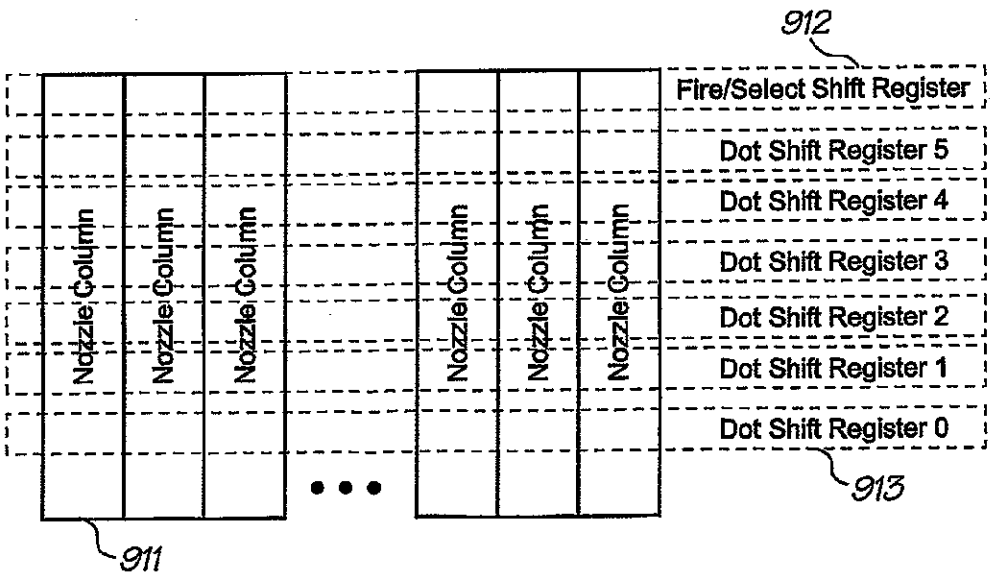

912
Fire/Select Shift Register
Dot Shift Register 5
Dot Shift Register 4
Dot Shift Register 3
Dot Shift Register 2
Dot Shift Register 1
Dot Shift Register 0
913
Nozzle Column
911

FIG. 56

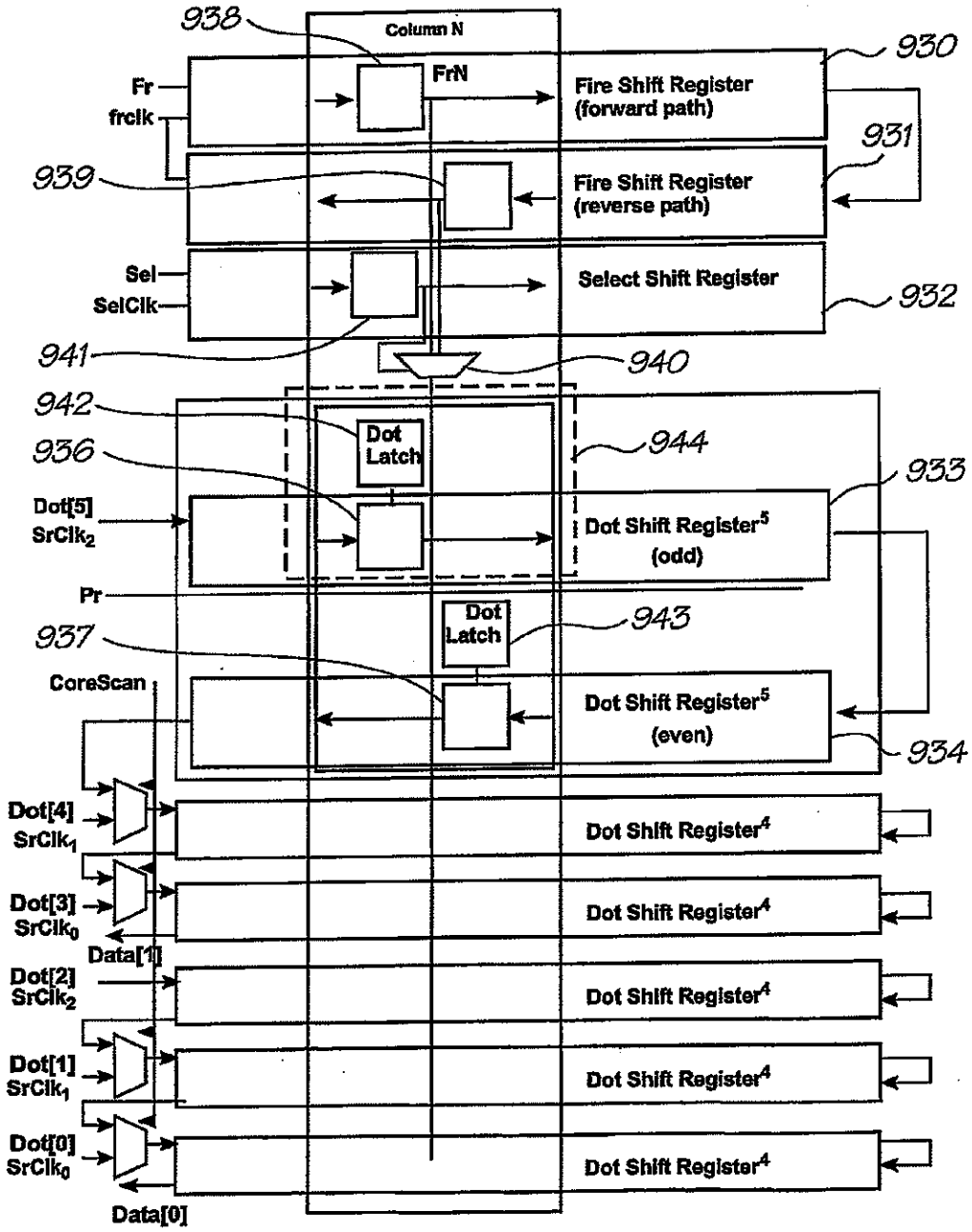

938
Column N
930
Fr
frclk
FrN
Fire Shift Register
(forward path)
931
939
Fire Shift Register
(reverse path)
Sel
SelClk
Select Shift Register
932
941
940
942
Dot
Latch
944
936
933
Dot[5]
SrClk2
Dot Shift Register5
(odd)
Pr
Dot
Latch
943
937
CoreScan
Dot Shift Register5
(even)
934
Dot[4]
SrClk1
Dot Shift Register4
Dot[3]
SrClk0
Data[1]
Dot Shift Register4
Dot[2]
SrClk2
Dot Shift Register4
Dot[1]
SrClk1
Dot Shift Register4
Dot[0]
SrClk0
Dot Shift Register4
Data[0]

FIG. 57

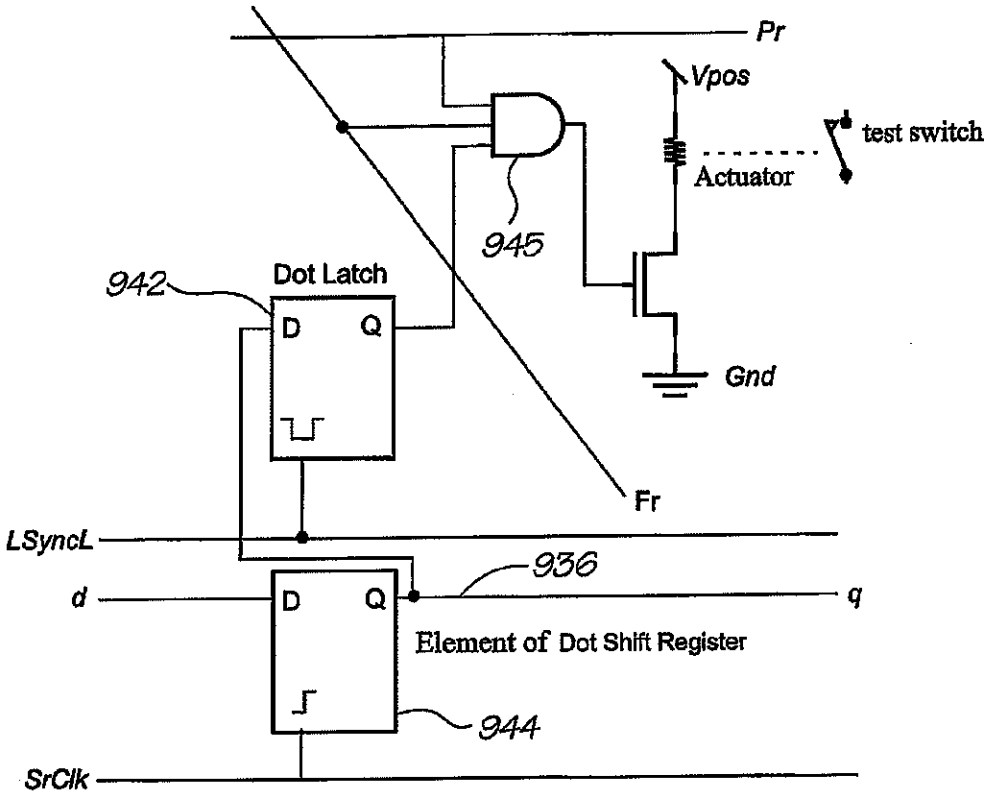

Pr
Vpos
test switch
Actuator
945
942
Dot Latch
D
Q
Gnd
Fr
LSyncL
936
d
D
Q
q
Element of Dot Shift Register
944
SrClk

FIG. 58