What Is Claimed Is:

1. A semiconductor device comprising:

a peripheral circuit region on a first substrate and including circuit devices;

a memory cell region on a second substrate overlaid on the first substrate, wherein the memory cell region includes gate electrodes spaced apart from each other in a first direction that is perpendicular to an upper surface of the second substrate, wherein the memory cell region includes channel structures that penetrate the gate electrodes and extend vertically to the second substrate, and wherein the channel structures include a channel layer; and

a through-wiring region that electrically connects the memory cell region and the peripheral circuit region,

wherein the through-wiring region includes:

through-contact plugs that extend in the first direction to penetrate the memory cell region, wherein the through-contact plugs electrically connect the memory cell region and the circuit devices;

an insulating region that surrounds the through-contact plugs, wherein the insulating region includes first insulating layers and second insulating layers that are alternately stacked; and

dummy channel structures that penetrate the first insulating layers and the second insulating layers,

wherein the dummy channel structures include a dummy channel layer, and

wherein the dummy channel structures are arranged in rows and columns such that at least one dummy channel structure is positioned between the through-contact plugs adjacent to each other.

2. The semiconductor device of claim 1, wherein in the through-wiring region, a number of the through-contact plugs equals a number of the dummy channel structures.

3. The semiconductor device of claim 1 or claim 2, wherein at least one of the dummy channel structures comprises a structure that corresponds to a structure of the channel structures.

4. The semiconductor device of any one of claims 1 to 3, wherein each of the channel structures comprises a gate dielectric layer, the channel layer on the gate dielectric layer, and a channel insulating layer on the channel layer.

5. The semiconductor device of any one of claims 1 to 4, wherein each of the dummy channel structures has a maximum diameter between about 70 nm to about 130 nm, and wherein each of the through-contact plugs has a maximum diameter between about 250 nm to about 350 nm.

6. The semiconductor device of any one of claims 1 to 5, wherein each of the channel structures comprises a first channel structure and a second channel structure stacked in the first direction, and

wherein each of the dummy channel structures comprises a first dummy channel structure and a second dummy channel structure stacked in the first direction.

7. The semiconductor device of claim 6, wherein at least portions of the first dummy channel structures and the second dummy channel structures are spaced apart from each other in the first direction and are disconnected from each other.

8. The semiconductor device of claim 6, wherein at least portions of the first dummy channel structures and the second dummy channel structures are shifted from each other in a second direction that is perpendicular to the first direction.

9. The semiconductor device of any one of claims 6 to 8, wherein at least a first of the first dummy channel structures has a structure different from a structure of a second of the first channel structures.

10. The semiconductor device of any one of claims 1 to 7, wherein the memory cell region further comprises separation regions that penetrate the gate electrodes and that extend in a second direction that is perpendicular to the first direction, and wherein the separation regions are spaced apart from the through-wiring region.

11. The semiconductor device of claim 10, wherein the through-wiring region is centered between two adjacent separation regions.

12. The semiconductor device of any one of claims 1 to 11, wherein the memory cell region further comprises interlayer insulating layers alternately arranged with the gate electrodes, and

wherein the first insulating layers are at the same height level as the interlayer insulating layers, and the second insulating layers are at the same height level as the gate electrodes.

13. A semiconductor device comprising:

a peripheral circuit region provided on a first substrate and including circuit devices;

a memory cell region provided on a second substrate overlaid on the first substrate, wherein the memory cell region includes a stacked structure comprising spaced-apart gate electrodes, above the second substrate, and wherein the memory cell region includes channel structures that extend vertically to the second substrate and that penetrate the gate electrodes, and wherein the channel structures include a channel layer; and

a through-wiring region including through-contact plugs that extend vertically and that electrically connect the memory cell region and the peripheral circuit region to each other,

wherein the through-wiring region includes an insulating region that surrounds the through-contact plugs,

wherein the through-wiring region further includes dummy channel structures that are regularly arranged throughout the through-wiring region and that include a dummy channel layer,

wherein the insulating region includes first insulating layer and second insulating layers that are alternately stacked, and

wherein the dummy channel structures penetrate the first insulating layers and the second insulating layers.

14. The semiconductor device of claim 13, wherein at least portions of the dummy channel structures are in the through-contact plugs.

15. The semiconductor device of claim 14, wherein the dummy channel structures in the through-contact plugs have a structure different from a structure of the channel structures.

16. The semiconductor device of any one of claims 13 to 15, wherein each of the channel structures comprises a gate dielectric layer, the channel layer on the gate dielectric layer, and a channel insulating layer on the channel layer, and

wherein each of the dummy channel structures in the through-contact plugs comprises the dummy channel layer.

17. The semiconductor device of claim 13, wherein the dummy channel structures are between a respective pair of the through-contact plugs adjacent to each other in at least one direction.

18. A semiconductor device comprising:

a first substrate;

circuit devices on the first substrate;

a second substrate on the circuit devices;

gate electrodes spaced apart from each other in a first direction;

channel structures that penetrate the gate electrodes and extend vertically from the second substrate, wherein the channel structures include a channel layer;

separation regions that extend in a second direction perpendicular to the first direction, wherein the separation regions extend through the gate electrodes and are spaced apart from each other and parallel to each other; and

a through-wiring region located between adjacent separation regions and spaced apart from the adjacent separation regions,

wherein the through-wiring region includes:

through-contact plugs;

an insulating region that surrounds the through-contact plugs; and

dummy channel structures that include a dummy channel layer and that are provided in at least the same number as a number of the through-contact plugs,

wherein a lower end of each of the through-contact plugs is at a lower level than a lowermost gate electrode among the gate electrodes,

wherein an upper end of each of the through-contact plugs is at a higher level than an uppermost gate electrode among the gate electrodes,

wherein the insulating region includes first insulating layer and second insulating layers that are alternately stacked, and

wherein the dummy channel structures penetrate the first insulating layers and the second insulating layers.

19. The semiconductor device of claim 18, wherein the through-contact plugs and the dummy channel structures are arranged in the same pattern as each other.

20. The semiconductor device of claim 18 or 19, wherein the dummy channel structures overlap the through-contact plugs.