CLAIMS

What is claimed is:

1. A diode, comprising:

a semiconductor layer;

a phase change material layer;

wherein the semiconductor layer and the phase change material layer have different energy bandgaps and different carrier concentrations such that an isotype heterojunction is formed at a boundary interface between the semiconductor layer and the phase change material layer.

2. The diode of claim 1,

wherein the isotype heterojunction is a P-p heterojunction.

3. The diode of claim 2,

wherein the semiconductor layer is a p-type semiconductor material and the phase change material layer is a p-type phase change material.

4. The diode of claim 1,

wherein the isotype heterojunction is a N-n heterojunction.

5. The diode of claim 4,

wherein the semiconductor layer is a n-type semiconductor material and the phase change material layer is a n-type phase change material.

6. The diode of any one of claims 1 to 5,

wherein the phase change material layer comprises chalcogenide alloy.

7. The diode of claim 6,

wherein the phase change material layer has an energy bandgap less than 5 eV.

8. The diode of claim 6 or 7,

wherein the phase change material layer has a carrier concentration of about 10^{20} cm^{-3} or less.

9. The diode of any one of claims 1 to 8,

wherein the phase change material layer comprises a phase change magnetic material.

10. The diode of claim 9,

wherein the phase change magnetic material is a compound consisting of a phase change material component and a ferromagnetic material component, wherein the phase change magnetic material exhibits both magnetic properties and phase change effects.

11. The diode of any one of claims 1 to 10,

wherein the semiconductor layer comprises a semiconductor material.

12. The diode of claim 11,

wherein the semiconductor material comprises any one of a group consisting of group IV elements, IV-IV compounds, III-V compounds, II-VI compounds, IV-VI compounds and organic semiconductors.

13. The diode of claim 11,

wherein the semiconductor layer comprises an energy bandgap larger than 0.1 eV.

14. The diode of claim 11,

wherein the semiconductor layer has a carrier concentration larger than 10^{10} cm^{-3}.

15. The diode of any one of claims 1 to 14,

wherein the diode has a leakage current of about 10^{-6}A to about 10^{-10}A.

16. The diode of any one of claims 1 to 14,

wherein the diode has a leakage current less than 10^{-6}A.

17. The diode of any one of claims 1 to 16,

wherein the diode has a reverse breakdown voltage larger than 3 V.

18. A memory device comprising a diode of any one of claims 1 to 17.

19. The memory device of claim 18, further comprising:

a controller configured to provide a plurality of operation cycles for the diode, wherein each operation cycle comprises a set mode and a reset mode.

20. The memory device of claim 18 or 19,

wherein the diode comprises a high resistance state and a low resistance state, and is configured to store data by changing between the high resistance state and the low resistance state during each operation cycle of the memory device.

21. The memory device of claim 20,

wherein the diode changes from the low resistance state to the high resistance state when the phase change material layer changes from a crystalline to an amorphous state, and wherein the diode changes from the high resistance state to the low resistance state when the phase change material layer changes from the amorphous state to the crystalline state.

22. The memory device of claim 21,

wherein the diode is at the high resistance state when the phase change material layer is at the amorphous state and is at the low resistance state when the phase change material layer is at the crystalline state.

23. The memory device of any one of claims 20 to 22,

wherein in the reset mode of the memory device, the controller is configured to pass a current equal to a reset current of the memory device through the isotype heterojunction of the diode to change the diode from the low resistance state to the high resistance state.

24. The memory device of any one of claims 20 to 23,

wherein in the set mode of the memory device, the controller is configured to pass a current equal to a set current of the memory device through the isotype heterojunction of the diode to change the diode from the high resistance state to the low resistance state.

25. The memory device of any one of claims 19 to 24,

wherein the controller is configured such that each operation cycle further comprises a read mode, and wherein in the read mode of the memory device, the controller is configured to apply a read current or a read voltage of the memory device at the isotype heterojunction.

26. The memory device of claim 25,

wherein in the read mode of the memory device, an electrical parameter measured at the low resistance state of the diode is read as a first data value.

27. The memory device of claim 26,

wherein in the read mode of the memory device, an electrical parameter measured at the high resistance state of the diode is read as a second data value different from the first data value.

28. The memory device of claims 26 or 27,

wherein the electrical parameter comprises any one of voltage, current and resistance.

29. The memory device of any one of claims 20 to 28,

wherein the controller is configured such that the plurality of operation cycles comprises at least 10^4 cycles.

30. The memory device of any one of claims 20 to 28,

wherein the controller is configured such that the plurality of operation cycles comprises at least 10^{10} cycles.

31. The memory device of any one of claims 20 to 28,

wherein the controller is configured to provide a bias voltage to the diode.

32. The memory device of claim 31,

wherein the bias voltage ranges from about 0 V to about 5 V.

33. The memory device of any one of claims 20 to 31,

wherein the controller is configured to provide a read and write current or a read and write voltage having a pulse width of about 1 ms or smaller to the diode.

CLAIMS

1. A diode, comprising:

a semiconductor layer;

a phase change material layer;

wherein the semiconductor layer and the phase change material layer have different energy bandgaps and different carrier concentrations such that an isotype heterojunction is formed at a boundary interface between the semiconductor layer and the phase change material layer; wherein the phase change material layer comprises a phase change magnetic material that includes a phase change material component and a ferromagnetic material component.

2. The diode of claim 1,

wherein the isotype heterojunction is a P-p heterojunction.

3. The diode of claim 2,

wherein the semiconductor layer is a p-type semiconductor material and the phase change material layer comprises a p-type phase change material.

4. The diode of claim 1,

wherein the isotype heterojunction is a N-n heterojunction.

5. The diode of claim 4,

wherein the semiconductor layer is a n-type semiconductor material and the phase change material layer comprises a n-type phase change material.

6. The diode of claim 1,

wherein the diode has a leakage current less than 10^{-6}A.

7. A memory device, comprising:

a diode, comprising:

a semiconductor layer;

a phase change material layer;

wherein the semiconductor layer and the phase change material layer have different energy bandgaps and different carrier concentrations such that an isotype heterojunction is formed at a boundary interface between the semiconductor layer and the phase change material layer; wherein the phase change material layer comprises a phase change magnetic material that includes a phase change material component and a ferromagnetic material component.

8. The memory device of claim 7, further comprising:

a controller configured to provide a plurality of operation cycles for the diode, wherein each operation cycle comprises a set mode and a reset mode.

9. The memory device of claim 7, wherein the diode comprises a high resistance state and a low resistance state, and is configured to store data by changing between the

high resistance state and the low resistance state during each operation cycle of the memory device.

10. The memory device of claim 9, wherein the diode changes from the low resistance state to the high resistance state when the phase change material layer changes from a crystalline state to an amorphous state, and wherein the diode changes from the high resistance state to the low resistance state when the phase change material layer changes from the amorphous state to the crystalline state.

11. The memory device of claim 10, wherein the diode is at the high resistance state when the phase change material layer is at the amorphous state and is at the low resistance state when the phase change material layer is at the crystalline state.

12. The memory device of claim 9, wherein in the reset mode of the memory device, the controller is configured to pass a current equal to a reset current of the memory device through the isotype heterojunction of the diode to change the diode from the low resistance state to the high resistance state.

13. The memory device of claim 9, wherein in the set mode of the memory device, the controller is configured to pass a current equal to a set current of the memory device through the isotype heterojunction of the diode to change the diode from the high resistance state to the low resistance state.

14. The memory device of claim 8, wherein the controller is configured such that each operation cycle further comprises a read mode, and wherein in the read mode of the memory device, the controller is configured to apply a read current or a read voltage of the memory device at the isotype heterojunction.

15. The memory device of claim 14, wherein in the read mode of the memory device, an electrical parameter measured at the low resistance state of the diode is read as a first data value.

16. The memory device of claim 15, wherein in the read mode of the memory device, an electrical parameter measured at the high resistance state of the diode is read as a second data value different from the first data value.

17. The memory device of claim 15, wherein the electrical parameter comprises any one of voltage, current and resistance.

18. The memory device of claim 8, wherein the controller is configured such that the plurality of operation cycles comprises at least 10^4 cycles.

19. The memory device of claim 8, wherein the controller is configured such that the plurality of operation cycles comprises at least 10^{10} cycles.