WHAT IS CLAIMED IS:

1. A three-dimensional memory, comprising:

a stack structure comprising gate layers and dielectric layers disposed alternately; the stack structure comprising a step structure comprising a plurality of staircase structures disposed in a first direction and having different heights in a second direction; the staircase structure comprising a plurality of steps; and the first direction being perpendicular to the second direction;

a plurality of first stops disposed in the first direction and located on the plurality of steps of at least one of the staircase structures, with each of the plurality of first stops disposed on the corresponding step of the plurality of steps;

a protection layer covering the step structure and the first stops;

a plurality of contact posts each extending through the protection layer and the first stop and being connected with the gate layer in the step corresponding to the first stop;

isolation structures extending in the first direction and through the stack structure; the isolation structures dividing the stack structure into a plurality of memory blocks, with each memory block comprising the step structure; and

a plurality of second stops disposed in the first direction and located on the plurality of steps of other staircase structures among the plurality of staircase structures other than the staircase structures on which the first stops are disposed;

wherein the memory block comprises a plurality of gate line isolation structures each extending through the second stop and the stack structure and extending in the first direction, and each gate line isolation structure comprises a plurality of sub-isolation structures disposed at intervals.

2. The three-dimensional memory of claim 1, wherein the staircase structures where the first stops are located are disposed at intervals with the isolation structures.

3. The three-dimensional memory of claim 1 or claim 2, wherein, in the second direction, the memory block comprises a first staircase structure, a second staircase structure, and a third staircase structure, with the first stops disposed on the plurality of steps of the second staircase structure.

4. The three-dimensional memory of claim 1 or claim 2, wherein, in the second direction, the memory block comprises a first staircase structure and a second staircase structure, the first staircase structure being disposed at intervals with the isolation structure, and the first stops being disposed on the plurality of steps of the first staircase structure.

5. The three-dimensional memory of claim 1 or claim 2, wherein each memory block further comprises a sidewall;

the isolation structures comprise a first isolation structure and a second isolation structure;

in the second direction, the first isolation structure is located between two adjacent sidewalls in different memory blocks; the second isolation structure is located between two adjacent step structures; and in the second direction, the step structures in two memory blocks adjacent to the second isolation structure are disposed symmetrically.

6. The three-dimensional memory of claim 5, wherein, in the second direction, and along a direction from the first isolation structure toward the second isolation structure, the plurality of staircase structures in the memory block have decreasing heights.

7. The three-dimensional memory of claim 5, wherein, in the second direction, two staircase structures adjacent to both sides of the second isolation structure have same heights.

8. The three-dimensional memory of claim 1 or claim 2, wherein the protection layer further covers the second stops and at least a part of the protection layer is located between the second stop and the step adjacent to the second stop.

9. The three-dimensional memory of claim 1 or claim 8, wherein a material for the second stop is same as a material for the gate layer.

10. The three-dimensional memory of claim 1, wherein a material for the first stop comprises silicon nitride.

11. The three-dimensional memory of claim 1, wherein, in a third direction, a thickness of the first stop is same as a thickness of the gate layer of a previous step; and the previous step is adjacent to and higher than the step corresponding to the first stop; and

wherein the third direction is perpendicular to the first direction and the second direction.

12. The three-dimensional memory of claim 1 or claim 8, wherein the first stop comprises carbon-doped silicon nitride.

13. The three-dimensional memory of claim 12, wherein a material for the second stop is same as the material for the first stop.

14. The three-dimensional memory of claim 1 or claim 8, wherein a thickness of the second stop is greater than a thickness of the gate layer, and the second stop comprises an insulating material.

15. The three-dimensional memory of claim 1, wherein at least a part of the protection layer is located between the first stop and the step adjacent to the first stop.

16. The three-dimensional memory of claim 1, further comprising a separating layer covering the step structures and located between the step structure and the first stop.

17. A method of fabricating a three-dimensional memory, comprising:

forming an initial stack structure comprising sacrificial layers and dielectric layers disposed alternately; the initial stack structure comprising a step structure comprising a plurality of staircase structures disposed in a first direction and having different heights in a second direction; the staircase structure comprising a plurality of steps; and the first direction being perpendicular to the second direction;

forming a plurality of first stops on the plurality of steps of at least one of the staircase structures; the plurality of first stops being disposed in the first direction, with each of the plurality of first stops disposed on one of the plurality of steps;

forming a protection layer covering the step structures and the first stops, at least a part of the protection layer being located between the first stop and the step adjacent to the first stop;

replacing the sacrificial layers with gate layers to form a stack structure;

forming a plurality of contact posts each extending through the protection layer and the first stop and being electrically connected with the gate layer in the step corresponding to the first stop;

forming a plurality of second stops on the plurality of steps of other staircase structures among the plurality of staircase structures other than the staircase structures on which the first stops are disposed; each second stop is disposed on one step;

forming a plurality of third slits extending in the first direction; the third slit extending through the second stop and the initial stack structure; wherein each of the third slits comprises a plurality of third sub slits separated from each other in the first direction; and

forming gate line isolation structures in the third slits.

18. The method of claim 17, wherein the forming the plurality of first stops on the plurality of steps of at least one of the staircase structures comprises:

etching the uppermost sacrificial layer and dielectric layer of each step to form the plurality of first stops.

19. The method of claim 17, further comprising:

forming a first slit extending in the first direction and through the initial stack structure; the first slit dividing the initial stack structure into a plurality of initial memory blocks, each of which comprises the step structure; and

forming an isolation structure in the first slit.

20. A memory system, comprising:

a controller; and

a three-dimensional memory, comprising:

a stack structure comprising gate layers and dielectric layers disposed alternately; the stack structure comprising a step structure comprising a plurality of staircase structures disposed in a first direction and having different heights in a second direction; the staircase structure comprising a plurality of steps; and the first direction being perpendicular to the second direction;

a plurality of first stops disposed in the first direction and located on the plurality of steps of at least one of the staircase structures, with each of the plurality of first stops disposed on the corresponding step of the plurality of steps;

a protection layer covering the step structure and the first stops;

a plurality of contact posts, each of which extends through the protection layer and the first stop and is connected with the gate layer in the step corresponding to the first stop;

isolation structures extending in the first direction and through the stack structure; the isolation structures dividing the stack structure into a plurality of memory blocks, with each memory block comprising the step structure; and

a plurality of second stops disposed in the first direction and located on the plurality of steps of other staircase structures among the plurality of staircase structures other than the staircase structures on which the first stops are disposed;

wherein the memory block comprises a plurality of gate line isolation structures each extending through the second stop and the stack structure and extending in the first direction, and each gate line isolation structure comprises a plurality of sub-isolation structures disposed at intervals; and

wherein the controller is coupled to the three-dimensional memory and configured to control the three-dimensional memory to store data.