ARCHITECTURE FOR GENERAL PURPOSE PROGRAMMABLE SEMICONDUCTOR PROCESSING SYSTEM AND METHODS THEREFOR

BACKGROUND OF THE INVENTION

[0001] The present invention relates in general to semi-conductor manufacturing technologies and in particular to methods and apparatus of optimizing a set of operations in a semi-conductor capital equipment processing system.

[0002] Semi-conductor fabrication facilities often cost billions of dollars to design and operate. Optimizing throughput and decreasing costs are therefore critical for profitability. Capital equipment processing systems within these facilities, however, often require significant human manual intervention creating the potential for process variances or even outright operation mistakes.

[0003] Most semi-conductor capital equipment processing systems are normally controlled by sophisticated computers comprising operating software programs, wherein users via a interface are provided the ability to send requests to the equipment and receive output information from the equipment. These procedure steps for the most part are executed manually. In a typical operating environment, the user manually configures parameters for the manufacturing process (e.g., voltage, gas flow mix, gas flow rate, pressure, etc.) and then manually initiates start execution. The processing system examines its state by either evaluating signals from one or more sensing devices (e.g., position encoders, temperature and pressure sensors, flow rate indicators, etc.) or by requesting that the operator input information (e.g. the results of spectra optical emission, gas proportion mix, etc.). Test product is initially run through the system, to insure that the process is within acceptable parameters, after which the production run is started. During this process, the operator is usually expected to follow printed procedures and physically write down system measurements at appropriate time.

[0004] However, because of differences in training, experience, or attitude, different operators can implement the same test differently on the same machine. Furthermore, information entered in the process data notebooks may be incomplete or incorrect, presenting problems for process engineers who are tasked to insure that the fabrication process is optimally configured and manufacturing yields are maintained at an acceptable level.

[0005] Process variance is further compounded when multiple versions of the same processing system are concurrently used in the manufacture of the same product. Since an otherwise identical piece of fabrication equipment may be installed at a different time, or is used to a different degree, its maintenance cycle does not necessarily match that of the others, potentially causing chamber-to-chamber process variation.

[0006] Furthermore, there is often a need to safely and quickly modify the operation of a processing system at the customer site. In general, changes in semi-conductor fabrication equipment procedures are often difficult to implement, especially in the case of multiple equipment units. This lack of process flexibility can create substantial inefficiency and hence significantly increase production costs. For example, a customer may want the processing equipment to perform a new testing procedure because of some newly discovered process variance. In order to implement this new procedure, the vendor must first create or modify an existing written procedure and send a field engineer to the customer site to perform training, then monitor for changes in tool performance for a period of time to insure proper functionality. This process can take several weeks, potentially costing several hundreds of thousands of dollars.

[0007] In view of the foregoing, there is desired an architecture for a general purpose programmable semi-conductor processing system.

SUMMARY OF THE INVENTION

[0008] The invention relates, in one embodiment, to a method of optimizing a set of steps in a semi-conductor processing system comprising a software control program, wherein the semi-conductor processing system includes a first function, a second function, and a third function, and further includes a memory for storing a set of variables, and wherein the set of steps further includes a first step, a second step, and a third step. The invention includes generating the first step on an editor application, wherein the first function is added to the first step, and if required, a first set of user input instructions is added. The invention also includes generating the second step on the editor application, wherein the second function is added to the second step, and if required, a second set of user input instructions is added; and generating the third step on the editor application, wherein the third function is added to the third step, and if

required, a third set of user input instructions is added. The invention further includes placing the first step, the second step, and the third step in a proper order; transferring the set of steps to the semi-conductor processing system; executing the set of steps; storing a set of results in the set of variables; and, if required, generating a report from the set of variables.

[0009] The invention relates, in another embodiment, to an apparatus for optimizing a set of steps in a semi-conductor processing system comprising a software control program, wherein the semi-conductor processing system includes a first function, a second function, and a third function, and further includes a memory for storing a set of variables, and wherein the set of steps further includes a first step, a second step, and a third step. The invention includes a means of generating the first step on a editor application, wherein the first function is added to the first step, and if required, a first set of user input instructions is added. The invention also includes a means of generating the second step on the editor application, wherein the second function is added to the second step, and if required, a second set of user input instructions is added; and a means of generating the third step on the editor application, wherein the third function is added to the third step, and if required, a third set of user input instructions is added. The invention further includes a means of placing the first step, the second step, and the third step in a proper order; a means of transferring the set of steps to the semi-conductor processing system; a means of executing the set of steps; a means of storing a set of results in the set of variables; and, if required, a means of generating a report from the set of variables. These and other features of the present invention will be described in more detail below in the detailed description of the invention and in conjunction with the following figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

[0011] FIG. 1 depicts a simplified diagram of a process for creating macros, according to one embodiment of the invention;

[0012] FIG. 2 depicts a simplified set of macros for controlling a semi-conductor processing system, according to one embodiment of the invention;

[0013] FIG. 3 depicts a simplified report of the results of the simplified set of macros for controlling a semi-conductor processing system, according to one embodiment of the invention;

[0014] FIG. 4 depicts a simplified flowchart showing the steps for creating a macro for controlling a semi-conductor processing system, according to one embodiment of the invention; and,

[0015] FIGS. 5A-B depict a graphical display for a semi-conductor processing system, according to one embodiment of the invention.

[0016] FIGs. 6A-6B depict the macro editor, according to one embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] The present invention will now be described in detail with reference to a few preferred embodiments thereof as illustrated in the accompanying drawings. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process steps and/or structures have not been described in detail in order to not unnecessarily obscure the present invention.

[0018] In accordance with one embodiment of the present invention, a macro engine is advantageously employed to extend and enhance the capabilities of a semi-conductor processing system. That is, a set of control instructions or steps, called a macro, can be created to control the functions of the semi-conductor processing system and to further store process information in the memory in order to generate a report. Furthermore, these instructions can be created and modified with a macro editor, and subsequently stored in a file.

[0019] In one embodiment, the set of macros comprise a manufacturing procedure that was previously programmed in a non-macro fashion, such as hardware startup qualification. In another embodiment, the set of macros comprise manufacturing

procedures that were previously physically printed. In yet another embodiment, the set of macros allows the user to enter system measurements directly into the semi-conductor processing system. In yet another embodiment, the set of macros substantially monitors operator actions and subsequently creates a log of semi-conductor processing system events, actions, errors, and problems. In yet another embodiment, this log can be electronically retrieved and remotely analyzed. In another embodiment, a user interface is employed to allow the operator to interact with the set of macros. In another embodiment, the semi-conductor processing system can be fully automated, and run without user interaction. In another embodiment, the set of macros can be standardized on all substantially equivalent semi-conductor procession systems, substantially reducing chamber-to-chamber performance variations. In still another embodiment, the set of macros can be executed from a remote host. In another embodiment, the set of macros can be obfuscated or encrypted.

[0020] Referring now to FIG. 1, a simplified diagram of a process for creating macros is shown, according to one embodiment of the invention. Initially, a library of macro procedures 102 is created for use in a semi-conductor processing system. For example, in a plasma processing system, this library can consist of tool health checks such as daily and weekly preventative maintenance (PM) qualifications, wet clean and recovery, hardware start-up qualification, chamber matching, and troubleshooting.

[0021] This library may then be uploaded to the software control program 106 of a semi-conductor processing system. In one embodiment, the semi-conductor processing system comprises a macro engine 108 that interprets macro procedures. In another embodiment, the semi-conductor processing system comprises a macro engine 108 that executes macro procedures. Each of these macro procedures can then be performed in proper sequence by macro engine 108. During operation, the semi-conductor processing system, in turn, examines its state and compares the result to established specifications, or requests that the operator input information. Macro engine 108 may further compare tool data with macro specifications, and may generate and locally store 110 an electronic summary report, a tool performance tracking report, and/or raw data in datalog format. In one embodiment, each report may be in a web-based output format, such as XML or HTML.

[0022] Furthermore, these reports and raw data can be collected from multiple semi-conductor processing systems and subsequently analyzed by offline or online analytical software. This information may also be imported into a service notification 124 that may automatically send an alert to the appropriate person, should a problem arise. In addition, each semi-conductor processing system's electronic summary report 125 may be aggregated in a factory hosted and may be remotely accessed with remote diagnostics 126. Through a host executable program 128, this information may be re-incorporated into the creation and modification of macro procedure library 102.

[0023] Referring now to FIG. 2, a set of macros is shown for controlling a semi-conductor processing system. Although in this example, the set of macros is executing within a Lam software macro engine, the present invention can be applied to other types of semi-conductor processing equipment and software. This macro, entitled dailycheck, is composed of multiple steps that may be executed in sequential order. Furthermore, each step can further require the operator to begin its execution (as shown at line 9 "startRequired: false"), and to continue on to the next step in the case of the previous step's failure (as shown at line 8 "continueIfFailed: true").

[0024] The first step (as shown on lines 1-11) processes the chamber state offline in order to prevent waferflow into the PM after this macro step. This ensures that users do not inadvertently process unintended wafers during the macro sequence. The second step (as shown on lines 12-36), records the current values stored in the software AI parameters on the PM/Diagnose/System Information user interface window. This information provides a snapshot of the tool state. The third step (as shown on lines 37-59) monitors key tool performance data and alert users when the tool has drifted out of control. It is the start of the Daily Process Module Qual macro sequence.

[0025] The fourth step (as shown on lines 60-122) checks the current values stored in the software AI parameters on the PM/Diagnose/IO/System Heater Channels user interface window and other temperature related software parameters vs. their recommended setpoints. The fifth step (as shown on lines 123-137) executes a chamber pumpdown. The sixth step (as shown on lines 138-147) idles the chamber. The seventh step (as shown on lines 148-169) records the current values stored in the software AI parameters on the PM/Diagnose/IO/Manometer Raw Reading user interface window and

other pressure related software parameters. The eighth step (as shown on lines 170-183) executes a chamber leakrate check. The ninth step (as shown on lines 184-197) executes a chamber pumpdown. The tenth step (as shown on lines 198-235) executes the VCI No-Plasma V-Probe test with spec checking.

[0026] The eleventh step (as shown on lines 236-249) executes a chamber pumpdown. The twelfth step (as shown on lines 250-288) executes the one point gas calibration for process gases at 100% of MFC full scale. The thirteenth step (as shown on lines 289-327) executes the one point gas calibration for process gases at 30% of MFC full scale. The fourteenth step (as shown on lines 328-366) executes the one point gas calibration for process gases at 10% of MFC full scale. And finally, the fifteenth step (as shown on lines 367-377) processes chamber state online to allow waferflow into the PM after this macro step. This ensures that users can routinely process wafers after the completion of the macro sequence.

[0027] Referring now to FIG. 3, a simplified report is shown of the results of the set of macros for controlling a semi-conductor processing system, as described in FIG. 2, according to one embodiment of the invention. Each macro step in FIG. 2 may have a corresponding report section in FIG. 3. Initially, a status summary of all the steps is shown. For example, step 4 (Chamber Temp Check) and step 14 (Gas Cal One Point Various) have failed, while the remaining steps have passed. In one embodiment, this report is generated in a spreadsheet format, such as Microsoft Excel.

[0028] Referring now to FIG. 4, a simplified flowchart showing the steps for creating a macro for controlling a semi-conductor processing system is shown. Initially, a non-macro procedure is created or revised at step 402. If a macro version of the procedure is desired at step 406, the macro is generated with the macro editor at step 408. At this point, both the macro and non-macro procedures are tested and optimized on the semi-conductor processing system, at step 410. The procedure is then finalized and approved by management at step 412. The both the macro and non-macro procedures may then be submitted to a document control system at step 414, after which they would be available for use on the semi-conductor processing system at step 418.

[0029] Referring now to FIGS. 5A-B, a graphical display for a semi-conductor processing system is shown, according to one embodiment of the invention. Although in

this example, the set of macros is executing within a Lam software macro engine, the present invention can be applied to other types of semi-conductor processing equipment and software. Referring now to FIG. 5A, the display window may be visually divided into several sections. Display box 524 shows the selected macro procedure, in this case the dailycheck procedure as shown in FIG. 2.

[0030] A set of buttons 504 – 522, allow the user to control the execution of macros within the semi-conductor processing system, here a plasma processing chamber. Button 504 allows the user to start the macro comprising steps, as shown in display window 526, and corresponding to the set of macros shown in FIG. 2. Display window 506 and 508 show that first and last steps within the macro that will be executing within macro engine. Button 510 allows the user to stop the macro procedure, button 512 allows the user to abort the macro procedure, and button 514 allows the user to temporarily pause the macro procedure. Where user input is optional, button 518 allows the user to skip user input, as shown in display box 532. Button 520 signals to macro engine that the user has completed user input. Button 522 allows the user to launch a help window, to further explain the current procedure. Display box 530 displays information describing the macro to the user. Display box 534 displays information describing the required user input shown in display box 532. Display box 528 shows the simplified report described in FIG. 3. Referring now to FIG. 5B, the display window of FIG. 5A is shown, with a macro engine help window 536.

[0031] Referring now to FIGS. 6A-B, the macro editor is shown, according to one embodiment of the invention. Although in this example, the macro editor is associated with the Lam software macro engine, the present invention can be applied to other types of semi-conductor processing equipment and software. Generally, a semi-conductor processing system engineer will use a macro editor to create the macro procedure, as shown in FIG. 4. Referring now to FIG. 6A, display box 606 shows the list of available macros for the specific semi-conductor processing system that may be used to construct the dailycheck macro. Furthermore, portions of existing customized macros, as shown in display box 619, may also be ported into the dailycheck macro. Since macros generally execute in sequential order, the engineer can alter an element within the macro procedure by moving it up, at button 616, or down at button 618. Display box 612 displays the

simplified report that will be generated after the dailycheck procedure is executed. The engineer can further edit or add a macro at button 614.

[0032] Referring now to FIG. 6B, a user input window of the macro editor, as shown in FIG. 6A is shown, according to one embodiment of the invention. The selected macro name in entered in display box 622, and a corresponding description is added to display box 624. If the user is required to start the macro, check box 626 is checked. If the test is allowed to continue should a failure occur, check box 628 is selected. The individual steps required for use input are entered in display area 630.

[0033] While this invention has been described in terms of several preferred embodiments, there are alterations, permutations, and equivalents which fall within the scope of this invention. For example, although the drawings are described in the context of plasma processing, it should be understood that the invention also applies to other portions of semi-conductor manufacturing, such as photolithography, direct wafer stepping, die attach, etc. Furthermore, the term semi-conductor processing system is used in its generic sense, and can be understood to comprise equipment within the fabrication facility, directly involved in the production of semi-conductors or glass panels, and which are further capable of storing a control program as a set of macros. It is therefore intended that the following appended claims be interpreted as including all such alterations, permutations, and equivalents as fall within the true spirit and scope of the present invention.

[0034] Advantages of the invention include the optimization of user interaction with semi-conductor processing equipment. Other advantages included potentially reducing process variance between substantially similar semi-conductor processing systems, and further optimizing semi-conductor processing equipment configuration flexibility.

[0035] Having disclosed exemplary embodiments and the best mode, modifications and variations may be made to the disclosed embodiments while remaining within the subject and spirit of the invention as defined by the following claims.

CLAIMS

What is claimed is:

1. A method of automating a set of off-line tasks in a semi-conductor processing system, comprising:

creating, using an editor application, a macro comprising a set of steps, said set of steps pertaining to said set of off-line tasks to be performed prior to processing substrates in said semi-conductor processing system;

providing said macro to a macro execution engine in said semi-conductor processing system;

executing said macro at said semi-conductor processing system, using said macro execution engine, thereby performing said set of steps; and

generating a report using data values collected during said executing.

2. The method of claim 1, wherein one or more steps of said set of steps prevent a waferflow.

3. The method of claim 1, wherein said set of steps are executed by an automatic timer.

4. The method of claim 1, wherein one or more steps of said set of steps prevent wafers from being processed.

5. The method of claim 1, wherein said report is electronically retrieved from said semi-conductor processing system.

6. The method of claim 1, wherein said report is in a spreadsheet format.

7. The method of claim 1, wherein said report is in a text format.

8. The method of claim 1, wherein said report is in a datalog format.

9. The method of claim 1, wherein said report is in a binary format.

10. The method of claim 1, wherein said set of steps is transferred to said semi-conductor processing system during the manufacture of said semi-conductor processing system.

11. The method of claim 1, wherein said set of steps is transferred to said semi-conductor processing system after said semi-conductor processing system has been installed at a semi-conductor fabrication facility.

12. The method of claim 1, wherein said set of steps is obfuscated.

13. The method of claim 1, wherein said set of steps is encrypted.

14. The method of claim 1, where said macro can only be accessed with a password.

15. The method of claim 1, wherein one of said set of steps requires a user input.

16. The method of claim 1, wherein in one of said set of steps, a checklist is presented to a user for manual execution.

17. The method of claim 1, wherein said macro is executed from a remote host.

18. A method of automating a set of off-line tasks in a plurality of semi-conductor processing systems, comprising:

creating, using an editor application, a macro comprising a set of steps, said set of steps pertaining to said set of off-line tasks that are performed prior to processing substrates in said plurality of semi-conductor processing systems;

providing said macro to macro execution engines in said plurality of semi-conductor processing systems;

executing said macro at said plurality of semi-conductor processing systems, using said macro execution engines, thereby performing said set of steps;

generating reports having therein data values collected during said executing at each of said plurality of semi-conductor processing systems; and

providing said reports to a facility for analysis.

19. The method of claim 18 further comprising generating an alert based on said reports.

20. The method of claim 18 wherein said plurality of semi-conductor processing systems is a plurality of plasma processing systems.

21. The method of claim 18, wherein said set of steps is transferred to said plurality of semi-conductor processing systems during manufacture of said plurality of semi-conductor processing systems.

22. The method of claim 18, wherein said set of steps is transferred to one of said plurality of semi-conductor processing systems after said one of said plurality of semi-conductor processing systems has been installed at a semi-conductor fabrication facility.

23. The method of claim 18, wherein said set of steps is obfuscated.

24. The method of claim 18, wherein said set of steps is encrypted.

25. The method of claim 18, wherein one or more steps of said set of steps prevent a waferflow.

26. The method of claim 18, wherein one or more steps of said set of steps prevent wafers from being processed.