[0011] The non-volatile semiconductor memory device 100 thus structured can be configured to write data in a predetermined one of the memory cell transistors 103, read data from a predetermined one of the memory cell transistors 103 and erase data written in the memory cell transistors 103 by regulating voltages to be respectively applied to the higher order bit lines 101a and 101b, the higher order source lines 110a and 110b and the word lines 102a to 102h and by controlling on/off states of the first semiconductor switches 104a to 104d and the second semiconductor switches 111a to 111d.

[0012] In FIG. 6, the memory cell transistor 103 in the first row of the memory block 106a is set as a selected memory cell transistor 115 in which data is written, whereas all the remaining memory cell transistors 103 are set as non-selected memory cell transistors 116 in which data is not written.

[0013] It should be herein noted that for the sake of explanatory convenience, the memory block 106a on which the selected memory cell transistor 115 is disposed will be referred to as a selected block 117, whereas the memory blocks 106b, 106c and 106d on which only the non-selected memory cell transistors 116 are disposed will be referred to as non-selected blocks 118.

[0014] Actually in the non-volatile semiconductor memory device 100, for instance, when data is written in only the selected memory cell transistor 115 in the first row of the selected block 117, a high voltage of 12[V] is applied to a word line 120 (hereinafter referred to as a selected word line) that is the one connected to the selected memory cell transistor 115 among the plural word lines 102a to 102h, whereas a low voltage of 4[V] is applied to the ~~selected~~ word lines 121 (hereinafter referred to as non-selected word lines) that are the other remaining ones among the plural word lines 102a to 102h.

[0015] Further, at this time, in the non-volatile semiconductor memory device 100, a low voltage of 0[V] as a writing voltage can be applied to a higher order bit line 122 (herein referred to as a selected bit line) that is the one to which the selected memory cell transistor 115 is connected, whereas a high voltage of 8[V] as a writing prevention

selected memory cell wiring 18a. And further in the non-volatile semiconductor memory device 1, a voltage of 8[V] is applied to the higher order source line 12b of a memory cell column wiring 18b, i.e., the memory cell column wiring in which only the non-selected blocks 118 are disposed (hereinafter referred to as a non-selected memory cell wiring), while a writing prevention voltage of 8[V] (charge accumulating prevention voltage) can be applied to the higher order bit line 7b of the non-selected memory cell column wiring 18b.

[0046] In addition to this, in the non-volatile semiconductor memory device 1, a P-side gate voltage of 0[V] (first gate voltage) can be configured to be applied to the first selected gate line 108a shared with the selected block 117 in the same row (hereinafter referred to as a selected block row). Accordingly, in the non-selected memory cell column wiring 18b, the PMOS transistor ~~9a~~ 9b to which the writing prevention voltage of 8[V] is being applied from the higher order bit line can be switched on.

[0047] Thus, in the non-volatile semiconductor memory device 1, with the PMOS transistor 9b in the non-selected memory cell column wiring 18b being switched on, the writing prevention voltage of 8[V] can be applied through the PMOS transistor 9b to the lower order bit line 8b of the non-selected memory cell column wiring 18b intersecting with the selected word line 120. At this time, in the non-selected memory cell column wiring 18b, the NMOS transistor 15b is switched off while a voltage of 8[V] is applied thereto from the higher order source line 12b and a voltage of 8[V] is applied thereto from the second selected gate line 113a, and the potential of the lower order source line 13b will be the same as that of the lower order bit line 8b.

[0048] Accordingly, as to a non-selected memory cell transistor 116, i.e., the memory cell transistor at which the selected word line 120 and the lower order bit line 8b of the non-selected memory cell column wiring 18b intersect with each other, the writing prevention voltage of 8[V] is applied to one terminal thereof through the PMOS transistor 9b from the higher order bit line 7b of the non-selected memory cell column wiring 18b, although the high gate voltage of 12[V] is applied

10b, 10c and 10d, the memory block 10a on which the readout memory cell transistor 20 is disposed is referred to as a readout block 22a while the other remaining memory blocks 10b, 10c and 10d are referred to as non-readout blocks 23. Further, the memory cell column wiring 2a in which the readout memory cell transistor 20 is disposed is herein referred to as a selected memory cell column wiring (readout memory cell column wiring) 18a.

[0059] Actually, in the non-volatile semiconductor memory device 1, a fixed voltage of 2[V] can be applied to the higher order source line 12a of the selected memory cell column wiring 18a and the higher order source line 12b of the non-selected memory cell column wiring (non-readout memory cell column wiring) 18b, while a pre-charge voltage of 3[V] can be applied to the higher order bit line 7a of the selected memory cell column wiring 18a. Further, a fixed voltage of 2[V] can be applied to the higher order bit line 7b of the non-selected memory cell column wiring 18b. In the non-volatile semiconductor memory device 1, a P-side gate voltage of 0[V] is applied to the first selected gate line 108a shared in the row in which the readout block 22a is located (hereinafter referred to as a readout block row).

[0060] In other words, as to the PMOS transistor 9a on the readout block 22a, for instance, the pre-charge voltage of 3[V] is applied to the source thereof from the higher order bit line 7a, while the P-side gate voltage of 0[V] is applied to the gate thereof from the first selected gate line 108a. As a result, the PMOS transistor 9a can be switched on. Thus, in the readout block 22a, the pre-charge voltage of 3[V] can be applied from the higher order bit line 7a to ~~each~~ the lower order bit line 8a through the PMOS transistor 9a, and the pre-charge voltage can be applied to one ends of the memory cell transistors 103 connected to ~~each~~ the lower order bit line 8a.

[0061] At this time, an N-side gate voltage of 3[V] can be applied to the second selected gate line 113a shared in the readout block row. Accordingly, as to ~~each~~ the NMOS transistor 15a in the readout block row, the fixed voltage of 2[V] is applied to the source thereof from the higher order source line 12a, while the N-side gate voltage of 3[V]

flowing through the readout memory cell transistor 20.

[0064] It should be noted that at this time, in the row in which only the non-readout blocks 23 are aligned (hereinafter referred to as a non-readout block row), a P-side gate voltage of 3[V] equal to the pre-charge voltage is applied to the respective PMOS transistors 9c and 9d from the first selected gate line 108b, and thereby, the PMOS transistors 9c and 9d can be switched off. Thus, on the non-readout block row, the ~~pre-charge~~ voltages ~~of 3[V]~~ from the higher order bit lines ~~7b~~ 7a and 7b are blocked by the PMOS transistors 9c and 9d. Accordingly, the ~~pre-charge~~ voltages cannot be applied to the non-readout memory cell transistors 21 disposed in the lower order bit lines 8c and 8d connected to the PMOS transistors 9c and 9d.

[0065] Thus, the pre-charge voltage to be applied to the higher order bit line 7a can be configured to be applied to only the readout memory cell transistor 20 from which data is intended to be read out in the selected memory cell column wiring 18a. It should be noted that in the non-readout block row, an N-side gate voltage of 3[V] is applied to the second selected gate line 113b. Accordingly, the NMOS transistors 15c and 15d are switched on, and the fixed voltage is applied without change to the lower order source line 13c from the higher order source line 12a.

[0066] Thus, in the non-volatile semiconductor memory device 1, it can be configured to be determined whether or not data has been written in the readout memory cell transistor 20 by measuring the pre-charge voltage of the higher order bit line 7a, which varies depending on whether or not electric charges are accumulated into the charge accumulation layer of the readout memory cell transistor 20.

[0067] It should be noted that this example describes a case of setting a pre-charge voltage to be 3[V] and of determining whether or not the pre-charge voltage is reduced towards the fixed voltage applied to the source due to the data in the memory cell transistor. However, the pre-charge voltage is not necessarily higher than the fixed voltage. For example, it is also possible to determine whether or not data has been written in the readout memory cell transistor 20 by variously

18b through the lower order bit line 8b while the PMOS transistor 9b is being switched on. And simultaneously with this, in the selected memory cell column wiring 18a, the writing voltage can be applied to the selected memory cell transistor 115 from the NMOS transistor 15a through the lower order source line 13a while the NMOS transistor 15a is being switched on.

[0084] Here, in the non-volatile semiconductor memory device 1, the writing gate voltage of 12[V] is applied as $V_{W1}$ to the selected word line 120 while the writing prevention gate voltage of 4[V] is applied as $V_{W2}$ to the non-selected word lines 121. Thus, $V_{W1} - V_{W2} < 9[V]$ is set as a voltage condition and a voltage difference to be controlled by the peripheral circuit of the word lines 102a to 102h is set to be less than 9[V]. Hence, MOS transistors (not shown in the figures), respectively including a gate insulating layer with a thickness of less than 13[nm], can be used in the peripheral circuit without using special MOS transistors respectively having a gate insulating layer with a large thickness in the peripheral circuit.

[0085] Further, in the non-volatile semiconductor memory device 1, the writing prevention voltage of 8[V] is applied as $V_{B1}$ to the higher order bit line 7b of the non-selected memory cell column wiring 18b, while the writing voltage of 0[V] is applied as $V_{B2}$ to the higher order bit line 7a of the selected memory cell column wiring 18a. Thus, $V_{B1} - V_{B2} < 9[V]$ is set as a voltage condition and a voltage difference to be controlled by the peripheral circuit of the higher order bit lines 7a and 7b is set to be less than 9[V]. Hence, MOS transistors (not shown in the figures), respectively including a gate insulating layer with a thickness of less than 13[nm], can be used in the peripheral circuit without using special MOS transistors respectively having a gate insulating layer with a large thickness in the peripheral circuit.

[0086] Further, in the non-volatile semiconductor memory device 1, the writing prevention voltage of 8[V] is applied as ~~$V_{B2}$~~-$V_{B1}$ to the higher order bit line 7b of the non-selected memory cell column wiring 18b, and the gate voltage of the PMOS transistor 9a is adjusted. An gate-to-substrate voltage $V_{GW}$ of the PMOS transistor 9b is thereby set

to be lower than the writing prevention voltage. Hence, $V_{B2}-V_{B1} > V_{GW}$ can be set as a voltage condition. Thus, in the non-volatile semiconductor memory device 1, it is possible to suppress the voltage to be applied to the PMOS transistor 9b, and to form the gate insulating layer with a film thickness of less than 13[nm] between the gate and the semiconductor substrate in the PMOS transistor 9b.

[0087] Here, when the PMOS transistors 9a and 9b are switched on while a gate voltage of 7[V] is applied thereto where the substrate voltages thereof are both set to be 8[V], the gate-to-substrate voltages of the PMOS transistors 9a and 9b become 1[V], and electric fields to be applied to the gate insulating films of the PMOS transistors 9a and 9b can be remarkably reduced. Similarly, when the NMOS transistors 15a and 15b are switched on while a gate voltage of 1[V] is applied thereto where the substrate voltages thereof are both set to be 0V, the gate-to-substrate voltages of the NMOS transistors 15a and 15b become 1[V], and electric fields to be applied to the gate insulating films of the NMOS transistors 15a and 15b can be remarkably reduced. As a result, reliability of the gate insulating films can be remarkably enhanced. And thus, in the non-volatile semiconductor memory device 1, voltages to be applied to the NMOS transistors 15a and 15b can be suppressed. Therefore, it is possible to form the gate insulating film with a film thickness of less than 13[nm] between the gate and the semiconductor substrate in the NMOS transistor 15a.

[0088] In other words, such remarkable relaxation of electric field cannot be achieved when either NMOS transistors or PMOS transistors are configured to apply both of the writing voltage and the writing prevention voltage as with a conventional device. In comparison with this, in the present invention, combinational use of the PMOS transistors and the NMOS transistors can remarkably contribute to enhancement in reliability of the gate insulating films.

[0089] It should be noted that in the erasing action shown in FIG. 4, the case has been exemplified that the voltage of 0[V] is applied to the second selected gate line 113a, and thereby, the gate voltages of the NMOS transistors 15a and 15b are set to be 0[V]. However, the

Non-volatile Semiconductor Memory Device According to First Exemplary Embodiment

It should be noted that the aforementioned exemplary embodiment has described the case of applying the non-volatile semiconductor memory device 1 as a non-volatile semiconductor memory device configured to: apply an N-side gate voltage greater than or equal to ~~$V_{B1}$~~-$V_{B2}$ + $|V_{thn}|$ (where ~~$V_{B1}$~~-$V_{B2}$ is the voltage of the selected memory cell column wiring (writing voltage), while $V_{thn}$ is the threshold voltage of the NMOS transistor) to the NMOS transistor; and apply a P-side gate voltage less than or equal to ~~$V_{B2}$~~-$V_{B1}$ - $|V_{thp}|$ (where ~~$V_{B2}$~~-$V_{B1}$ is the voltage of the non-selected memory cell column wiring (writing prevention voltage), while $V_{thp}$ is the threshold voltage of the PMOS transistor) to the PMOS transistor, in writing data in the selected memory cell transistor. The non-volatile semiconductor memory device 1 is herein configured to: apply the N-side gate voltage of 8[V] greater than or equal to ~~$V_{B1}$~~-$V_{B2}$ + $|V_{thn}|$ to the NMOS transistor 15a; and apply the P-side gate voltage of 0[V] less than or equal to ~~$V_{B2}$~~-$V_{B1}$ - $|V_{thp}|$ to the PMOS transistor 9b. However, the present invention is not limited to this. As long as the N-side gate voltage to be applied to the NMOS transistor is greater than or equal to ~~$V_{B1}$~~-$V_{B2}$ + $|V_{thn}|$ while the P-side gate voltage to be applied to the PMOS transistor is less than or equal to ~~$V_{B2}$~~-$V_{B1}$ - $|V_{thp}|$, the N-side gate voltage and the P-side gate voltage may be variously set to have other voltage values.

[0097] Further, the aforementioned exemplary embodiment has explained the case that $V_{W1} - V_{W2} < 9$[V] (where $V_{W1}$ is the accumulating gate voltage of the selected word line while $V_{W2}$ is the accumulating prevention gate voltage of the non-selected word line) is established as a relational equation in accumulating electric charges into the selected memory cell transistor, and the condition that the voltage difference between $V_{W1}$ and $V_{W2}$ is less than 9[V] is configured to be satisfied by applying the writing gate voltage of 12[V] as $V_{W1}$ to the selected word line 120 and by applying the writing prevention gate voltage of 4[V] as $V_{W2}$ to the non-selected word lines 121. However, the present invention is not limited to this. As long as the

aforementioned condition of $V_{W1} - V_{W2} < 9[V]$ is satisfied, the voltages to be applied to the selected word line and the non-selected word line may be set to have various voltage values.

[0098] Further, the aforementioned exemplary embodiment has described the case that $V_{B1} - V_{B2} < 9[V]$ (where $V_{B1}$ is the charge accumulating prevention voltage of the non-selected memory cell column wiring while $V_{B2}$ is the charge accumulating ~~prevention~~ voltage of the ~~non~~-selected memory cell column wiring) is established as a relational equation in accumulating electric charges into the selected memory cell transistor, and the condition that the voltage difference between $V_{B1}$ and $V_{B2}$ is less than 9[V] is configured to be satisfied by applying the writing prevention voltage of 8[V] as $V_{B1}$ to the higher order bit line 7b of the non-selected memory cell column wiring 18b and by applying the writing voltage of 0[V] as $V_{B2}$ to the higher order bit line 7a of the selected memory cell column wiring 18a. However, the present invention is not limited to this. As long as the aforementioned condition of $V_{B1} - V_{B2} < 9[V]$ is satisfied, the voltages to be applied to the selected memory cell column wiring 18a and the non-selected memory cell column wiring 18b may be set to have various voltage values.

[0099] Further, the aforementioned exemplary embodiment has described the case that voltage is applied to the source line of the non-selected memory cell column wiring in accumulating electric charges into the selected memory cell transistor, where the voltage, applied to the source line of the non-selected memory cell column wiring, is set to have a voltage value, which is less than that of the voltage to be applied to the bit line of the non-selected memory cell column wiring and is also greater than or equal to that obtained by subtracting the threshold voltage $V_{thn}$ of the NMOS transistor from that of the N-side gate voltage to be applied to the NMOS transistor. However, the present invention is not limited to this. For example, any of the following conditions may be configured to be satisfied: that voltage is applied to the bit line of the selected memory cell column wiring in accumulating electric charges into the selected memory cell transistor, where the voltage, applied to the bit line of the selected memory cell

of switching on the PMOS transistor 9b, i.e., a condition of writing prevention voltage of 8[V] - $|V_{thp}| > V_{GP}$.

[0103] The PMOS transistor 9b, to the ~~drain~~ source of which the writing prevention voltage of 8[V] is applied from the higher order bit line 7b of the non-selected memory cell column wiring 18b, is switched on when the P-side gate voltage $V_{GP}$ of less than 8[V] is applied thereto, and the writing prevention voltage of 8[V] can be applied to the lower order bit line 8b of the non-selected memory cell column wiring 18b intersecting with the selected word line 120. At this time, as to the non-selected memory cell column wiring 18b, a voltage of 8[V] is being applied to the NMOS transistor 15b from the higher order source line 12b, while a voltage of 1[V] is being applied to the NMOS transistor 15b from the second selected gate line 113a. Therefore, the NMOS transistor 15b is switched off and the electric potential of the lower order source line 13b becomes the same as that of the lower order bit line 8b.

[0104] Accordingly, as to the non-selected memory cell transistor 116 at which the selected word line 120 and the lower order bit line 8b of the non-selected memory cell column wiring 18b intersect with each other, the writing prevention voltage of 8[V] is applied to one terminal thereof from the higher order bit line 7b of the non-selected memory cell column wiring 18b through the PMOS transistor 9b, although a high voltage of 12[V] as a gate voltage is applied to the control gate thereof from the selected word line 120. Therefore, a voltage difference is reduced between the control gate and the channel region, and electric charges cannot be injected into the charge accumulation layer from the channel region without occurrence of a quantum tunneling effect.

[0105] Further, at this time, in the non-volatile semiconductor memory device 25, an N-side gate voltage of greater than 0[V] can be applied to the second selected gate line 113a shared in the selected block row. The voltage of greater than 0[V] of the N-side gate voltage $V_{GN}$ is herein the one set based on a writing voltage of 0[V] to be applied to the higher order source line 12a of the selected memory cell column wiring 18a and a threshold voltage $V_{thn}$ of the NMOS transistor 15a in

higher order bit line 7a as long as the PMOS transistor 9a in the selected memory cell column wiring 18a can be switched off. On the other hand, various voltages may be applied to the higher order source line 12b as long as the NMOS transistor 15b in the non-selected memory cell column wiring 18b can be switched off.

[0109] The PMOS transistor 9a in the selected memory cell column wiring 18a may be switched off by applying, for instance, a selected bit voltage ~~$V_{B1}$~~-$V_{B2}$ of 4[V] to the higher order bit line 7a of one selected memory cell column wiring 18a, whereas the NMOS transistor 15b in the non-selected memory cell column wiring 18b may be switched off by applying, for instance, a non-selected source voltage $V_{S1}$ of 4[V] to the higher order source line 12b of the other non-selected memory cell column wiring 18b.

[0110] The selected bit voltage ~~$V_{B1}$~~-$V_{B2}$ is the one set for satisfying a condition that the voltage value thereof is greater than or equal to that of the writing voltage to be applied to the higher order ~~bit~~ source line ~~7a~~-12a of the selected memory cell column wiring 18a while being less than or equal to that obtained by adding a threshold voltage $|V_{thp}|$ of the PMOS transistor 9a to a P-side gate voltage $V_{GP}$ to be applied to the PMOS transistor 9a of the selected memory cell column wiring 18a (i.e., less than or equal to ($V_{GP}$ + $|V_{thp}|$)).

[0111] On the other hand, the non-selected source voltage $V_{S1}$ is the one set for satisfying a condition that the voltage value thereof is less than that of the writing prevention voltage to be applied to the higher order bit line 7b of the non-selected memory cell column wiring 18b while being greater than or equal to that obtained by subtracting a threshold voltage $V_{thn}$ of the NMOS transistor 15b from an N-side gate voltage $V_{GN}$ to be applied to the NMOS transistor 15b in the non-selected memory cell column wiring 18b (i.e., greater than or equal to ($V_{GN}$ - $V_{thn}$)). Even with the aforementioned configuration, a non-volatile semiconductor memory device 31 can achieve advantageous effects similar to those of the aforementioned exemplary embodiment.

[0112] Further, thus in the present invention, the source voltage is adjustable in addition to the gate voltage, and for instance, the

selected bit voltage ~~$V_{B1}$~~-$V_{B2}$ of 4[V] can be applied to the higher order bit line 7a, while the non-selected source voltage $V_{S1}$ of 4[V] can be applied to the higher order source line 12b. Therefore, it is possible to reduce a voltage difference between the source and gate voltages to be applied to the PMOS transistor 9c (in this case, source voltage of 4[V] - gate voltage of 8[V] = voltage difference of 4[V]) and a voltage difference between the source and gate voltages to be applied to the NMOS transistor 15d (in this case, source voltage of 4[V] - gate voltage of 0[V] = voltage difference of 4[V]). Accordingly, it is possible to remarkably relax electric fields applied to the gate insulating films of the PMOS transistor 9c and the NMOS transistor 15d, and to achieve enhancement in reliability of the transistors.

[0113] (2) Other Exemplary Embodiment

It should be noted that the present invention is not limited to the aforementioned exemplary embodiment, and a variety of modifications can be made within the scope of the present invention. For example, a non-volatile semiconductor memory device may be applied that is obtained by an arbitrary combination of the aforementioned non-volatile semiconductor memory devices 1 and 25 according to the first exemplary embodiment.

[0114] Further, the aforementioned exemplary embodiment has described the case that a SONOS memory cell transistor capable of accumulating electric charges into a silicon nitride film layer is applied as a memory cell transistor capable of accumulating electric charges into a charge accumulation layer. However, the present invention is not limited to this, and any other various memory cell transistors may be applied, such as a stack-type memory cell transistor in which a conductive polysilicon is disposed on a tunnel oxide film and electric charges are accumulated into the floating gate thereof.

[0115] Further, the aforementioned exemplary embodiment has described the case of applying the non-volatile semiconductor memory device 1, 25 having totally four memory blocks 10a, 10b, 10c and 10d formed in the matrix of two rows and two columns. However, the present invention is not limited to this. For example, a non-volatile