

CLAIMS

WHAT IS CLAIMED IS:

1. A power adjustment method of an upper electrode power supply of a semiconductor process apparatus, comprising:

obtaining a corresponding processing load of an upper electrode power supply of a reference process chamber when performing a semiconductor process step and a corresponding processing load of an upper electrode power supply of a current process chamber when performing the semiconductor process step;

determining a corresponding compensation coefficient for the current process chamber when performing the semiconductor process step according to the corresponding processing load of the current process chamber and the corresponding processing load of the reference process chamber; and

when the semiconductor process step is performed, controlling the upper electrode power supply of the current process chamber to output a compensation power, the compensation power being a product of a rated power of the upper electrode power supply set in the semiconductor process step performed by the current process chamber and the corresponding compensation coefficient.

2. The power adjustment method according to claim 1, wherein the compensation coefficient is a ratio of the corresponding processing load of the current process chamber when performing the semiconductor process step to the corresponding processing load of the reference process chamber when performing the semiconductor process step.

3. The power adjustment method according to claim 1 or 2, wherein upper electrode circuits are arranged at the reference process chamber and the current process chamber, the upper electrode power supply is configured to output power to the corresponding process chamber through a corresponding upper electrode circuit, and obtaining the corresponding processing load of the upper electrode power supply of the reference process chamber when performing the semiconductor process step and the corresponding processing load of the upper electrode power supply of the current process chamber when performing the semiconductor process step includes:

obtaining a plasma load corresponding to each semiconductor process step;

adding a circuit load corresponding to the reference process chamber and the plasma load of the performed semiconductor process step to obtain the processing load of the reference process chamber when performing the corresponding semiconductor process step; and

adding a circuit load corresponding to the current process chamber and the plasma load of the performed semiconductor process step to obtain the processing load of the current process chamber when performing the corresponding semiconductor process step.

4. The power adjustment method according to claim 3, wherein obtaining the plasma load corresponding to each semiconductor process step includes:

when performing each semiconductor process step, controlling the upper electrode power supply of any process chamber to output a processing power and detecting a process current between the upper electrode power supply and the corresponding process chamber;

obtaining the processing load of the process chamber corresponding to each semiconductor process step according to the processing power and the process current; and

subtracting the circuit load corresponding to the process chamber from the processing load of the process chamber corresponding to each semiconductor process step to obtain the plasma load corresponding to each semiconductor process step.

5. The power adjustment method according to claim 4, wherein the processing load is a ratio of the processing power to square of the process current.

6. The power adjustment method according to claim 4, wherein the circuit load corresponding to each process chamber is obtained by:

controlling the upper electrode power supply corresponding to each process chamber to output detection power to detect a detection current between each upper electrode power supply and the corresponding process chamber, the plasma being not ignited in the process chamber under the detection power; and

obtaining the circuit load corresponding to each process chamber according to the detection power and detection current corresponding to each process chamber.

7. The power adjustment method according to claim 6, wherein the circuit load is a ratio of the detection power to square of the detection current.

8. A semiconductor process apparatus, comprising:

a plurality of process chambers, each process chamber comprising an upper electrode power supply configured to apply a radio frequency power to an inductive coupling coil;

an acquisition unit configured to obtain a corresponding processing load of an upper electrode power supply of a reference process chamber when performing a semiconductor process step and a corresponding processing load of an upper electrode power supply of a current process chamber when performing the semiconductor step, wherein the reference process chamber is one of the plurality of process chambers, and the current process chamber is any other of the plurality of process chambers except for the reference process chamber;

a calculation unit configured to determine a corresponding compensation coefficient for the current process chamber when performing the semiconductor process step according to the corresponding processing load of the current process chamber and the corresponding processing load of the reference process chamber; and

a control unit configured to control, when the semiconductor process step is performed, the upper electrode power supply of the current process chamber to output a compensation power, the compensation power being a product of a rated power of the upper electrode power supply set in the semiconductor process step performed by the current process chamber and the corresponding compensation coefficient.

9. A semiconductor process apparatus, comprising:

a current process chamber, which comprises an upper electrode power supply configured to apply a radio frequency power to an inductive coupling coil when performing a semiconductor process step;

an acquisition unit configured to obtain a corresponding processing load of the upper electrode power supply of the current process chamber when performing the semiconductor process step and a corresponding processing load of an upper electrode power supply of a

reference process chamber belonging to a different semiconductor process apparatus when performing the semiconductor process step;

a calculation unit configured to determine a corresponding compensation coefficient for the current process chamber when performing the semiconductor process step according to the corresponding processing load of the current process chamber and the corresponding processing load of the reference process chamber; and

a control unit configured to control, when the semiconductor process step is performed, the upper electrode power supply of the current process chamber to output a compensation power, the compensation power being a product of a rated power of the upper electrode power supply set in the semiconductor process step performed by the current process chamber and the corresponding compensation coefficient.

10. The semiconductor process apparatus according to claim 8 or 9, wherein the semiconductor process apparatus further includes a plurality of current detection devices, wherein the plurality of current detection devices are arranged between a plurality of upper electrode power supplies and corresponding process chambers in a one-to-one correspondence, and the current detection devices are configured to obtain the process current and/or the detection current between each of the upper electrode power supplies and the corresponding process chamber, and the detection current refers to a current outputted by the upper electrode power supply when the plasma is not ignited in the process chamber.