PROCESS TO FABRICATE A NOVEL SOURCE-DRAIN EXTENSION

ABSTRACT

A process for fabricating a MOSFET device, featuring source/drain extension regions, formed after the utilization of high temperature processes, such as heavily doped source/drain regions, has been developed. Disposable insulator spacers are formed on the sides of doped, SEG silicon regions, followed formation of a gate insulator layer, and an overlying gate structure, on a region of the semiconductor substrate located between the doped SEG silicon regions. The temperature experienced during these process steps result in the formation of the heavily doped source/drain, underlying the SEG silicon regions. Selective removal of the disposable spacers, allows the source/drain extension regions to be placed in the space vacated by the disposable spacers, adjacent to the heavily doped source/drain region. Insulator spacers are then used to fill the spaces vacated by removal of the disposable spacers, directly overlying the source/drain extension regions. Additional iterations include the use of an L shaped spacer, overlying the source/drain extension region, as well as the formation of metal silicide, on the doped SEG silicon regions, and on the gate structures.

Figure no. 1 is suggested for publication

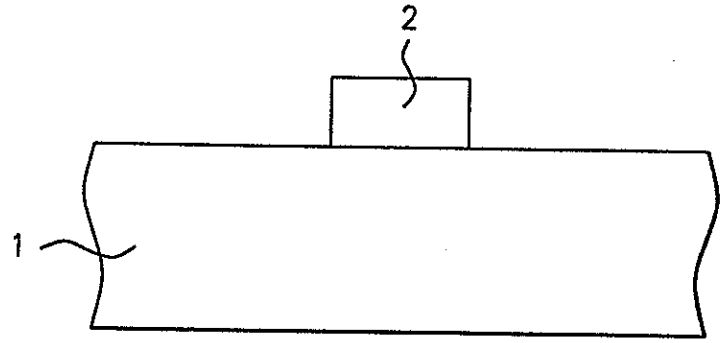


FIG. 1

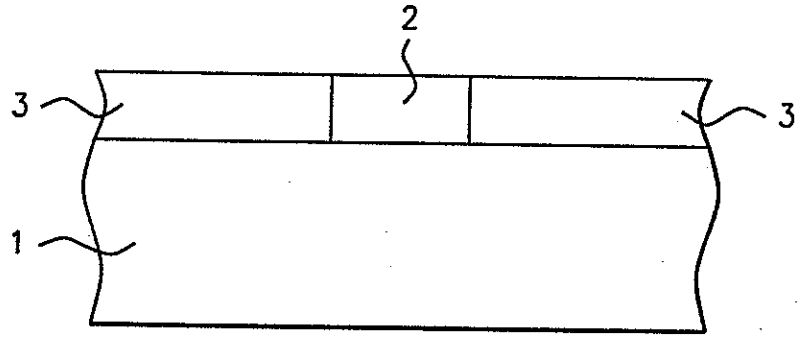


FIG. 2

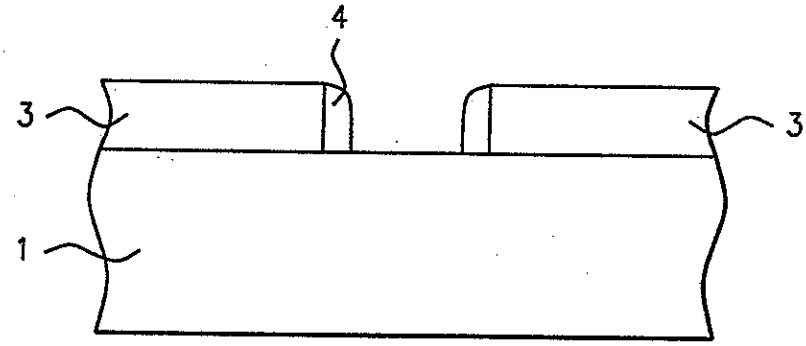


FIG. 3